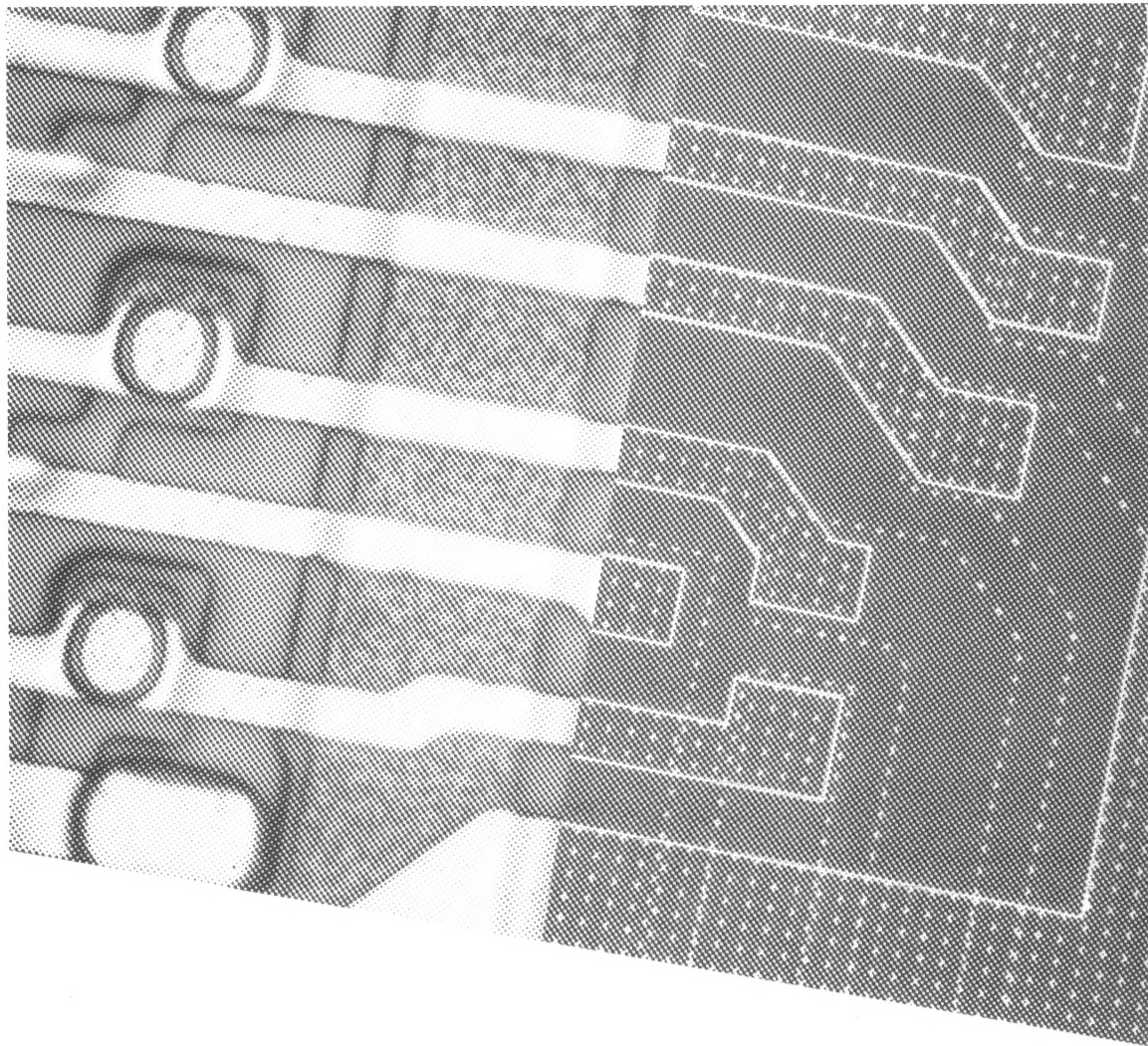


intel[®]

System Data Catalog

August
1978

BROWNING, S. L.



Intel was organized in 1968 to utilize the rapidly expanding technology of integrated electronics. During its brief history, Intel has become the world's largest supplier of MOS circuits, and is in the top ten of the world's producers of all semiconductor devices.

This System Data Catalog provides complete specifications on most of Intel standard memory systems, single board computers, Intellec microcomputer development systems, software, and peripherals. Margin tabs provide quick guides to major product categories; indexes located in Section 1 and at the beginning of each section allow location of specific products. Information on ordering, product flow, and technical literature may be found in Section 2.

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Telephone: (408) 987-8080
TWX: 910-338-0026 • Telex: 34-6372

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System Data Catalog

August
1978

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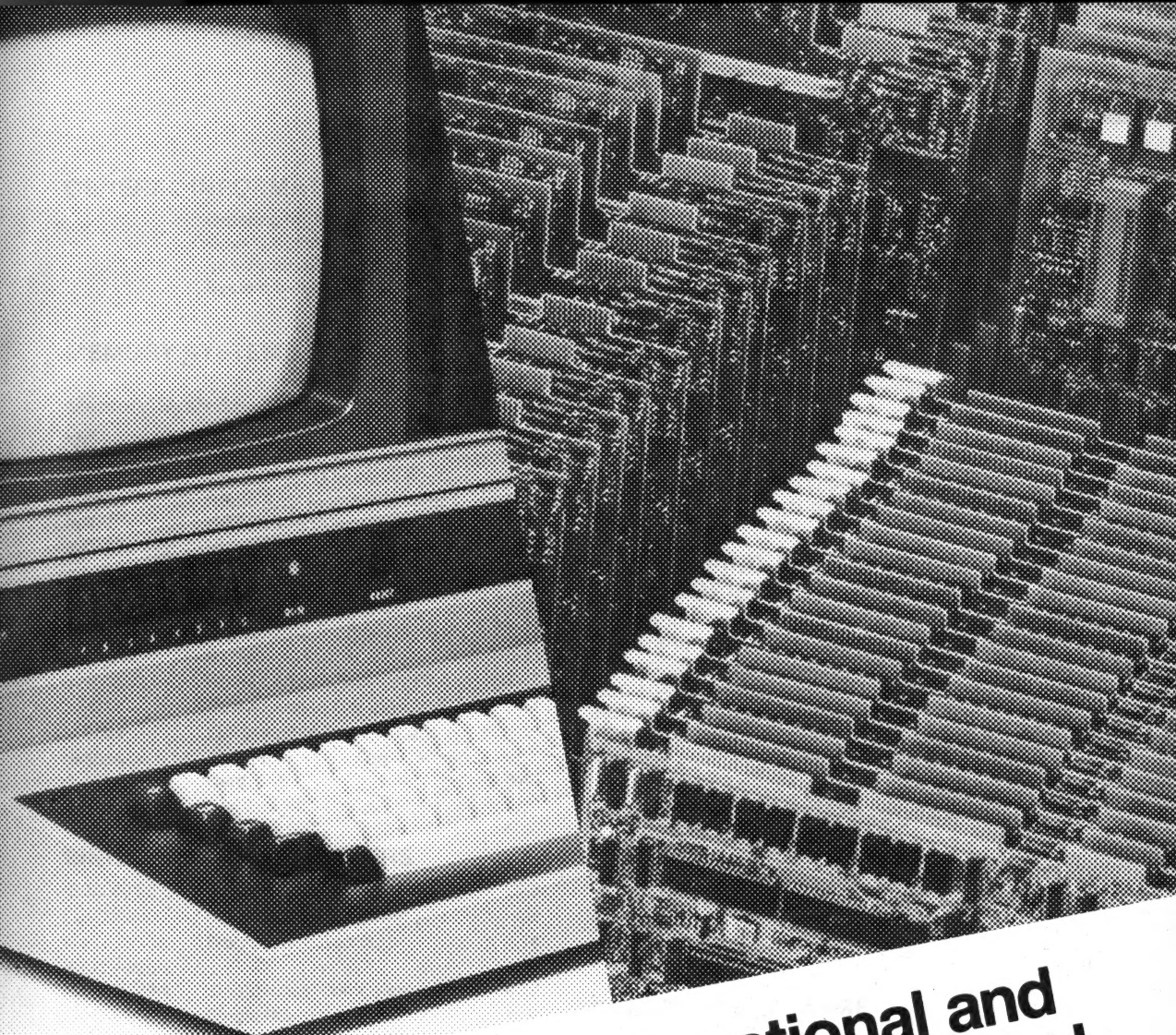
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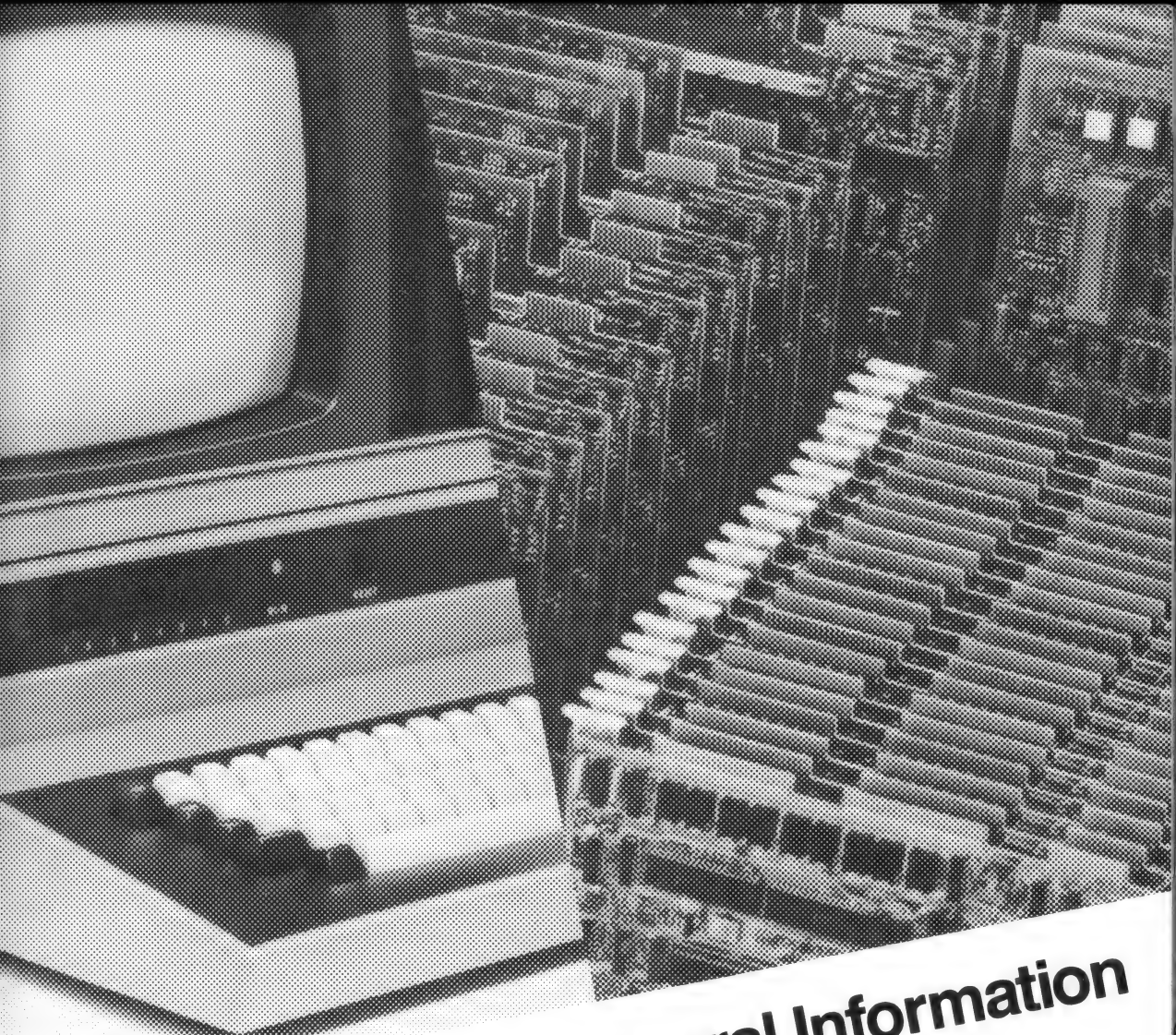
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ORDERING INFORMATION

PART NUMBERS

All products described in this catalog, including boards, systems, kits, and other peripheral support equipment, may be ordered using the part or model number designations listed under Ordering Information on each data sheet.

OPTIONS

The latest Intel OEM price list should be consulted for availability of various options. It may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

QUALITY ASSURANCE

A typical product flow



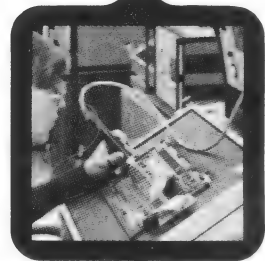
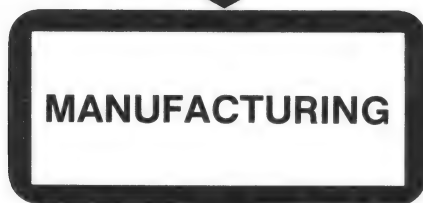
Gold Thickness Measurement on Raw Boards



Kit Audit



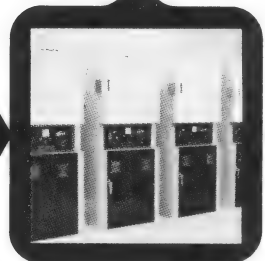
Automatic Test Systems Utilized in Board Testing



Single Board Computer Test Fixture



Visual Inspection of Printed Wire Assemblies



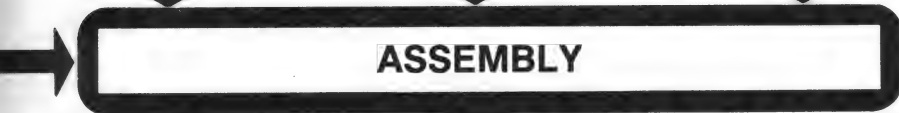
Ovens Utilized for Board Pre-Bake

Cable Testing Using an Automatic Test System

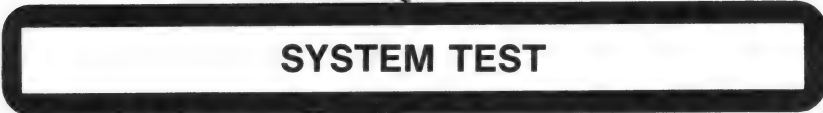
Checking Alignment of Floppy Disk Drives

XYZ Measurement of Sheet Metal

GENERAL



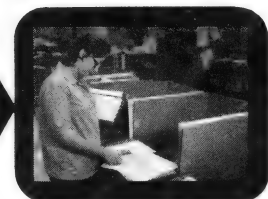
In-Process QC of System in Assembly



Aging in System Test



Boot-Up Test in System Test



Shipping Inspection

INTEL PRODUCT LITERATURE

The accelerating rate of new developments in microprocessors and memories has created the need for concise, up-to-the-minute design information. To assist customers in maintaining expertise in state of the art systems, Intel provides a variety of sales and technical literature including brochures, data sheets, application notes, handbooks, and technical manuals containing comprehensive information on microprocessors, microcomputers, memories, development systems, and software. The literature supplied without charge for each product is listed under Reference Manuals in the specifications section of each data sheet.

SALES LITERATURE

Catalogs

110400	1978 Component Data Catalog	\$3.00
610200	1978 System Data Catalog	\$2.00

Brochures

Microcomputer Product Line Brochure	N/C
8086 Brochure	N/C
iSBC 80 and System 80 Microcomputers Folder-Full (Configuration Guide)	N/C
Microcomputer Components Brochure	N/C
Memory Components Brochure	N/C
ICE-85 Brochure	N/C
Growing Static RAM Family Album	N/C
MOS RAMs Brochure	N/C
μScope 820 Brochure	N/C
PL/M Applications Brochure	N/C
1978 Intel Microcomputer Workshops Brochure	N/C

Application Notes

AP 4	2107A Application Note	N/C
AP 12	5101 Application Note	N/C
AP 15	8255 Programmable Peripheral Interface	N/C
AP 16	Using the 8251 Application Note	N/C
AP 17	2709 8K Erasable PROM Application Note	N/C
AP 22	Which Way For 16K	N/C
AP 23	2104A 4K RAM	N/C
AP 24	MCS-48 Family — 9800413B	N/C
AP 26	iSBC 80/10 & System 80/10	N/C
AP 27	Control With UPI-41	N/C
AP 28	Multibus Interfacing — 9800587A	N/C
AP 29	Using The Intel 8085 Serial I/O Lines	N/C
AP 30	Applications of 5 Volt EPROM and ROM Family for Microprocessor Systems	N/C
AP 31	Using the 8259 — 9800658A	N/C
AP 32	8275 & 8279 — 9800576	N/C
AP 33	RMX/80 — 9800577A	N/C
AP 35	CRYSTALS: Specifications — 9800652A	N/C

AP 36	Using the 8273 — 9800667A	N/C
AP 38	Applications Techniques For 8085A Bus — 9800703A	N/C
AP 40	Keyboard/Display Scanning With Intel's MCS-48 Microcomputers	N/C
AP 42	Writing Diagnostics for the μScope	N/C

Product Descriptions

9800365	MCS-85 Product Description	N/C
9800600	Peripherals Product Description	N/C
9800606	Intellec Series II Microcomputer Development Systems Functional Description and Specifications	N/C
9800615	MCS-48 Single Chip Family of Microcomputers Product Description	N/C
9800723	MCS-86 Product Description	N/C

Reference Cards

9800404	PROMPT48 Reference Cardlet	N/C
9800438	8085/8080 Assembly Language Reference Card	N/C
9800547	FORTRAN-80 Reference Card	N/C
9800582	μScope 820 8080A Operator's Reference Card	N/C
9800653	MCS-48 In-Circuit Emulator Reference Card	N/C
	MCS-48 Assembly Language Reference Card — July 1977	N/C
	UPI-41 Assembly Language Reference Card — June 1977	N/C

Reliability Reports

RR 7	2107A/2107B 4K Dynamic RAM	N/C
RR 8	Polysilicon Fuse Bipolar PROM	N/C
RR 9	MOS Static RAMs	N/C
RR 10	8080/8080A Microcomputer	N/C
RR 11	2416 16K CCD Memory	N/C
RR 12	2708 8K Erasable PROM	N/C
RR 14	2115/2125 MOS Static RAMs	N/C
RR 15	2104A 4K Dynamic RAM	N/C
RR 16	2116 16K Dynamic RAM	N/C
RR 17	iSBC 80/10 Single Board Computer	N/C
RR 18	H MOS Reliability	N/C

PRODUCT LITERATURE

TECHNICAL LITERATURE

Data Sheets

Each of the data sheets included in this catalog may be ordered separately. A complete listing of these data sheets by product name is included in the functional index in Section 1.

User's Guides

9800016	High Speed Paper Tape Reader Installation and Operation Guide	\$2.50
9800203	MCS-80 System Design Kit User's Guide	\$5.00
9800223	SBC 80P and SBC 80P10 Prototyping Package User's Guide	\$5.00
9800298	iSBC 635 Power Supply User's Guide	\$5.00
9800306	ISIS-II User's Guide	\$15.00
9800338	SBC 80P20 User's Guide	\$5.00
9800350	SBC 915 Go/No Go Diskette Diagnostic and Monitor Program User's Guide	\$5.00
9800354	SBC 925 Go/No Go Diskette Diagnostic and Monitor Program User's Guide	\$5.00
9800508	SBC 80P05 User's Guide	\$5.00
9800522	RMX/80 User's Guide	\$5.00
9800557	Intellec Series II Model 210 User's Guide	\$15.00
9800558	A Guide to Intellec Microcomputer Development Systems, by Daniel D. McCracken	\$2.00
	A Guide to PL/M Programming for Microcomputer Applications, by Daniel D. McCracken	\$9.95

9800185	In-Circuit Emulator/80 Operator's Manual	\$15.00
9800206	ISIS-I Diskette Operating System Operator's Manual	\$15.00
9800210	Series 3000 Microprogramming Manual	\$5.00
9800212	Diskette Operating System Microcomputer Development System MDS DOS Hardware Reference Manual	\$25.00
9800220	In-Circuit Emulator/30 Microcomputer Development System ICE-30 Hardware Reference Manual	\$25.00
9800221	Series 3000 Reference Manual	\$5.00
9800230	SBC 80/10 and SBC 80/10A Single Board Computer Hardware Reference Manual	\$5.00
9800236	Universal PROM Programmer Microcomputer Development System Peripheral Universal PROM Mapper Operator's Manual	\$15.00
9800255	MCS-48 and UPI-41 Assembly Language Programming Manual	\$5.00
9800265	SBC 416 16K PROM/ROM Expansion Board Hardware Reference Manual	\$5.00
9800268	PL/M Programming Manual	\$5.00
9800270	MCS-48 Family of Single Chip Microcomputers User's Manual	\$5.00
9800277	iSBC 104/108/116 Combination Memory and I/O Expansion Boards Hardware Reference Manual	\$5.00
9800278	SBC 508 I/O Expansion Board Hardware Reference Manual	\$5.00
9800279	SBC 016 16K RAM Expansion Board Hardware Reference Manual	\$5.00
9800292	ISIS-II 8080/8085 Macro Assembler Operator's Manual	\$10.00
9800294	SBC 501 Direct Memory Access Controller Hardware Reference Manual	\$5.00
9800297	SBC 630 Power Supply User's Manual	\$5.00
9800300	ISIS-II PL/M-80 Compiler Operator's Manual	\$15.00
9800301	8080/8085 Assembly Language Programming Manual	\$5.00
9800307	Intellec PROMPT 80/85 User's Manual	\$5.00
9800316	System 80/10 Microcomputer Hardware Reference Manual	\$5.00
9800317	SBC 80/20 and SBC 80/20-4 Single Board Computer Hardware Reference Manual	\$5.00
9800349	SBC 211/212 Diskette Hardware System Hardware Reference Manual	\$5.00

Manuals

9800017	MCS-8 User's Manual	\$2.50
9800019	8008 Assembly Language Programming Manual	\$5.00
9800025	4004/4040 Assembly Language Programming Manual	\$5.00
9800042	MCS-40 User's Manual	\$5.00
9800129	Intellec 800 Microcomputer Development System Operator's Manual	\$15.00
9800132	Intellec Microcomputer Development System Reference Manual	\$25.00
9800133	Universal PROM Programmer Reference Manual	\$25.00
9800153	MCS-80 User's Manual	\$7.50
9800167	In-Circuit Emulator/80 Microcomputer Development System Hardware Reference Manual	\$25.00
9800172	ROM Simulator Microcomputer Development System ROM SIM Reference Manual	\$25.00

PRODUCT LITERATURE

GENERAL

9800366	MCS-85 User's Manual	\$5.00	9800488	SBC 032/048/064 Random Access Memory Boards Hardware Reference Manual	\$5.00
9800385	SBC 519 Programmable I/O Expansion Board Hardware Reference Manual	\$5.00	9800489	SBC 556 Optically Isolated Programmable I/O Board Hardware Reference Manual	\$5.00
9800386	Intellec Microcomputer Development System Diagnostic Confidence Test Operator's Manual	\$5.00	9800504	UPI-41 User's Manual	\$5.00
9800388	SBC 517 Combination I/O Expansion Board Hardware Reference Manual	\$5.00	9800505	SBC 660 System Chassis Hardware Reference Manual	\$5.00
9800402	PROMPT48 Microcomputer User's Manual	\$5.00	9800559	Intellec Series II Installation and Service Manual	\$15.00
9800410	SBC 310 High-Speed Mathematics Unit Hardware Reference Manual	\$5.00	9800592	μScope 8080A Probe Service Manual	\$15.00
9800420	SBC 202 Double Density Diskette Controller Hardware Reference Manual	\$5.00	9800593	μScope 820 Microprocessor System Console Service Manual	\$15.00
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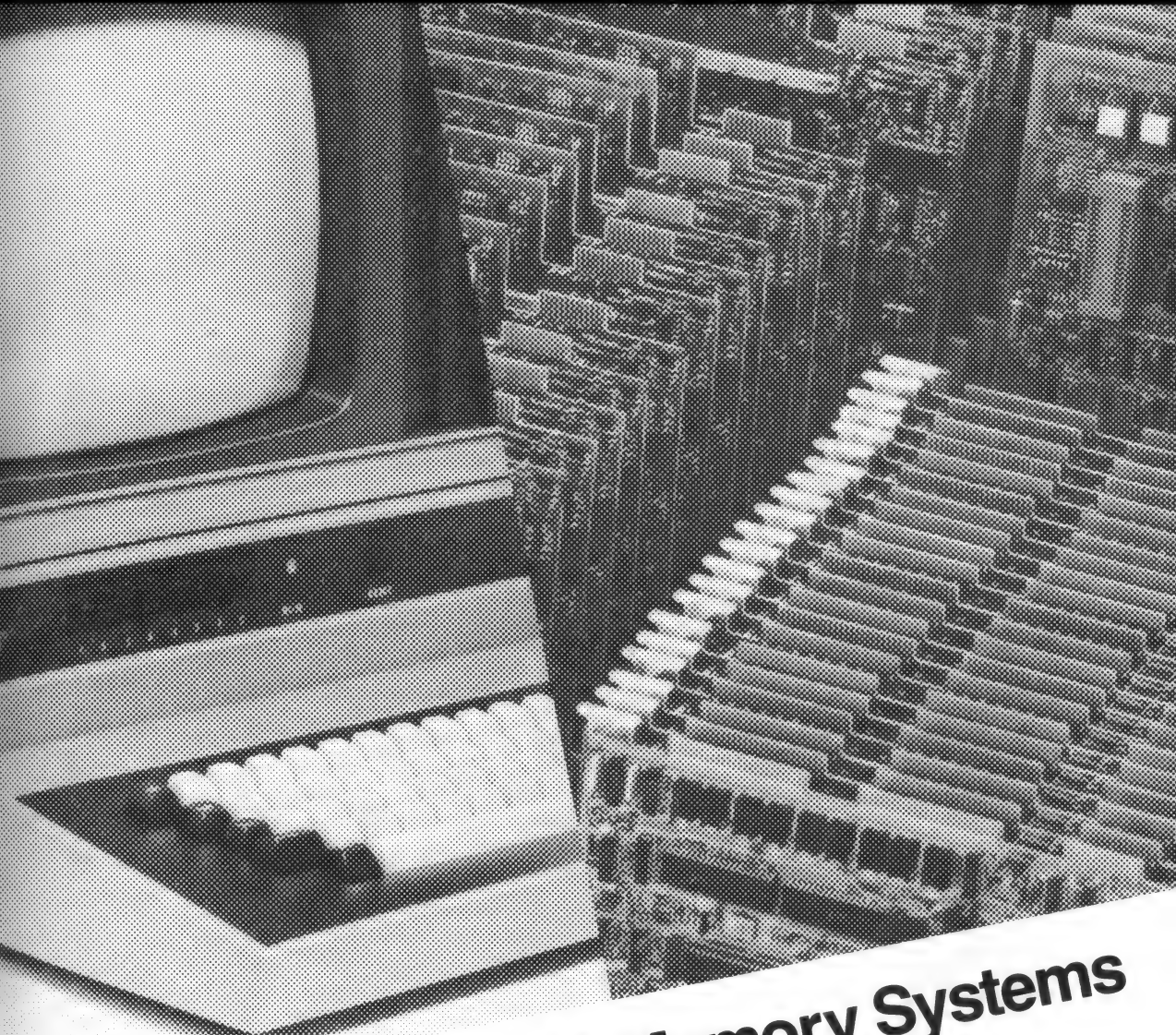
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3 Memory Systems

Memory Systems

Add-On/Add-In Memories

MEMORY SYSTEMS

INTRODUCTION

Intel's standard line of memory systems include OEM memory systems for use in general and special purpose applications, and add-on/add-in memory systems and cards for use with DEC* microcomputer and minicomputer systems. This section provides information on the standard in-40, in-1600, in-3000, and in-7000 general purpose memories, and the special purpose in-477 and in-5770 memories. The in-5770, a video refresh memory system providing 4-bit resolution to the picture elements of video images projected onto raster-scan CRT display terminals, is designed specifically for image-enhancement applications in conjunction with sophisticated, computer-driven medical, scientific, and laboratory applications such as X-rays. The DEC-compatible add-on/add-in memories include the in-1670, in-4011, in-4711, in-5004, and the in-5034, a single hex height card offering users of DEC PDP*-11/04 and 11/34 computers a high density 32K, 48K, or 64K \times 18-bit memory with built-in high reliability and low power consumption features. These standard products cover a wide range of applications, and because they use proven designs manufactured in volume, provide the most cost-effective solutions for most applications. However, in applications whose specialized requirements cannot be met with standard products, Intel designs and manufactures customized systems in exact conformance with user specifications.

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in-5034 PDP-11/04, 11/34 Add-In Memory Card	3-48

*DEC and PDP are registered trademarks of Digital Equipment Corporation.

STORAGE CAPACITY (BYTES)

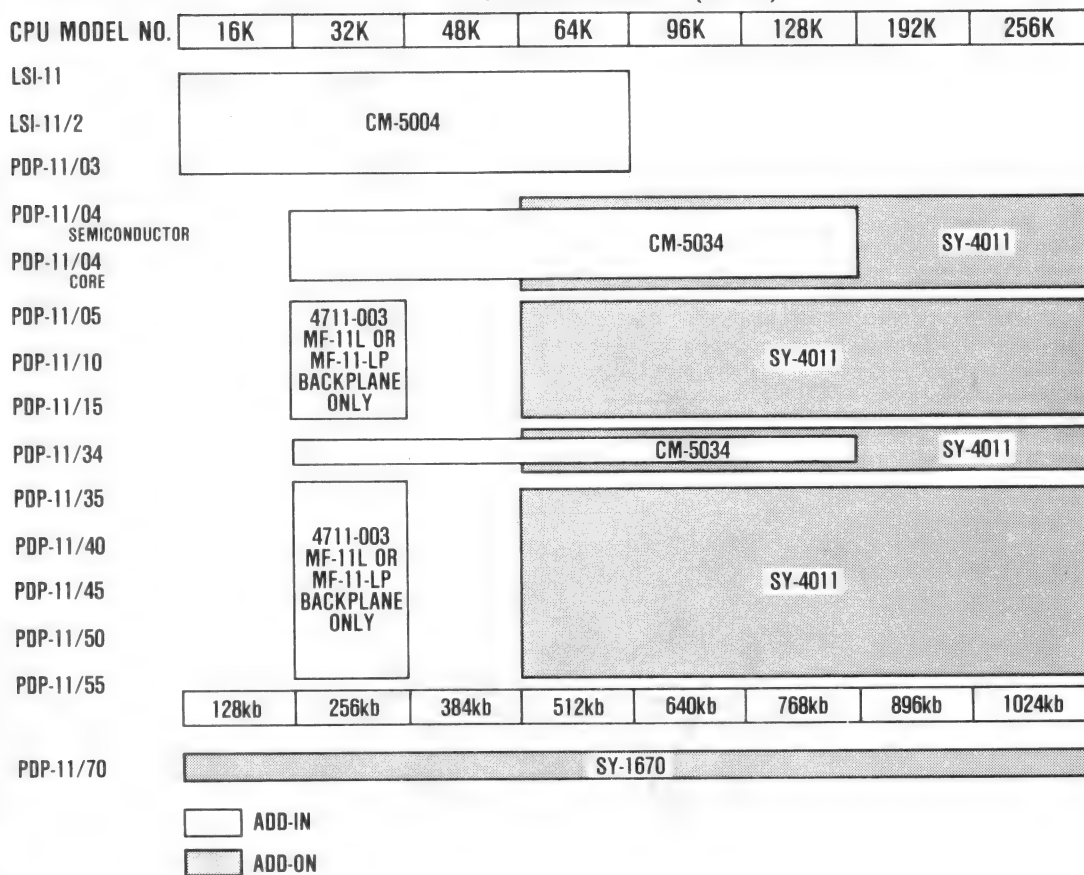


Figure 1. DEC-Compatible Product Selection Guide

in-40 DYNAMIC RAM MEMORY SYSTEM

64K words \times 16 bits per card basic modular capacity

Modular expandability

Two chassis options

- **7-inch minichassis capacity to 256K \times 9, 128K \times 18, or 64K \times 36**
- **10½-inch unichassis capacity to 768K \times 9, 384K \times 18, 256K \times 36, 128K \times 54, or 96K \times 72**

Dynamic MOS RAMs provide high density memory with low system cost

Address selection provides internal modular select capability

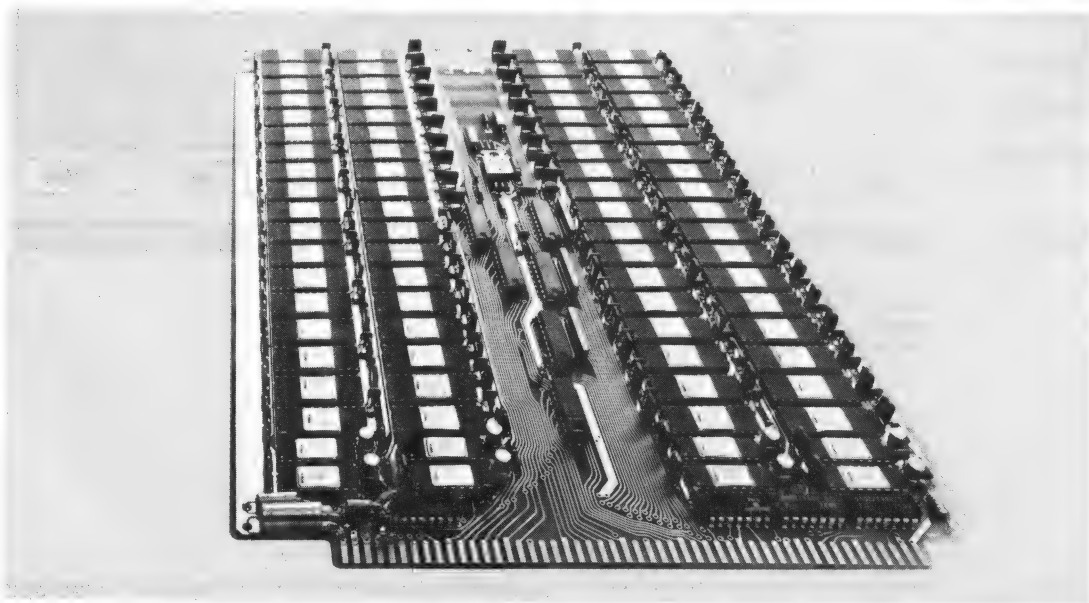
Word/byte data control option for varying word lengths

Address register provides time-shared addressing and write data functions

Automatic refresh and externally initiated refresh option

Fast cycle time

The Intel in-40 Dynamic RAM Memory System is a general purpose memory system available as a basic card set or mounted in either of two optional card chassis complete with connectors and back panel wiring. The basic card set system consists of three card types: memory cards (MUs), control cards (CUs), and optional buffer cards (BUs). A single control card is capable of addressing 128K words \times 18 bits or 256K words \times 9 bits, and drives up to eight memory cards. Module selection is done internally within the system. The system's basic modular capacity of 16K \times 18 or 32K words \times 9 bits per card set may be expanded to 128K \times 18 or 256K \times 9 by adding memory cards, and beyond the basic 128K-word capacity by using buffer cards. Each buffer card functions as a secondary control card, and drives up to eight memory cards. Using the optional 7-inch minichassis provides a total capacity of up to 256K \times 9, 128K \times 18, or 64K \times 36, including power. The 10½-inch unichassis provides a total capacity of up to 768K \times 9, 384K \times 18, 128K \times 54, or 96K \times 72.



FUNCTIONAL DESCRIPTION

The in-40 is a semiconductor memory system designed to provide a basic $16K \times 18$ bits (or $32K \times 9$) of memory per card set, expandable to $128K \times 18$ bits ($256K \times 9$) with additional memory cards. The basic in-40 system is available as a card set or mounted in a card chassis with connectors and back panel wiring. A single control card is capable of addressing $128K \times 18$ bits or $256K \times 9$ bits of memory. Module selection is done internally within the memory system. Block diagrams of the in-40 system featuring word lengths of less than nine bits and more than nine bits are shown in Figure 1.

System Components

The in-40 memory system consists of three basic printed circuit cards for memory storage, control, and buffering, all housed in either of two optional card chassis with connectors and back panel wiring (see Chassis Options). The typical $128K \times 18$ -bit (or $256K \times 9$ -bit) configuration consists of eight memory cards and one control card, housed in a 7-inch chassis. Multiple $128K$ in-40 systems provide extended storage capacity, and require the buffer card for buffering and multiple addressing. The three cards function as follows:

Memory Card — The MU-40 memory card, which provides the basic $16K$ -word \times 18 -bit storage units for the in-40 memory system, is a printed circuit card assembly containing a total of 72 2107C memory chips, along with clock drivers, sense amplifiers, address decoding circuitry, an address buffer and loader, write enable buffers, and a high speed inverter and data latch for incoming data.

Control Card — The CU-40 control card, which serves as the control unit for the in-40 memory system, contains the data and address registers, all control generation logic, response and timing signals, and priority circuitry. The control card receives interface signals and address inputs from the processor, generates the internal control signals required by the system, and checks address parity. Additionally, the control card decodes address inputs for memory selection, controls memory interleaving between two identical memory systems, controls cycle priority and initiation, generates mode signals, generates control card timing signals, provides inhibit circuitry, controls the clear memory functions, controls the data save function, and controls the system reset. A single CU-40 controls up to eight MU-40 memory cards.

Buffer Card — The BU-40 buffer card is used when the system is expanded beyond the eight memory card maximum. The buffer card functions as a secondary control card, and is used to multiplex address and data inputs and to buffer data and control inputs. A single BU-40 buffer card controls up to eight memory unit cards.

Chassis Options

To accommodate a wide range of memory capacities, Intel offers a number of chassis options, available as standard equipment. The in-40 system, whose outer dimensions and card outline are shown in Figure 2, may be mounted in either of the two optional chassis.

Minichassis — The 7-inch HC-40 memory chassis (see Figure 3) is designed to accommodate up to 11 memory cards, mounted horizontally with space for one control card and one interface card. The chassis is mounted on

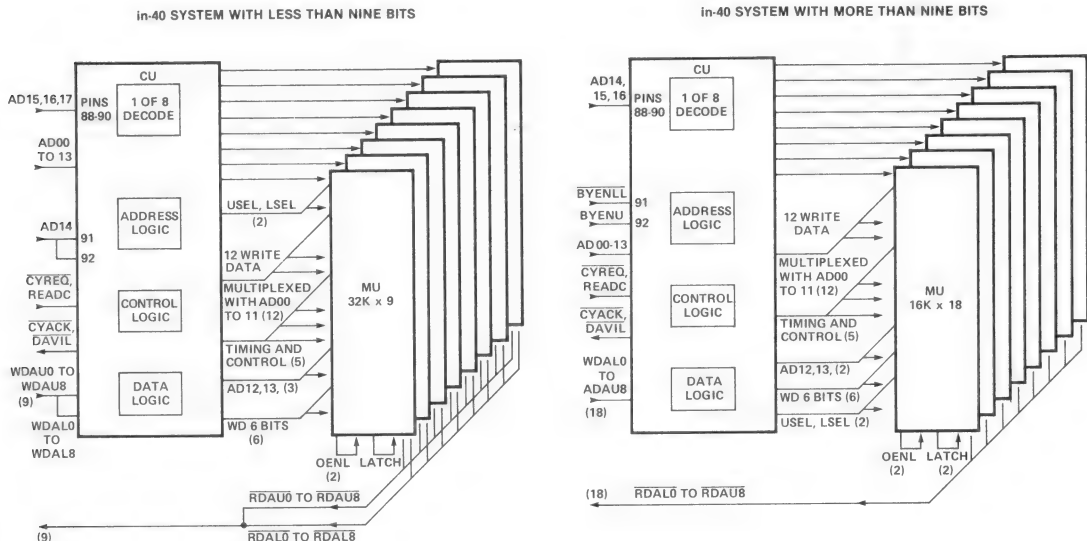


Figure 1. in-40 System Block Diagram Featuring Word Lengths of Less Than or More Than Nine Bits

slides for easy movement in and out, and may be mounted in a 19-inch relay rack. All connections are made from the rear of the unit. The unit features a front panel circuit breaker and power indicator light, and the use of an unwired backplane for all power and ground connections. The minichassis power supply, included in the unit, provides for all in-40 systems included in the unit.

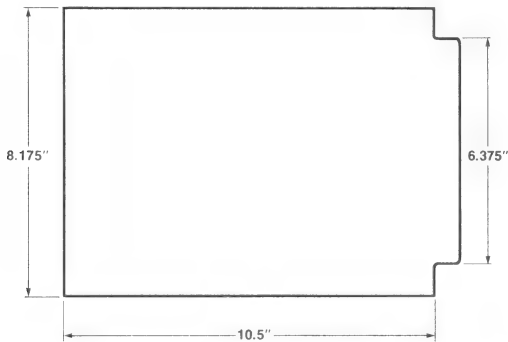


Figure 2. in-40 System Card Dimensions

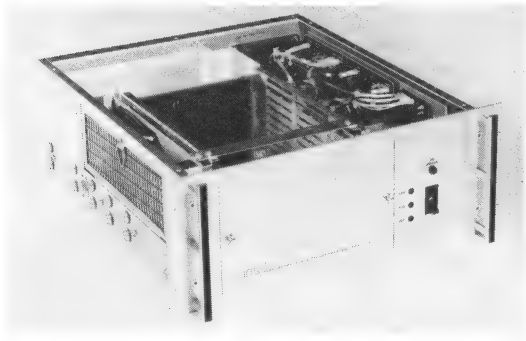


Figure 3. HC-40 Minichassis

Unichassis — The 10½-inch VC-40 unichassis (see Figure 4) is a vertical mount cardcage designed to accommodate up to 33 in-40 memory and control cards for mounting in a standard 19-inch relay rack. The chassis may be wired for a number of memory sizes and configurations, and may also be used in multiple arrangements for even larger memory configurations. The unichassis features the use of a full PC backplane with provisions to accept individual I/O cable wiring or DIP-socket flat cable connections.

Operation

The in-40 operates in read, write, data save, and refresh modes, with provisions for an optional read-modify-

write operation. Several refresh options are available, including externally initiated refresh.

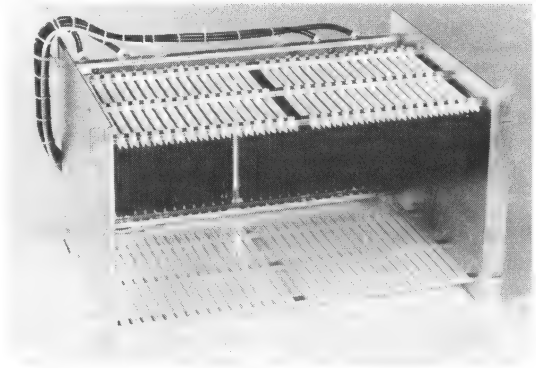


Figure 4. VC-40 Unichassis Unit

Interface

Inputs/Outputs — All input/output signals required by the in-40 are compatible with TTL integrated circuits. These inputs and outputs are summarized in Tables 1 and 2, respectively.

Signal	Operation
Cycle request	Initiates memory cycles upon going low in conjunction with read control signal. Ignored during refresh operations.
Read control	Controls selection of read or write operation. Initiates read cycle when low, write cycle when high, both in conjunction with cycle request signal. Ignored during refresh operation.
Address (0-17)	Controls address selection for internal chip addressing, card row addressing, card select addressing, and module interleaving in 18 address inputs supplied by processor.
Write data (0-17)	Enables write operation when low with read control signal held high. Inhibits all read operation signals.
Byte enable upper, byte enable lower	Enables byte operation on either or both bytes of data word. Enables read or write operation in upper byte when byte enable upper signal goes high. Enables read or write operation in lower byte when byte enable lower signal goes low. Initiates both bytes in systems requiring full word operation, with byte enable input signals tied to form one line.

Table 1. in-40 Input Signal Operations

Signal	Operation
Cycle acknowledge	Indicates (when returned to processor) memory cycle initiation by cycle request input signal. Remains low throughout memory cycle. Not generated during refresh operation.
Data available	Indicates (when returned to processor during read operations) availability of read data on output lines. Used by processor to strobe read data.
Read data (0-17)	Controls data transfer on 18 bidirectional lines between PDP-11 processor and in-40 memory. Bits 0-7 carry data on lower bytes, bits 8-17 on upper byte.

Table 2. in-40 Output Signal Operations

SPECIFICATIONS

Storage Capacity

4K, 8K, 16K, or 32K words per card, expandable to 128K \times 18 or 256K \times 9

Word Length

8, 9, 10, 12, 16, or 18 bits per memory card. Longer words are made by combining memory cards.

Performance

Cycle Time — 550 ns max

Access Time — 400 ns max

Retention Time — 2 ns max

Operational Modes

Read (NDR0)

Write

Data save

Refresh

Read-modify-write

Interface Characteristics

Interface — TTL compatible

Address Input — 12-18 binary lines (single ended)

Data Input — Up to 18 lines (single ended)

Data Output — Up to 18 lines (single ended)

Control Input — 4 lines: cycle request, read/write, byte enable 1 and 2 (single ended)

Control Output — 2 lines: cycle acknowledge, data available (single ended)

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring users of products with proven quality and reliability. In addition, all Intel memory systems products are covered by a one-year Intel warranty.

Interface Signals

Input

Low: -1.0 to $+0.7V @ \leq 2$ mA

High: $+2.2$ to $+5.5V @ \leq 100 \mu A$

Output

Low: -0.5 to $+0.5V @ \leq 16$ mA

High: $+2.4$ to $+5.25V @ \leq 200 \mu A$

Note

TTL levels all inputs and outputs

Physical Characteristics

Card

Width: 10.5 in. (26.67 cm)

Height: 8.175 in. (20.76 cm)

Depth: 0.45 in. (1.15 cm)

Weight: Less than 1.0 lb (0.46 kg)

Minichassis

Width: 19 in. (48.26 cm)

Height: 7 in. (17.78 cm)

Depth: 17 in. (43.18 cm)

Weight: Less than 70 lb (154 kg)

Unichassis

Width: 19 in. (48.26 cm)

Height: 10.5 in. (26.67 cm)

Depth: 12.5 in. (31.75 cm)

Weight: Less than 70 lb (154 kg)

Electrical Characteristics**MU-40 DC Power Requirements**

Selected		
Voltage	Current (max)	Regulation (%)
V _{DD} + 12.0V	1.3A	± 5
V _{CC1} + 5.0V	0.35A	± 5
V _{CC2} + 5.0V	0.65A	± 5
V _{BB} - 5.0V	<10.0 mA	± 5
Unselected		
Voltage	Current (max)	Regulation (%)
V _{DD} + 12.0V	0.20A	± 5
V _{CC1} + 5.0V	0.35A	± 5
V _{CC2} + 5.0V	0.65A	± 5
V _{BB} - 5.0V	<10.0 mA	± 5

CU-40 DC Power Requirements

Voltage	Current (max)	Regulation (%)
V _{CC1} + 5.0V	2.00A	± 5
*V _{CC2} + 5.0V	0.55A	± 5
V _{BB} - 5.0V	0.30A	± 5

* <1.0 mA during data save

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, - 40°C to + 85°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-40-000 — in-40 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
MU-40-608	8K × 16	Memory card with cycle and access times of 500 ns and 350 ns, respectively
MU-40-616	16K × 16	Same as above except capacity
MU-40-808	8K × 18	Same as above except capacity
MU-40-816	16K × 18	Same as above except capacity
MU-42-608	8K × 16	Memory card with cycle and access times of 550 ns and 400 ns, respectively
MU-42-616	16K × 16	Same as above except capacity
MU-42-808	8K × 18	Same as above except capacity
MU-42-816	16K × 18	Same as above except capacity
CU-40	—	Control card to operate up to eight MU-40 cards
CU-42	—	Control card to operate up to eight MU-42 cards
BU-40	—	Buffer card for use with MU-40 and CU-42
BU-42	—	Buffer card for use with MU-42 and CU-42
HC-40	—	Minichassis to hold up to 11 in-40 cards. Includes cooling fans, power supply, and unwired backplane.
VC-40	—	Unichassis cardcage to hold up to 33 in-40 cards. Includes unwired backplane.



in-1600 Dynamic RAM Memory System

64K words × 18 bits or 128K words × 9 bits per card basic modular capacity

Modular expandability

Design versatility with variety of system configurations

Two chassis options

- **7-inch minichassis capacity to 1024K × 9, 512K × 18, or 256K × 36**
- **10½-inch unichassis capacity to 3072K × 9, 1536K × 18, 1024K × 36, 512K × 54, or 384K × 72**

Dynamic MOS RAMs for high density memory with low system cost

Flexible addressing and control functions

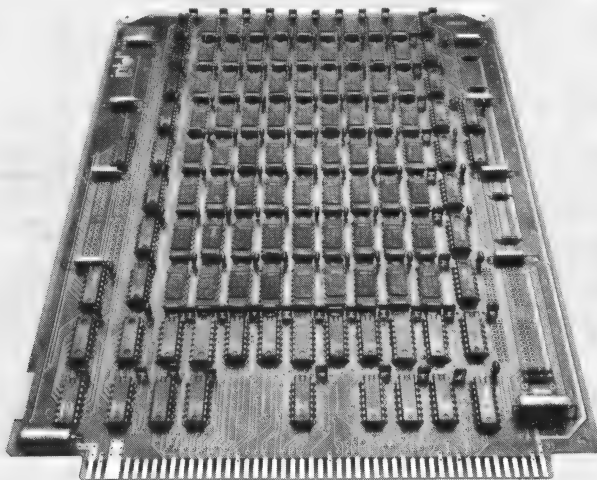
Address selection provides internal modular select capability

Word/byte data control option for varying word lengths

Automatic refresh and externally initiated refresh option

Fast cycle time

The Intel in-1600 Dynamic RAM Memory System is a general purpose memory system available as a basic card set or mounted in either of two optional card chassis complete with connectors and back panel wiring. The basic card set consists of three card types: memory cards (MUs), control cards (CUs), and buffer cards (BUs). These may be arranged in a variety of system configurations, providing great versatility in system design. A single control card is capable of addressing 512K words × 18 bits or 1024K words × 9 bits, and drives up to eight memory card modules. Module selection is done internally within the system. The system's basic modular capacity of 64K × 18 or 128K words × 9 bits per card may be expanded to 512K × 18 or 1024K × 9 by adding memory cards, and beyond this maximum 512K-word capacity by using buffer cards. Each buffer card functions as a secondary control card, and drives up to eight memory cards. Output buffer cards are used only where required to buffer output data from the memory and drive it onto the data bus. Using the optional 7-inch minichassis provides a total capacity of up to 1024K × 9, 512K × 18, or 256K × 36, including power. The 10½-inch unichassis provides a total capacity of up to 3072 × 9, 1536K × 18, 1024K × 36, 512K × 54, or 384K × 72.



FUNCTIONAL DESCRIPTION

The in-1600 is a semiconductor memory system designed to provide a basic storage capacity of $64K \times 18$ bits (or $128K \times 9$) of memory per card set, expandable to $512K \times 18$ ($1024K \times 9$) with additional memory cards. The basic in-1600 system is available as a card set or mounted in a card chassis with connectors and back power wiring. A single control card is capable of addressing $512K$ words \times 18 bits or $1024K$ words \times 9 bits of memory. As shown in Table 1, the system is available in a variety of configurations, with or without optional buffer cards. Module selection is done internally within the memory system. Simplified block diagrams of the in-1600 system in $512K \times 18$ and $512K \times 36$ configurations are shown in Figure 1.

System Components

The in-1600 memory system consists of four basic printed circuit cards for memory storage, control, buffering, and output buffer support, all housed in either of two optional control card chassis complete with connectors and back panel wiring (see Chassis Options). Multiple in-1600 systems provide extended storage capacity, and require buffer cards for buffering and multiple addressing. The four cards function as follows:

Memory Card — The MU-160 memory card, which provides the basic $64K$ -word \times 18 -bit storage units for the in-1600 memory system, is a printed circuit card assembly containing memory chips, along with clock drivers, address decoding circuitry, mode circuitry, memory chip address circuitry, read data output drivers, high speed latches and inverters for incoming write data, and jumpers for partially populated memory cards.

Bits	Words				
	32K	64K	128K	256K	512K
8	1CU 1MU — $32K \times 16$ — 1	1CU 1MU — $64K \times 16$ — 1	1CU 2MU — $64K \times 16$ — 1	1CU 4MU — $64K \times 16$ — 2	1CU 8MU — $64K \times 16$ — 2
9	1CU 1MU — $32K \times 18$ — 1	1CU 1MU — $64K \times 18$ — 1	1CU 2MU — $64K \times 18$ — 1	1CU 4MU — $64K \times 18$ — 2	1CU 8MU — $64K \times 18$ — 2
12	1CU 1MU — $32K \times 12$ — 1	1CU 1MU — $64K \times 12$ — 1	1CU 2MU — $64K \times 12$ — 1	1CU 4MU — $64K \times 12$ — 2	1CU 8MU — $64K \times 12$ — 2
16	1CU 1MU — $32K \times 16$ — 1	1CU 1MU — $64K \times 16$ — 1	1CU 2MU — $64K \times 16$ — 1	1CU 4MU — $64K \times 16$ — 2	1CU 8MU — $64K \times 16$ — 2
18	1CU 1MU — $32K \times 18$ — 1	1CU 1MU — $64K \times 18$ — 1	1CU 2MU — $64K \times 18$ — 1	1CU 4MU — $64K \times 18$ — 2	1CU 8MU — $64K \times 18$ — 2
24	1CU + 1BU 2MU — $32K \times 12$ — 2	1CU + 1BU 2MU — $64K \times 12$ — 2	1CU + 1BU 4MU — $64K \times 12$ — 2	1CU + 1BU 8MU — $64K \times 12$ — 3	1CU + 2BU 16MU — $64K \times 12$ — 3
32	1CU + 1BU 2MU — $32K \times 16$ — 2	1CU + 1BU 2MU — $64K \times 16$ — 2	1CU + 1BU 4MU — $64K \times 16$ — 2	1CU + 1BU 8MU — $64K \times 16$ — 3	1CU + 2BU 16MU — $64K \times 16$ — 3
36	1CU + 1BU 2MU — $32K \times 18$ — 2	1CU + 1BU 2MU — $64K \times 18$ — 2	1CU + 1BU 4MU — $64K \times 18$ — 2	1CU + 1BU 8MU — $64K \times 18$ — 3	1CU + 2BU 16MU — $64K \times 18$ — 3
48	1CU + 2BU 3MU — $32K \times 16$ — 2	1CU + 2BU 3MU — $64K \times 16$ — 2	1CU + 2BU 6MU — $64K \times 16$ — 3	1CU + 2BU 12MU — $64K \times 16$ — 4	1CU + 2BU 24MU — $64K \times 16$ — 4
64	1CU + 3BU 4MU — $32K \times 16$ — 2	1CU + 3BU 4MU — $64K \times 16$ — 2	1CU + 3BU 8MU — $64K \times 16$ — 3	1CU + 3BU 16MU — $64K \times 16$ — 4	[3]
72	1CU + 3BU 4MU — $32K \times 18$ — 2	1CU + 3BU 4MU — $64K \times 18$ — 2	1CU + 3BU 8MU — $64K \times 18$ — 3	1CU + 3BU 16MU — $64K \times 18$ — 4	[3]

□ Unichassis
■ HMS = Horizontal minichassis, including power supplies and cooling.

Notes

1. Board count/configuration
2. Dash number of required in-LPS power supply
3. Contact factory

Table 1. in-1600 Memory System Configuration Chart

Control Card — The CU-160 control card, which serves as the control unit for the in-1600 memory system, receives control inputs from the processor, generates all timing and control signals required by the system, and controls and routes address inputs and write data to the memory cards or buffer cards, as required. The CU-160 contains all the address and logic circuitry required to operate the in-1600 system, including data

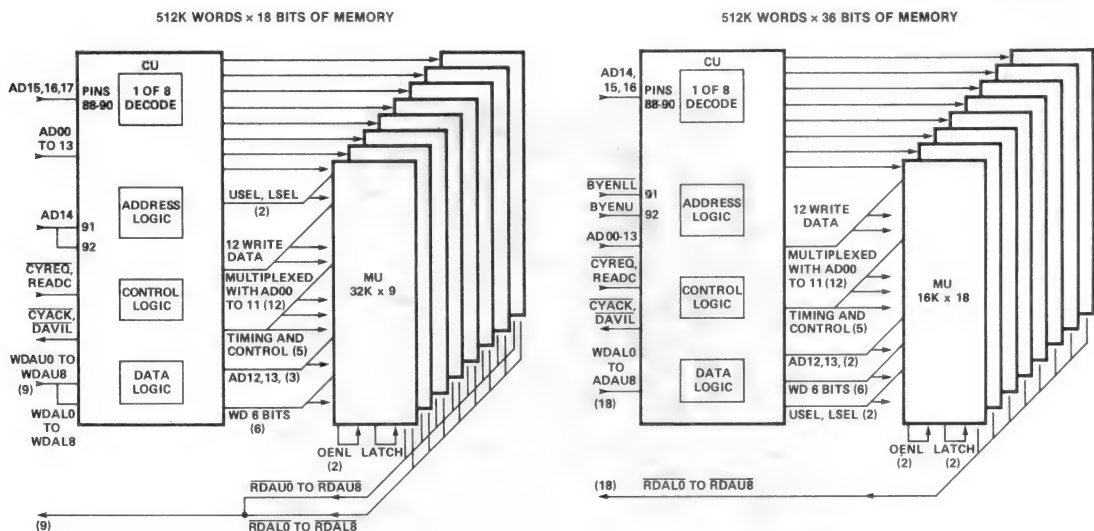


Figure 1. in-1600 System Block Diagrams Featuring Systems With Either 18 or 36 Bits of Memory

and address registers, all control generation logic, response and timing signals, and priority (arbitration) circuitry. One CU-160 controls up to eight MU-160 memory cards.

Buffer Card — The BU-160 buffer card is used either when the system is expanded beyond the eight memory card maximum, or when the word length is extended beyond 18 bits. The buffer card functions as a secondary control card, and is used to multiplex address and data inputs and to buffer data and control inputs. A single BU-160 buffer card controls up to eight memory cards.

Chassis Options

To accommodate a wide range of memory capacities, Intel offers a number of chassis options, available as standard equipment. The in-1600 system whose outer dimensions and card outline are shown in Figure 2, may be mounted in either of the two optional chassis.

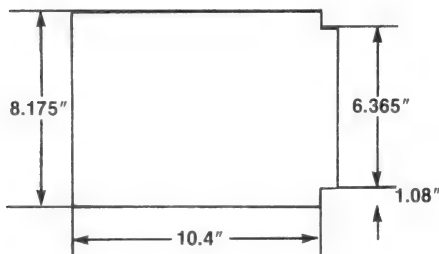


Figure 2. in-1600 System Card Dimensions

Minichassis — The 7-inch HC-1600 memory chassis (see Figure 3) is designed to accommodate up to 11 MU-1600 cards, mounted horizontally. The chassis is mounted on slides for easy movement in and out, and may be mounted in a 19-inch relay rack. All connections are made from the rear of the unit. The unit features a front panel circuit breaker and power indicator light, and the use of an unwired backplane for all power and ground connections. The minichassis power supply, included in the unit, provides power for all in-1600 systems.

Unichassis — The 10½-inch VC-40 unichassis (see Figure 4) is a vertical mount cardcage designed to accommodate up to 33 in-1600 printed circuit cards for mounting in a standard 19-inch relay rack. The chassis may be wired for a number of memory sizes and configurations (e.g., 128K × 96 or 256K × 48 with 32 cards), and may also be used in multiple arrangements for even larger memory configurations. The unichassis features the use of a full PC backplane with provisions to accept individual I/O cable wiring or DIP-socket flat cable connectors.

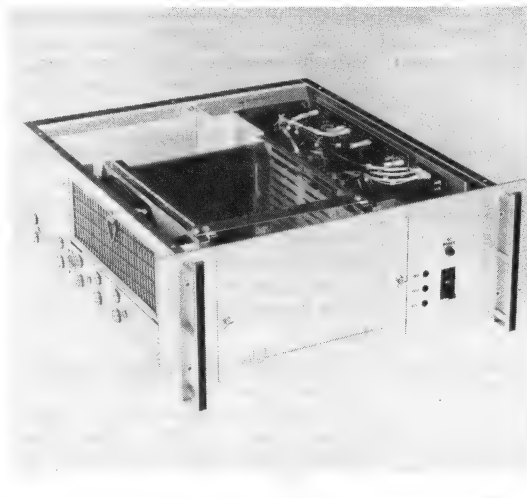


Figure 3. HC-1600 Minichassis Unit

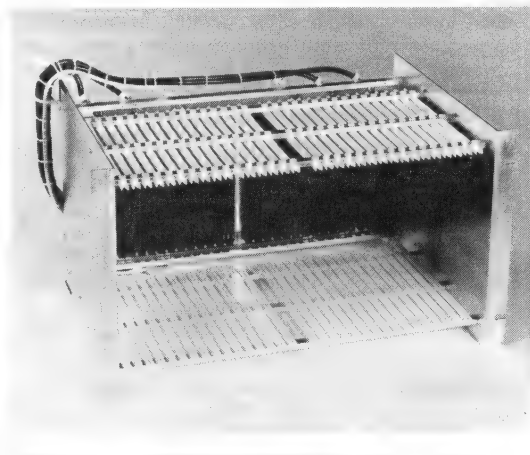


Figure 4. VC-40 Unichassis Unit

Operation

The in-1600 operates in read, write, read-modify-write, and refresh modes. These standard operations may be performed either on a full data or on half a data word (byte).

Interface

Input/Output — All input/output signals required by the in-1600 are compatible with TTL integrated circuits. These input and output signal operations are summarized in Tables 2 and 3, respectively.

Signal	Operation	Signal	Operation
Cycle request	Initiates memory cycle upon going low if no other memory cycle is in progress; if other cycle is in progress, initiates new cycle upon completion of cycle in progress if held low until new cycle starts.		in lower byte when byte enable lower signal goes low. Initiates both bytes in systems requiring full word operation, with byte enable upper tied high and byte enable lower tied low. Initiates single byte operation in systems with extended capacity and shorter word length, with both byte enable signals tied together to form one line to access upper byte when high, lower byte when low.
Read control	Controls selection of read or write operation. Initiates write cycle when high; if low at time of cycle initiation, system automatically goes into read cycle. Ignored during refresh operation.	Refresh go (optional)	Initiates refresh operation when sent to memory in response to refresh request output from memory. May be internally generated by memory when tied to refresh request signal.
Read-modify-write control	Enables read-modify-write mode during read operation (with cycle request and read control signals low), if driven low within 330 ns after cycle request. Initiates write portion of cycle (after data is modified) when driven high within 7.5 μ s after completion of read operation. Aborts cycle if processor fails to drive signal high during required period.	Address	Controls address selection for internal chip addressing, card row addressing, and memory module or buffer unit card select addressing in 19 address inputs supplied by the processor.
Byte enable upper, byte enable lower	Enables byte operation on either or both bytes of data word. Enables read or write operation in upper byte when byte enable upper signal goes high. Enables read or write operation	Write data	Controls write byte operation when both signals are low. Initiates write operation on upper byte when low, on lower byte when high.

Table 2. in-1600 Input Signal Operations

Signal	Operation
Cycle acknowledge	Indicates (when returned to processor) normal memory cycle initiation by cycle request input. Remains low throughout memory cycle. Not generated during refresh operation.
Data available	Indicates (when sent to processor during read operations) availability of read data on output lines. Used by processor to strobe read data.
Read data	Transfers read data from memory to processor via buffer unit card.
Refresh request	Requests refresh cycle when generated by refresh circuitry. Sent to processor (in externally controlled refresh operation) as request for refresh operation; processor responds by supplying refresh go signal. Not sent to processor (in internally controlled refresh operation); tied to refresh go input.

Table 3. in-1600 Output Signal Operations

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring users of products with proven quality and reliability. In addition, all Intel memory systems products are covered by a one year Intel warranty.

SPECIFICATIONS

Storage Capacity

16K, 32K, 64K, or 128K words per card, expandable to 1024K \times 18 or 2048K \times 9.

Word Length

8, 9, 10, 12, 16, or 18 bits per memory card. Longer words are made by combining memory cards.

Performance

Cycle Time — 500 ns max

Access Time — 330 ns max

Retention Time — 2 ns max

Operational Modes

Read (NDRO)

Write

Refresh

Interface Characteristics

Interface — TTL compatible

Address Input — 14-20 binary lines (single ended)

Data Input — Up to 18 lines (single ended)

Data Output — Up to 18 lines (single ended)

Control Input — 3 lines: cycle request, read/write, byte control (single ended).

Control Output — 3 lines: cycle acknowledge, memory busy, data available (single ended).

Interface Signals

Input

Low: -1.0 to $+0.5V @ \leq 2$ mA

High: $+2.0$ to $+5.5V @ \leq 100$ μ A

Output

Low: -0.5 to $+5.0V @ \leq 15$ mA

High: $+2.4$ to $5.25V @ \leq 200$ μ A

Physical Characteristics

Card

Width: 8.175 in. (20.76 cm)

Height: 10.80 in. (27.43 cm)

Depth: 0.450 in. (1.15 cm)

Weight: 1.0 lb (0.46 kg)

Minichassis

Width: 19 in. (48.26 cm)

Height: 7 in. (17.78 cm)

Depth: 17 in. (43.18 cm)

Weight: Less than 70 lb (154 kg)

Unichassis

Width: 19 in. (48.26 cm)

Height: 10.5 in. (26.67 cm)

Depth: 12.5 in. (31.75 cm)

Weight: Less than 70 lb (154 kg)

Electrical Characteristics

MU-1600 DC Power Requirements

Selected		
Voltage	Current (max)	Regulation (%)
$V_{DD} + 12.0V$	1.60A	± 5
$V_{CC1} + 5.0V$	2.00A	± 5
$V_{CC2} + 5.0V$	1.15A	± 5
$V_{BB} - 5.0V$	13.0 mA	± 5
Unselected		
Voltage	Current (max)	Regulation (%)
$V_{DD} + 12.0V$	0.26A	± 5
$V_{CC1} + 5.0V$	2.00A	± 5
$V_{CC2} + 5.0V$	1.15A	± 5
$V_{BB} - 5.0V$	13.0 mA	± 5

CU-160 DC Power Requirements

Voltage	Current (max)	Regulation (%)
$V_{CC1} + 5.0V$	3.55A	± 5
$V_{CC2} + 5.0V$	0.55A	± 5
$V_{BB} - 5.0V$	0.30A	± 5

Environmental Characteristics

Temperature — $0^{\circ}C$ to $50^{\circ}C$ operating ambient, $-40^{\circ}C$ to $+125^{\circ}C$ non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-1600-000 — in-1600 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
MU-160-232	32K × 12	Memory unit card with cycle and access times of 500 ns and 330 ns, respectively
MU-160-264	64K × 12	Same as above except capacity
MU-160-632	32K × 16	Same as above except capacity
MU-160-664	64K × 16	Same as above except capacity
MU-160-832	32K × 18	Same as above except capacity
MU-160-864	64K × 18	Same as above except capacity
CU-160	—	Control card to operate up to eight MU-160 memory cards
BU-160	—	Buffer card for use with MU-160 and CU-160 cards
HC-1600	—	Minichassis for up to 11 in-1600 cards. Includes cooling fans, power supply, and unwired backplane.
VC-40	—	Unichassis cardcage to hold up to 33 in-7000 cards. Includes unwired backplane.



in-3000 DYNAMIC RAM MEMORY SYSTEM

**Up to 64K words × 20 bits per card
storage capacity**

**Dynamic MOS RAMs for high density
memory with low system cost**

**Addressability to 1024K bytes with con-
figuration option control**

**Byte data control for flexible capacity
and addressability**

**Optional error checking and correction
of single-bit errors**

**Simplified refresh with external refresh
option in any mode**

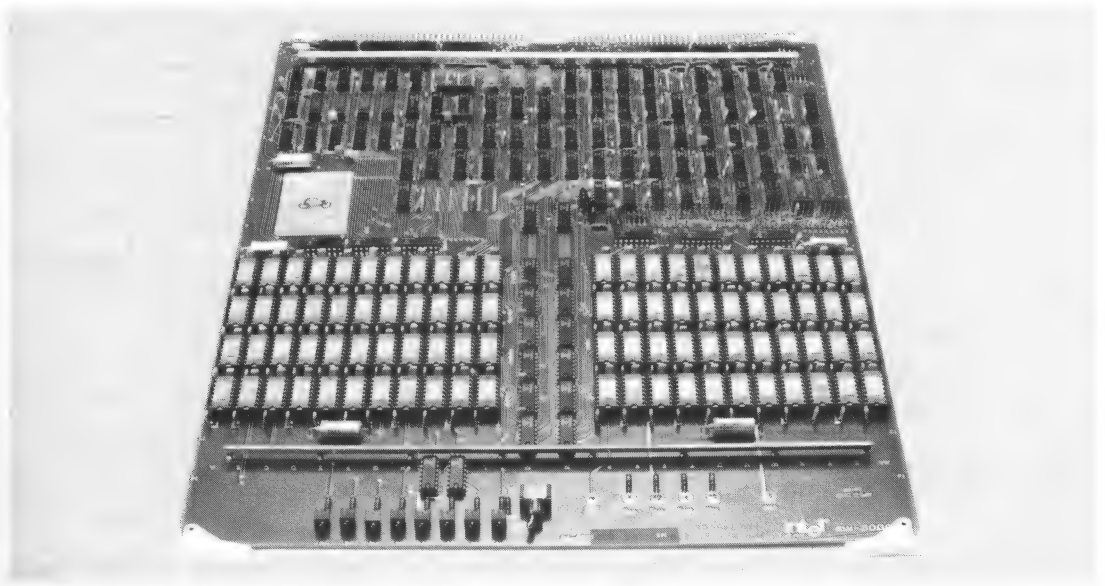
High speed cycle time: 450 ns max

All interfaces TTL compatible

Optional $\pm 15V$ operation

MEMORY
SYSTEMS

The Intel in-3000 Dynamic RAM Memory System is a complete general purpose dynamic memory with all required interface and control logic contained on a single printed circuit card measuring 11.75 × 15.4 inches. Standard configurations are 16K, 32K, or 64K words of 16, 18, or 20 bits per card. With the 16-bit configurations, an error checking and correction (ECC) option is also available. When the ECC option is specified, six check bits are added to the 16 data bits and stored as 22-bit words. The ECC automatically corrects all single bit errors and is transparent to the host system. The in-3000 simplifies system interface design with an exceptionally flexible addressing scheme. In the normal address mode 16 lines are used to select up to 64K words per card; however, a configuration option control input enables a 17th address line to provide up to 128K bytes per card, and additional inputs are provided to allow for system addressability up to 512K words (1024K bytes when the configuration option is selected). No external decoding is required. Each card slot in a multiple card system may be hardwired to respond to a given range of addresses, thus allowing all memory cards in a system to be identical and interchangeable. The in-3000 further simplifies interface design by incorporating a refresh scheme requiring only a single control line, which may be externally initiated in any mode (random, burst, etc.) capable of producing 128 refresh cycles per each two-millisecond period. The self-contained in-3000 is ideally suited for system applications requiring a simplified interface and a minimum number of spares. It is also the ideal choice for applications in which small blocks of memory are required to operate independently, such as systems in which interleaving is utilized to obtain a maximum data transfer rate.



FUNCTIONAL DESCRIPTION

The in-3000 semiconductor memory module consists of a single printed circuit card containing the memory storage area and all the logic and circuitry required for memory operation, including data circuitry, address circuitry, byte data control logic, timing logic, a provision for optional error correction circuitry (using the Hamming code technique to detect and correct single-bit errors), and the buffers and drivers necessary to present a TTL interface at the card connector. Block diagrams of both single-card and multiple-card system interface with the processor are shown in Figure 1.

Capacity

Each in-3000 memory card (CM-3000) provides a maximum storage capacity of 128K bytes per card, addressable as 16K, 32K, or 64K words with word lengths of 16, 18, or 20 bits per card. The maximum word length for a system using the error correction code is 16 bits at the interface. For longer word lengths or more capacity, additional cards are used.

Chassis Options

The in-3000 system, whose outer dimensions and card outline are shown in Figure 2, may be housed with a maximum of four in-3000 series memory cards in a horizontal mount chassis (HMS) providing a maximum storage capacity of 256K words \times 22 bits. The HMS chassis also accommodates a power supply, optional self-test card, and optional interface card with backplane wiring, and includes a front panel for mounting in a 19-inch RETMA equipment rack.

Addressability

Sixteen standard and three optional address inputs are available for addressing the in-3000 memory system. Their allocation is determined by the memory capacity

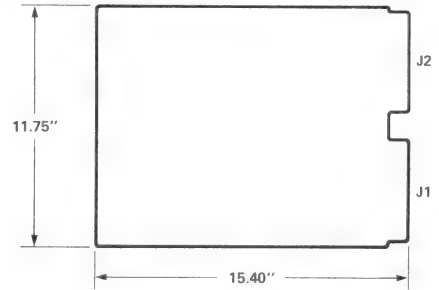


Figure 2. in-3000 System Card Outline and Dimensions

per card. To accommodate system expansion beyond a single memory module, the in-3000 includes a provision for three additional address inputs, which may be used for internal module select of one to eight memory modules. The memory select inputs are wired externally to predetermine the address selection of each memory card.

Byte Data Control — The two optional address inputs provided with the in-3000 system (column option COOP, address option ADOP) may be used to address bytes rather than words in the memory system. All 8K devices used on a single memory module must be of the same type (i.e., have the same portion of the chip functional, either upper or lower) to yield proper addressing. When the column option input is wired as shown in Table 2, and an address bit is supplied to the address option input, the memory system functions as either a 64K \times 22 or a 128K \times 11 bit system.

Operation

The in-3000 operates in read, write, read-modify-write, and refresh modes, with an optional error correction operation.

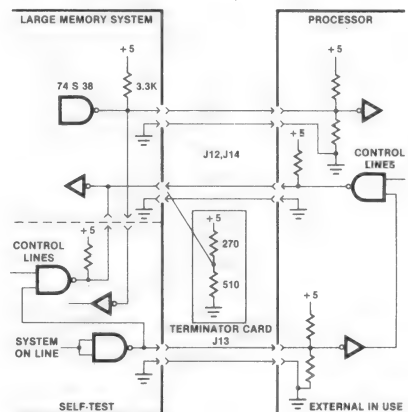
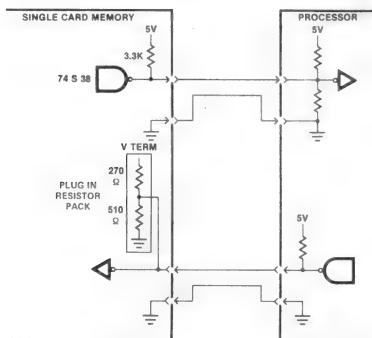


Figure 1. in-3000 Memory Unit to Processor Interface Diagrams

Input	Configuration	
	64K × 22 Bits	128K × 11 Bits
COOP J1-64	Logic "1" (open)	Logic "0" (0 volts)
ADOP J1-32	Don't care	Logic "0" selects lower byte; logic "1" selects upper byte

Table 2. Byte Data Control Address Option

Interface

All input and output signals required by the in-3000 are compatible with TTL integrated circuits. The in-3000 receives 15 inputs from the processor and returns three outputs. The input and output signal operations are summarized in Tables 3 and 4, respectively. All signals between the memory and the processor are carried on twisted pair transmission wire, as shown in Figure 1.

Signal	Operation	Signal	Operation
Request pulse	Initiates memory cycle upon going low, if memory is not busy (as indicated by memory busy output signal to processor held high).	Data out strobe option	Enables data output to pulse after cycle initiation from access time until termination of memory busy signal, when high. Enables data output and data available signal to remain valid after access time until subsequent receipt of new cycle request signal or of refresh initiate signal, when low. Must not be switched during memory cycle.
Byte control (1, 2)	Enables write operation in addressed byte when low. Enables read operation when high.	Refresh initiate	Initiates refresh cycle upon going low, if memory is not busy. Must not occur simultaneously with cycle request signal. Must occur a minimum of 128 times within each 2 ms period.
Split cycle	Initiates read-modify-write operation when low. Enables read portion of read-modify-write cycle.	Write data (0-19)	Controls data transfer on 20 bidirectional lines between processor and memory. On split cycle, data must be valid within 20 ns after leading edge of write signal and remain valid until 120 ns after leading edge. Input and output lines may be tied together at interface to form bidirectional data bus. During byte operations, byte 1 is defined as bits 0-7, 16, and 18; byte 2 as bits 8-15, 17, and 19.
Write pulse	Initiates write operation of read-modify-write operation if driven low within 5 μ s after cycle request.	Data option	Specifies, when high, that write data must be valid within 50 ns period after cycle initiation. Specifies, when low, that write data must become valid within 150 ns after leading edge of cycle initiation and must remain valid until 200 ns after leading edge.
Address (0-16)	Controls address selection on 17 single-ended inputs lines from processor to memory.	ECC disable	Disables decoders, when low, to prevent ECC logic from modifying read data.
Extended address	Controls memory card selection, in multiple card systems.		
Memory select (1, 2, 3)	Selects memory module, in conjunction with extended address bits. Used to select single board from up to eight available in fully expanded in-3000 memory system.		
Address option	Enables memory to function as byte-addressed board, when held high; i.e., 12K × 10 rather than 64K × 20.		
Address max	Enables, in conjunction with address option input, memory to function as byte-addressed board, when supplied with additional address input.		
General reset	Resets registers in memory, initializes timing circuits, and resets eight LED (light-emitting-diode) indicators of ECC (error correction code) logic, when high.		

Table 3. in-3000 Input Signal Operations

Signal	Operation
Memory busy	Indicates to processor, when low, that system is performing memory cycle. Prevents activation of cycle request signal or refresh initiate signal.
Data available	Indicates availability of data on output lines, when low. Occurs within specified access time after cycle initiation. Remains active as long as read data is valid.
Multiple bit error	Indicates to processor, when low, that uncorrectable error exists in read data (i.e., more than one bit is in error). Is valid at time of data available signal.

Table 4. in-3000 Output Signal Operations

SPECIFICATIONS

Storage Capacity

64K words \times 20 bits per card, expandable by using multiple card systems.

Word Length

16, 18, or 20 bits per card, expandable by using multiple card systems; 16 bits maximum with optional ECC.

Performance

Cycle Time

Read or Write Cycle: 450 ns max

Read-Modify-Write Cycle: 725 ns plus modify time without ECC; 775 ns plus modify time with optional ECC.

Access Time — 275 ns max without ECC; 325 ns max with optional ECC

Retention Time — 2 ms max

Operational Modes

Read (NDRO)

Write

Read-modify-write

Refresh

Interface Characteristics

Connectors — Two 80-pin double-sided PC edge, 0.125-in. centers

Interface — TTL compatible

Address Input — 17 binary lines (single ended)

Extended Address — 6 lines (3 input, 3 output) single ended

Memory Select — 3 lines (single ended)

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring users of products with proven quality and reliability. In addition, all Intel memory systems products are covered by a one-year Intel warranty.

Data Input — Up to 20 lines (single ended)

Data Output — Up to 20 lines (single ended)

Control Input — 12 lines: request pulse, byte control 1 and 2, split cycle, write pulse, address option, general reset 1 and 2, data out strobe option, refresh initiate, write data, data option, ECC disable (single ended)

Control Output — 3 lines: memory busy, data available, multiple bit error (single ended)

Physical Characteristics

Width: 11.75 in. (29.85 cm)

Height: 15.40 in. (39.12 cm)

Depth: 0.450 in. (1.15 cm)

Weight: Less than 2.0 lb (0.9 kg)

Mounting Centers: 0.625 in. (1.56 cm)

Electrical Characteristics

DC Power Requirements

Normal Voltages ($\pm 5\%$)	Standby Current (max)	Operating Current (max)
+ 12V DC	0.3A	1.7A
+ 5V DC	6.0A	6.0A
- 5V DC	0.08A	0.08A
Optional Voltages ($\pm 5\%$)	Standby Current (max)	Operating Current (max)
+ 15V DC	0.4A	1.0A
+ 5V DC	3.2A (5.0A) ¹	3.2A (5.0A) ¹
+ 15V DC	0.02A	0.02A
Termination Resistors ($\pm 5\%$)	All Inputs High	All Inputs Low
+ 5V DC (+ V term)	0.30A	0.75A

Notes

1. ECC option.

2. Sequencing requires -5V on before +12V (and -15V before +15V) and off reverse sequence.

3. The power supply provided with each in-3000 system allows 5A at +5V for the interface card.

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, -40°C to +125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Optional Versions

Option-001 — ECC

Option-003 — $\pm 15V$

Option-004 — With termination on-board

Option-005 — Extender card

Option-006 — Power supply

Option-007 — Self-test card

Option-008 — Custom interface card

Optional Equipment

EX-3000 Extender Board — Multiplayer printed circuit board used for maintenance purposes; compatible with CM-3000.

UT-3000 — Double-sided printed circuit board with provisions for mounting IC's, flat cable sockets, and other components. Customer logic and special interfaces can be assembled using the UT-3000, whose physical dimensions and edge connector layout are identical to the CM-3000 memory card.

Reference Manuals

TM-3000-000 — in-3000 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-3016-016	16K \times 16	Self-contained memory system card with cycle and access times of 450 ns and 275 ns, respectively
CM-3016-018	16K \times 18	Same as above except capacity
CM-3016-020	16K \times 20	Same as above except capacity
CM-3016-022	16K \times 16	Same as CM-3016-016 plus ECC (325 ns access time)
CM-3032-016	32K \times 16	Self-contained memory system card with cycle and access times of 450 ns and 275 ns, respectively
CM-3032-018	32K \times 18	Same as above except capacity
CM-3032-020	32K \times 20	Same as above except capacity
CM-3032-022	32K \times 16	Same as CM-3032-016 plus ECC (325 ns access time)
CM-3064-016	64K \times 16	Self-contained memory system card with cycle and access times of 450 ns and 275 ns, respectively
CM-3064-018	64K \times 18	Same as above except capacity
CM-3064-020	64K \times 20	Same as above except capacity
CM-3064-022	64K \times 16	Same as CM-3064-016 plus ECC (325 ns access time)
CM-3016-116	16K \times 16	Same as CM-3016-016 plus $\pm 15V$ power option
CM-3016-118	16K \times 18	Same as CM-3016-018 plus $\pm 15V$ power option
CM-3016-120	16K \times 20	Same as CM-3016-020 plus $\pm 15V$ power option
CM-3016-122	16K \times 16	Same as CM-3016-022 plus $\pm 15V$ power option
CM-3032-116	32K \times 16	Same as CM-3032-016 plus $\pm 15V$ power option
CM-3032-118	32K \times 18	Same as CM-3032-018 plus $\pm 15V$ power option
CM-3032-120	32K \times 20	Same as CM-3032-020 plus $\pm 15V$ power option
CM-3032-122	32K \times 16	Same as CM-3032-022 plus $\pm 15V$ power option
CM-3064-116	64K \times 16	Same as CM-3064-016 plus $\pm 15V$ power option
CM-3064-118	64K \times 18	Same as CM-3064-018 plus $\pm 15V$ power option
CM-3064-120	64K \times 20	Same as CM-3064-020 plus $\pm 15V$ power option
CM-3064-122	64K \times 16	Same as CM-3064-022 plus $\pm 15V$ power option



in-7000 STATIC RAM MEMORY SYSTEM

MEMORY
SYSTEMS

Up to 16K words \times 24 bits per card storage capacity

1K \times 4 static MOS RAMs

Addressability to 768K bytes

Word/byte data control options for flexible storage capacity and addressability

Three-state outputs

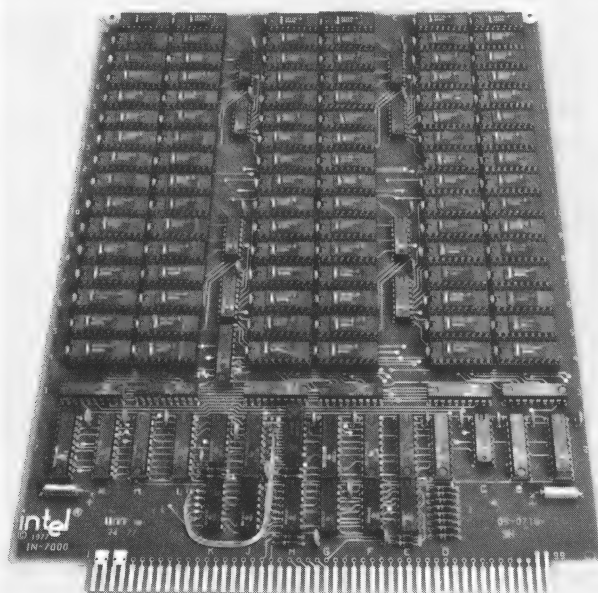
Fast cycle and access times: 250 ns max

Single +5V DC power supply

Two chassis options

Full line of accessories

The Intel in-7000 Static RAM Memory System is a complete general purpose static memory with all required interface and control logic contained on a single printed circuit card measuring 10.8 \times 8.175 inches. Standard configurations are 16K words of 12, 16, 20, or 24 bits per card. The interface design of the in-7000 provides for system addressability up to 256K words (768K bytes when using the byte control mode). No external decoding is required. Each card slot in a multiple card system may be externally controlled or hardwired to respond to a given range of addresses, thus allowing all memory cards in a system to be identical and interchangeable. The word/byte control option allows the byte control to be used for either reconfiguration or byte control: in the word mode, the byte control inputs select either or both halves of a word, effectively reconfiguring a 16K \times 12 card to a 32K \times 6, a 16K \times 16 card to a 32K \times 8, etc.; in the byte mode, any combination of three bytes in a 25-byte word may be selected by the byte control inputs. Three-state drivers are utilized in the data output circuits for simplified "OR-tie" expansion and implementation of a bidirectional data bus. High speed cycle and address times for the in-7000 are identical at 250 nanoseconds. The in-7000 system may be housed in either of two optional chassis, with a full line of accessories, including an extender board and two utility boards.



FUNCTIONAL DESCRIPTION

The CM-7000 semiconductor memory module consists of a single printed circuit card containing the memory storage area and all the logic and circuitry required for memory operation, including data circuitry, address circuitry, mode enable and the word/byte control logic, timing logic, and a provision for three-state data pathing. All memory devices used on the CM-7000 are fully DC stable (static) and require no refreshing. The CM-7000 differs from the CM-7001 version only in cycle and access times, with all other specifications identical.

Capacity

Each in-7000 memory card has a maximum storage capacity of $16K \text{ words} \times 24 \text{ bits}$, with one word consisting of either two 12-bit data bytes or three 8-bit data bytes. The byte control inputs may be used to configure the system as a $16K \times 24$, $32K \times 12$, or $48K \times 8$ unit. Whatever the configuration, the maximum bit capacity remains the same. The in-7000 memory capacity may be expanded to $256K \times 24$, $512K \times 12$, or $768K \text{ words} \times 8 \text{ bits}$ by using multiple card systems.

Chassis Options

To accommodate a wide range of memory capacities, Intel offers a number of chassis options, available as standard equipment. The in-7000 system, whose outer dimensions and card outline are shown in Figure 1, may be mounted in either of two optional chassis, the 7-inch wide horizontal mount minichassis or the 10½-inch vertical mount unichassis.

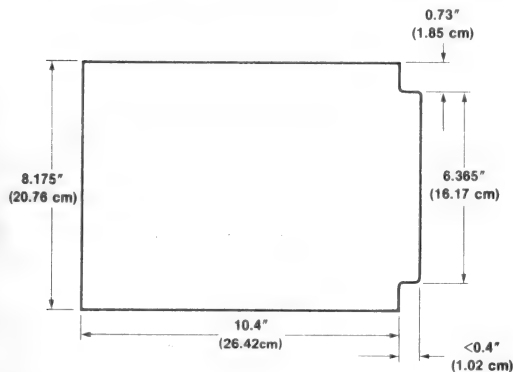


Figure 1. CM-7000 System Card Dimensions

Minichassis — The 7-inch HC-7000-000 Minichassis (see Figure 2) is a horizontal mount chassis designed to accommodate up to eight CM-7000 circuit cards, providing a maximum storage capacity of $128K \times 16$ or 96×24 . The chassis is mounted on slides for easy movement in and out, and may be mounted in a standard 19-inch relay rack. All connections are made from the rear of the unit.

The unit features a front panel circuit breaker and power indicator light, and use of an unwired backplane for all power and ground connections. The minichassis power supply, included in the unit, provides power for all in-7000 systems included in the unit.

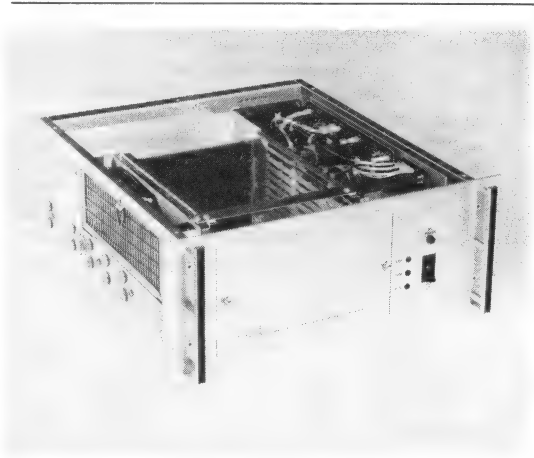


Figure 2. HC-7000-000 Minichassis Unit

Unichassis — The 10½-inch VC-40 Unichassis (see Figure 3) is a vertical mount cardcage designed to accommodate up to 33 CM-7000 printed circuit cards for mounting in a standard 19-inch relay rack. The chassis may be wired for a number of memory sizes and configurations (e.g., $128K \times 96$ or $256K \times 48$ with 32 cards), and may also be used in multiple systems for even larger memory configurations. The unichassis features the use of a full PC backplane with provisions to accept individual I/O cable wiring or DIP-socket flat cable connectors.

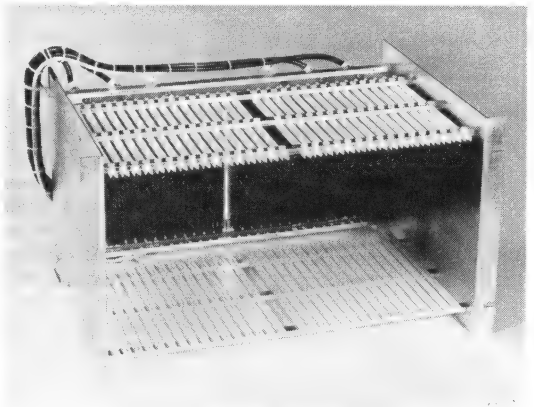


Figure 3. VC-40 Unichassis Unit

Operation

The in-7000 operates in read, write, and read-modify-write modes. All memory cycles are initiated by externally supplied signals.

Interface

Input/Output — All input and output signals required by the CM-7000 are compatible with TTL integrated circuits. The CM-7000 receives 18 inputs from the processor and returns one read data output. Five signals generated on the memory card (the write data clock signal and four output enable signals) are available at the interface as both inputs and outputs. The operations initiated by these signals may be controlled either internally or externally. For internal control, the output pins are externally wired back to the input pins. For external con-

trol, the externally generated signals are wired to the input pins. The full range of input and output operations for the CM-7000 are summarized in Tables 1 and 2, respectively.

Signal	Operation
Read data (0-23)	Transfers read data from memory to processor via 24 binary lines. (Access time is specified on plug.) Latches data and remains stable while output enable signal is active or until 100 ns of next cycle. Opposite in polarity to write data signal.

Table 2. in-7000 Output Signal Operation

Signal	Operation	Signal	Operation
Cycle request	Initiates memory cycle upon going low. Required at beginning of each cycle.	Byte control (1, 2, 3)	Disables operation of any or all bytes when held low (with word/byte enable signal also held low).
Read/write	Initiates read cycle when held high; initiates write cycle upon going low at beginning of cycle, and held low for duration of cycle.	Address (0-17)	Controls address selection on 18 binary lines from processor to memory. Address lines must be stable at cycle initiation and held stable to a maximum 100 ns cycle time.
Read-modify-write	Must be held high during read and write cycles. Enables read-modify-write mode during read operation if driven low within 50 ns after cycle request. Initiates write portion of cycle (after data is modified) if driven high within 250 ns after cycle request, to achieve minimum 440 ns read-modify-write cycle time. Initiates cycle independently of other command signals.	Module select (0-3)	Selects memory module, in conjunction with four highest order address bits. Used to select single card from 16 available in fully expanded in-7000 memory system.
Word/byte enable	Determines, in conjunction with byte enable signals, whether independent operation of memory word is three 8-bit bytes or two 12-bit words, assuming card is fully populated for 24-bit word. Enables byte selection by three byte enable inputs of 8-bit bytes when held high. Enables byte selection by two byte enable inputs of 12-bit word when held low. Normally is permanently connected to either high or low state.	Write data (0-23)	Controls binary data transfer on 24 data lines from processor to memory. Must become stable within first 50 ns of write cycle, and within first 50 ns of write portion of read-modify-write cycle, and must be held stable until 150 ns after cycle request, unless write data clock strobe is externally controlled.
		Write data clock	Enables write data latches via internal timing when on-board control signal pins on interface are hardwired externally. Controlled externally by applying desired timing signal.
		Output enable (4 lines)	Enables read data outputs and transfers read data onto output lines. May be internally or externally controlled by appropriated pin wiring.

Table 1. in-7000 Input Signal Operations

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the

quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring users of products with proven quality and reliability. In addition, all Intel memory systems products are covered by a one-year Intel warranty.

SPECIFICATIONS

Storage Capacity

Up to 16K words \times 24 bits

Word Length

12, 16, 20, or 24 bits per card, expandable to longer words by combining cards.

Performance

Cycle Time

Read or write cycle: 250 ns (in-7000), 350 ns (in-7001)

Read-write-modify cycle: 440* ns (in-7000), 610* ns (in-7001)

Access Time — 250 ns (in-7000), 350 ns (in-7001)

*Note

Modify time must be added

Operational Modes

Read (NDRO)

Write

Read-modify-write

Interface Characteristics

Connector — 100-position double-sided PC edge, 0.125-in. centers

Interface — TTL compatible

Address Input — 18 binary lines (single ended)

Data Input — Up to 24 lines (single ended)

Data Output — Up to 24 lines (single ended)

Control Input — 11 lines: cycle initiate, read/write, read-modify-write, word/byte option, byte control 1-3, module select 0-3 (single ended)

Physical Characteristics

Card

Width: 8.175 in. (20.76 cm)

Height: 10.80 in. (27.43 cm)

Depth: 0.450 in. (1.15 cm)

Weight: 1.0 lb (0.46 kg)

Minichassis

Width: 19 in. (48.26 cm)

Height: 7 in. (17.78 cm)

Depth: 17 in. (43.18 cm)

Weight: Less than 70 lb (154 kg)

Unichassis

Width: 19 in. (48.26 cm)

Height: 10.5 in. (26.67 cm)

Depth: 12.5 in. (31.75 cm)

Weight: Less than 70 lb (154 kg)

Electrical Characteristics

DC Power Requirements

Voltage	Current* (max)
+ 5.0V \pm 5%	9A

*Selected or unselected

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient; - 40°C to + 125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Optional Equipment

HC-7000-000 — Minichassis for up to six in-7000 cards; includes cooling fans, power supply, and unwired backplane.

VC-40 — Unichassis cardcage to hold up to 33 in-7000 cards; includes unwired backplane.

EX-10 Extender Board — A multilayer printed circuit board used for maintenance purposes; compatible with the in-7000, the minichassis, and the unichassis.

UT-10 — A utility board containing 24 positions for 16-pin IC's and space for two 50-pin flat cable sockets; compatible with the in-7000, the minichassis, and the unichassis.

Reference Manuals

TM-7000-000 — in-7000 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-7000-216	16K × 12	Memory system card with cycle and access times of 250 ns
CM-7000-616	16K × 16	Same as above except capacity
CM-7000-016	16K × 20	Same as above except capacity
CM-7000-416	16K × 24	Same as above except capacity
CM-7001-216	16K × 12	Memory system card with cycle and access times of 350 ns
CM-7001-616	16K × 16	Same as above except capacity
CM-7001-016	16K × 20	Same as above except capacity
CM-7001-416	16K × 24	Same as above except capacity
HC-7000-000	—	Minichassis for up to 6 in-7000 cards. Includes cooling fans, power supply and unwired backplane
VC-40	—	Unichassis cardcage to hold up to 33 in-7000 cards. Includes unwired backplane.
BA-40	—	Blower assembly for VC-40
EX-10	—	Extender card for in-7000
UT-10	—	Utility board for in-7000
IC-10	—	Interface connector for HC-7000 or VC-40 backplanes, or VC-40 backplanes



in-477 CRT REFRESH MEMORY SYSTEM

Single card memory system complete with addressing and timing logic

256K-bit capacity, addressable as 16K-word \times 16-bit or as 256K-word by 1-bit memory

Used with computer driven 512×512 CRT image display matrix

Expandable in multiple card systems for both gray scale and color displays

Utilizes MOS dynamic RAMs for maximum bit density at low system cost

Operates in single bit, serial word, and parallel word mode control

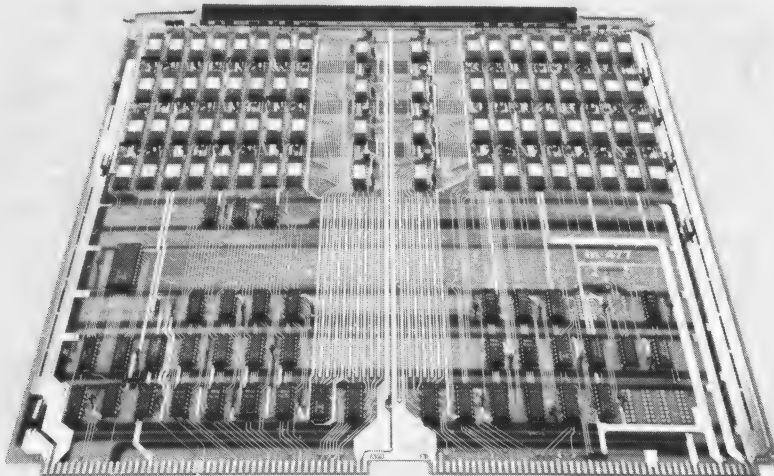
Provides automatic refresh or externally initiated refresh

Provides high speed 10 MHz bit rate in serial read mode

- access time: 450–650 ns
- cycle time: 280–350 ns

Provides jumper selectable system control options

The Intel in-477 CRT Refresh Memory System is a special purpose, single card, random access memory designed to store and retrieve digital video image data for sophisticated computer driven CRT displays. The storage capacity of each card is 256K ($K = 1024$) bits, addressable as either a 16K-word \times 16-bit memory or a 256K-word \times 1-bit memory, expandable by combining additional cards in multiple card systems. The 256K-word memory maintains a one-to-one relationship with each picture element comprising the 512×512 graphic matrix common to most CRT terminals. The in-477 refresh memory is specifically designed for image enhancement applications; refresh may be accomplished either by normal read and write cycles or by user generated refresh cycles within the specified retention time. Each card may be operated in single-bit per cycle serial mode or in a 16-bit parallel mode to create both gray scale and multi-color displays; the 16-bit parallel-to-serial register includes external clocking and loading to permit serial bit readout at speeds higher (10 MHz max) than those possible during normal card cycle time. The in-477 utilizes $4K \times 1$ -bit MOS dynamic RAM technology for maximum bit density at low system cost. Two chassis models have been designed for in-477 multiple card housing and are available as standard optional equipment. A variety of optional system control features may be implemented using a number of available jumper options, thus providing design flexibility in a wide range of specialized applications.



SPECIFICATIONS

Storage Capacity

256K bits, addressable as 16K-word 16-bit memory, or as 256K word 1-bit memory.

Performance

Cycle Time — 650 ns max

Access Time — 350 ns max

Retention Time — 2 ms max

Split Cycle (R/M/W) — 950 ns max

Serial Data Rate — 10 MHz max

Operational Modes

Parallel read (16 bits)

Parallel write (16 bits)

Parallel read-modify-write (16 bits)

Single bit read

Single bit write

Single bit read-modify-write

Serial read

Refresh

Clear set

Interface Characteristics

Connectors — Interface connections for the memory may be made via two 100-pin edge connectors on the memory card which mate with any of the following connectors:

Intel: 46-0010-001

Viking: 3VH50/1CN5

Amp: 1-67878-0

CDC: VPB01C50E00A1

Sylvania: 7900-0281-X

Input/Output — TTL compatible

Address Input — 18 binary lines

Data Input/Output — 17 open-collector, bidirectional lines, as follows:

Parallel Data: 16 lines

Single Bit Data: 1 line

Serial Data: 1 line

Control Input — Nine lines: clock enable, write enable, word/bit select, mode enable, card select, write time gate, clear memory enable, shift register load, serial shift clock

Control Output — Data

Physical Characteristics

Width: 15 in. (38.10 cm)

Length: 15 in. (38.10 cm)

Mounting Centers: 0.5 in. (1.27 cm)

Electrical Characteristics

DC Power Requirements

Voltage ($\pm 5\%$)	Current (max)
+5V DC	3.0A
+12V DC	1.5A
-5V DC	0.05A

Environmental Characteristics

Temperature — 0°C to +50°C operating ambient, -40°C to +125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-477-000 — in-477 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-477	256K \times 1	512 \times 512 \times 1 video refresh memory card with cycle and access times of 650 ns and 350 ns, respectively
CM-477-1	256K \times 1	512 \times 512 \times 1 video refresh memory card with cycle and access times of 450 ns and 280 ns, respectively
HC-477	—	Chassis with cooling fans and unwired backplane to accommodate up to 12 CM-477 cards
VC-477	—	Chassis with unwired backplane to accommodate up to 24 CM-477 cards
UT-477	—	Utility card
EX-477	—	Extender card



in-5770 VIDEO REFRESH MEMORY SYSTEM

Single card memory system complete with addressing and timing logic

256K-word \times 4-bit capacity in four image planes, each 256K \times 1 bit wide

Four-bit resolution, allowing 16 shades of gray for image enhancement

Expandable in multiple card systems for greater resolution in both gray scale and multicolor displays

Utilizes MOS dynamic RAMs for maximum bit density at low system cost

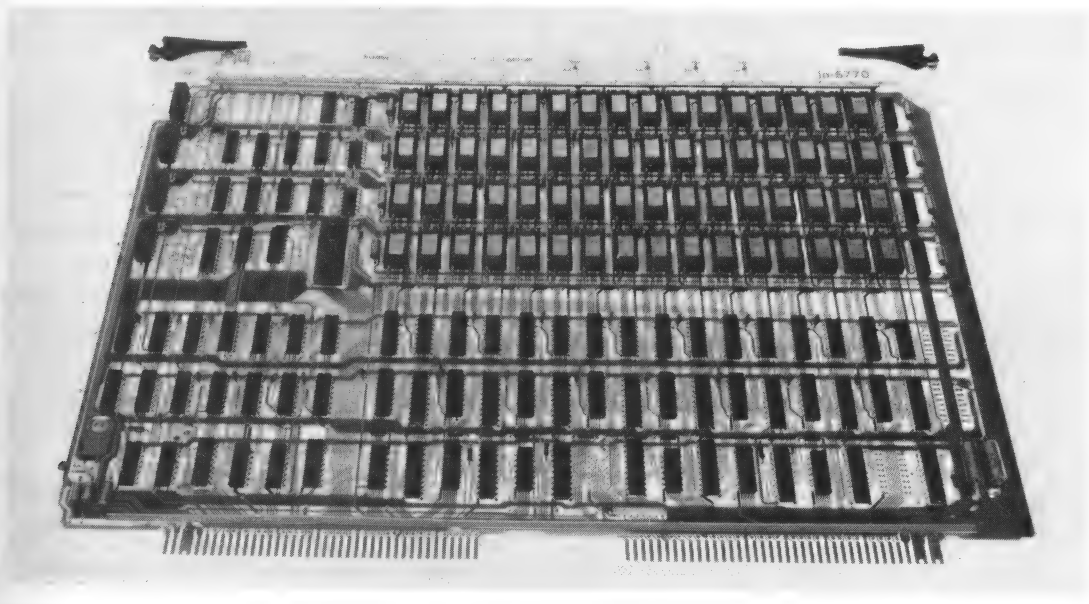
Operates in both parallel and single bit mode control

Provides automatic refresh or externally initiated refresh

High speed 14.3 MHz bit rate in serial read mode

MEMORY
SYSTEMS

The Intel in-5770 Video Refresh Memory System is a special purpose, single card, random access memory system designed to store and retrieve digital video image data for sophisticated computer driven CRT displays. The storage capacity of each card is 256K ($K = 1024$) 4-bit words arranged in four image planes to provide the 16 gray shades necessary to ensure the high picture quality required for medical and scientific laboratory computer modeling displays; a typical image enhancement application is the detailed analysis and interpretation of black and white x-ray images. Multiple in-5770 cards may be used in parallel for systems applications requiring more than four bits per picture element for special graphic displays such as color enhancement, overlays, or enlargements of portions of the display. The in-5770 refresh memory is specifically designed for image enhancement applications; refresh may be accomplished either by normal read and write cycles or by user generated refresh cycles within the specified retention time. Each memory card contains all the logic and timing circuitry required to generate memory addresses and clock pulses, and utilizes 16K \times 1 MOS dynamic RAM technology for maximum bit density at low system cost. An optional chassis and power supply are available for multiple card housing.



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FUNCTIONAL DESCRIPTION

The in-5770 is a video refresh random access memory card system designed specifically for storing and retrieving digital video image data with high resolution, but also used for conventional storage applications. The complete system consists of one 16 x 11.25-inch edge connector type printed circuit card containing the semiconductor storage area and all the required address and data latches and control logic needed to operate the memory. The two standard configurations are 512 x 512 using Intel's 16K x 1 dynamic MOS RAM and 512 x 256 using the 8K x 1 dynamic MOS RAM. The memory is arranged in four planes either 16K x 16 or 8K x 16. A block diagram of the in-5770 memory system is shown in Figure 1.

Capacity

Each CM-5770 memory card has the capacity to store a 512 x 512 display with four bits per picture element. The two standard configurations are 512 x 512 x 4 (CM-5770-512) and 512 x 256 x 4 (CM-5770-256). The memory stor-

age area in the 512 x 512 version consists of 64 Intel 16K x 1 dynamic N-channel MOS RAM silicon gate memory chips. The 16,384 storage cells on each chip are arranged in a 128 x 128 array requiring seven row and seven column addresses to select one cell. Each cell holds one bit of information. The memory chips are arranged in four rows of 16 chips each, with each 4 x 4 block of chips representing one 16K x 16 plane of data. The memory storage area in the 512 x 256 version uses 64 Intel 8K x 1 dynamic N-channel MOS RAM memory chips with 8192 storage cells arranged as a 64 x 128 array. The 8K RAMs are partial 16K devices with only one half of the array operational. The in-5770 memory capacity may be expanded using up to a maximum of 24 CM-5770 cards per system.

Chassis Option

To accommodate a wide range of memory capacities, Intel offers a number of chassis options, available as standard equipment. The in-5770 system, whose outer dimensions and card outline are shown in Figure 2, may be mounted in the optional VC-5770 vertical chassis.

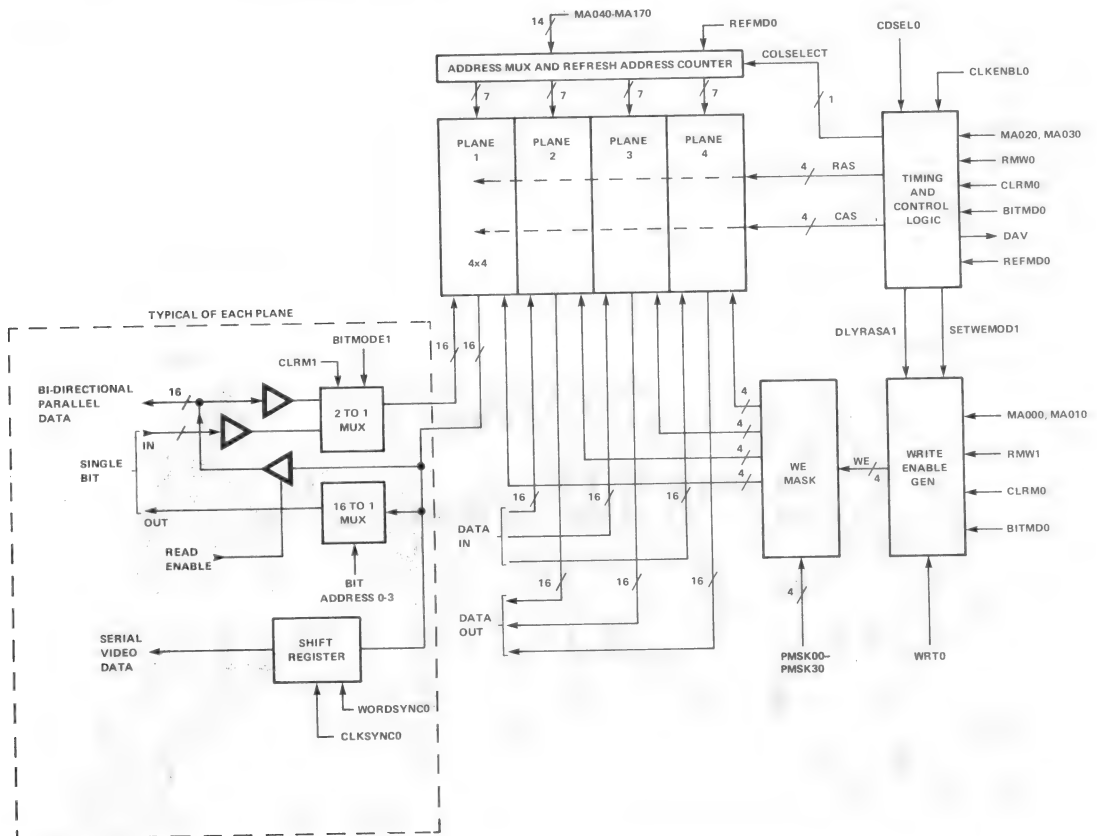


Figure 1. In-5770 Video Refresh Memory System Block Diagram

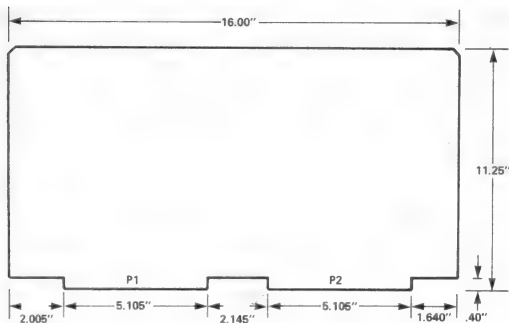


Figure 2. in-5770 Card Dimensions

Vertical CRT Chassis — The VC-5770 (as shown in Figure 3) is a 24-slot chassis used for a combination of in-5770 CRT refresh memories and custom control interface card mounted vertically. The UT-5770 utility card may also be used with the in-5770 to provide custom logic. Power supplies and cooling fans are not included. Power is supplied by the in-CPS series of power supplies.

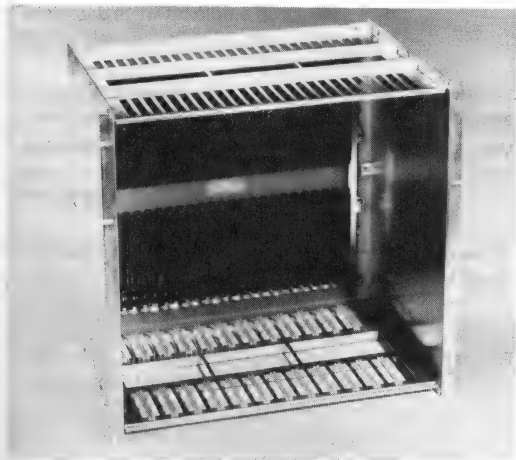


Figure 3. VC-5770 Vertical CRT Chassis Unit

Chassis Power Supply — For the VCRT chassis option when used with the in-5770 CRT refresh memory card, in-CPS power supplies are recommended, as shown in Table 5. Four models are available to satisfy the power requirements of a range of memory cards from 1 to 24. The VC-5770 has space for up to 24 in-5770 cards.

Operation

The in-5770 provides both parallel and single bit mode control to perform four basic memory operations plus the refresh operation. The card is read in a sequential manner for CRT refreshing, with random access read, write, or read-modify-write operations performed in

VC-5770 (qty)	Power Supply Model	Power Supply Drawers
1-4	in-CPS-1	1
5-8	in-CPS-2	1
9-16	in-CPS-3	1
17-24	in-CPS-4	1

Note
Power must be specified if other than 110V AC, 50/60 Hz.

Table 1. in-CPS Power Supplies

between the CRT refresh reads. During a CRT refresh read, 16 bits of data from each plane are read on the memory card and are internally converted to serial bit lines, clocked at 70-nanosecond or longer intervals.

Read Operation — In all read modes, a full 16-bit data word is read out from the addressed location in each memory plane. During parallel read operations, a 16-bit data word is read from each plane of the memory array and placed on the output lines, 64 lines in all, resulting in 64 bits being simultaneously available at the interface. During serial read operations, 16 bits from each memory plane are loaded into shift registers and transferred out serially on four output lines. During single bit read operations, a 16-bit word is read from each of the four memory planes, but only one bit from each plane is transferred to the single bit output lines.

Write Operation — In write modes, 64 bits of data are stored in the location specified by the address inputs. During parallel write operations, 64 bits are received at the interface, and stored as four 16-bit words, one in each memory plane. The parallel write mode writes a 16-bit data word selectively in any or all of the planes, under control of a plane select mask. During single-bit write operations, four bits (one pixel) are received at the interface and stored with one bit in each memory plane.

Read-Modify-Write Operation — In a read-modify-write operation, internal memory timing is arranged so that read data is output from the card during the first portion of the cycle, followed by a 90 ns modify period during which a new data word is generated by the user and stored in the memory. During a parallel read-modify-write operation, a full 16-bit word is read and rewritten in each memory plane. During a single bit read-modify-write operation, a single bit is read and rewritten into each memory plane.

Clear Operation — A clear mode provides a convenient way for clearing the screen and for generating test patterns. During a clear mode operation, the data applied on the single bit input lines is written into all 16 bits of the selected address in all four memory planes.

Video Refresh Operation — In image enhancement applications, photographic or video images are converted to a matrix of picture elements with binary elements designating the intensity assigned to each. This information is sent from the computer to the refresh memory and stored for later CRT display. Since data sent directly to a screen from the computer quickly fades, the in-5770 continuously recreates stored graphic images as required by projecting a 512 x 512 matrix of shaded picture elements onto the CRT screen.

Memory Refresh Options — All rows of memory devices within the in-5770 must be refreshed once every 2 milliseconds to prevent loss of data. The refresh operation takes place automatically during serial read for video refresh. However, if normal read operations do not use all 128 chip rows within the memory, refresh cycles must be externally initiated. Data refreshing in N-Channel MOS RAMs is normally achieved by sequentially scanning the memory at the rate of 128 times each 2 milliseconds.

Interface

Input/Output — All in-5770 input/output signals are compatible with TTL integrated circuits. The input and output signal operations for the in-5770 are summarized in Tables 2 and 3, respectively.

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced.

Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring the users of products with proven quality and reliability. In addition all Intel memory systems products are covered by a one year Intel warranty.

Signal	Operation
Data available	Indicates to processor, upon going high at access time, that valid read data is available on data bus.
Single bit data (0-3)	Transfer single bit read data out of memory on four unidirectional lines.
Serial video data (0-3)	Transfers serial video data out of memory on four unidirectional lines.

Table 3. in-5770 Output Signal Operations

Signal	Operation	Signal	Operation
Addresses (0-17)	Controls address selection of both single bit data and parallel data on 18 bidirectional lines.	Clear mode	Initiates write operation, when held low at beginning of cycle, of data on single bit write data lines into all 16 bits of addressed word.
Card select	Enables memory activity on card when low.	Parallel read enable	Enables, when low, readout of data onto 64 bidirectional lines.
Memory cycle start	Initiates memory cycle upon going from high to low.	Video data load sync	Enables, when low, parallel loading of shift registers for serial transfer out of video data during serial read operations.
Bit mode	Indicates to memory, when low, that single bit write cycle or read-modify-write cycle is to be performed. Enables parallel operation when high.	Video data serial clock sync	Clocks shift registers, upon going from low to high, for serial transfer out of video data during serial read operations.
Write	Initiates write operation when held low at beginning of memory cycle.	Refresh mode	Initiates refresh cycle, when held low at beginning of memory cycle, on address location specified by internal refresh counter.
Read-modify-write	Initiates read operation when held low at beginning of memory cycle. Initiates write operation after 90 ns delay. Writes user supplied data into location initially read out.	Single bit write data (0-3)	Transfers single bit write data to memory on four bidirectional lines, 16 for each plane.
Plane select write mask	Inhibits writing operation, when driven low during write or read-modify-write operation on data within given planes, on all data within that plane.	Parallel memory data (0-15)	Transfers parallel data to and from memory on 64 bidirectional lines, 16 for each plane.

Table 2. in-5770 Input Signal Operations

SPECIFICATIONS

Storage Capacity

256K \times 4 bits, addressable as 64-bit words (16 bits per image plane), or as 4-bit words (1 bit per image plane)

Word Length

16 bits on the parallel bus per image plane
1 bit on the single bit bus per image plane
1 bit on the serial data bus per image plane

Performance

Cycle Time

Read, Write, or Refresh: 450 ns max
Read-Modify-Write: 780 ns max

Access Time

Parallel Data: 380 ns max
Single Bit Data: 390 ns max

Retention Time — 2 ms max

Serial Data Rate — 14.3 MHz max

Operational Modes

Parallel write (16 bits)
Parallel read-modify-write (16 bits)
Single bit write
Single bit read-modify-write
Parallel read (16 bits)
Single bit read
Serial read
Clear mode write
Memory refresh

Interface Characteristics

Connector — Two 80-pin double-sided PC edge, 0.125 in. centers, type SAE 8100 (Stanford Applied Engineering) or equivalent

Input/Output — TTL compatible (single ended)

Address Input — 18 binary lines

Data Input

Parallel Data: 64 bidirectional lines
Single Bit Data: 4 unidirectional lines

Data Output

Parallel Data: 64 bidirectional lines
Single Bit Data: 4 unidirectional lines
Serial Mode Data: 4 unidirectional lines

Control Input — 17 lines: memory cycle start, write, single bit mode, read-modify-write, card select, refresh, plane select write masks 0 through 3, clear mode, parallel read enable 0 through 3, serial data clock, serial data load enable, video data load sync

Control Output — Data available

Interface Signals

Input

Low: -1.0V to $+0.8\text{V}$ @ 2 mA
High: $+2.2\text{V}$ to $+5.5\text{V}$ @ 100 μA

Output

Low: -0.5V to $+0.5\text{V}$ @ 15 mA
High: $+2.4\text{V}$ to $+5.2\text{V}$ @ 200 μA

Physical Characteristics

Card

Width: 11.25 in. (28.58 cm)
Length: 16 in. (40.64 cm)
Weight: 2 lb (1 kg)
Mounting Centers: 0.625 in. (1.59 cm)

Chassis

Width: 19 in. (48.26 cm)
Height: 17.5 in. (44.45 cm)
Depth: 11.5 in. (29.21 cm)

Electrical Characteristics

DC Power Requirements

Voltage ($\pm 5\%$)	Current (max)
+12V	2.5A
+5V	2.75A
-5V	100 mA

Environmental Requirements

Temperature — 0°C to 55°C operating ambient, -40°C to 125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 40,000 ft max, non-operating

Cooling — 200 linear ft per minute

Optional Accessories

IC-10 — 96-pin interface connector

EX-5770 — Extender card

UT-5770 — Utility card

IN-BA — Blower assembly (for VC-5770 only)

VC-5770 — Vertical mount chassis/cardcage with unwired backplane to accommodate up to 24 CM-5770 cards.

Reference Manuals

TM-5770-000 — in-5770 Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5770-512	256K × 4	512 × 512 × 4 video refresh memory system card
CM-5770-256	128K × 4	256 × 512 × 4 video refresh memory system card
VC-5770	—	Chassis with universal backplane to accommodate up to 24 CM-5770 cards
UT-5770	—	Utility card
EX-5770	—	Extender card



in-1670 PDP*-11/70 ADD-ON MEMORY SYSTEM

Total hardware and software compatibility with PDP-11/70

128K-bytes storage capacity expandable to 1024K bytes in 128K-byte increments

User access to full PDP-11/70 address space at 3,932,160 bytes

MOS RAMs provide high density memory with low system cost

Two-way memory system interleaving

ECC and error coding for single bit error correction and double bit error detection

High speed CPU data transfer rate

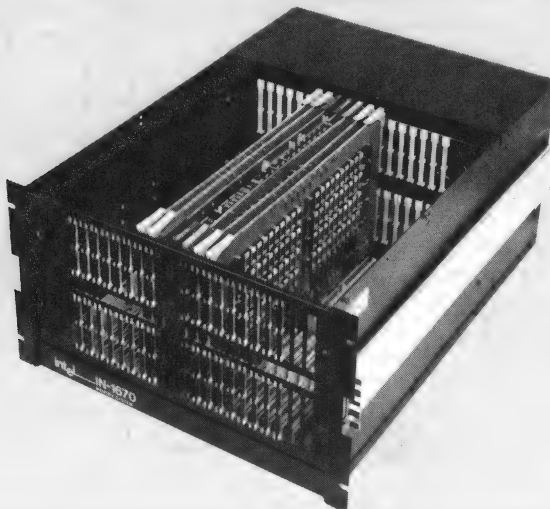
- cycle time: 790 ns
- access time: 950 ns

Installation and maintenance available from Intel

UL recognition

MEMORY
SYSTEMS

The Intel in-1670 PDP-11/70 Add-On Memory System is a monolithic memory system offering up to one megabyte of add-on memory for PDP-11/70 users, thus improving PDP-11/70 system performance with increased capacity, increased data transfer-speed, improved functional and component reliability, and reduced cost. The complete in-1670 system utilizes four types of printed circuit cards: memory unit cards, control unit cards, data cards, and error logging cards. All components are fully hardware and software compatible with the DEC* central processing unit (CPU) and are engineered to meet or exceed the specifications of similar DEC components. The Intel in-1670 is used in PDP-11/70 computer systems as a direct replacement for the memory module (MK-11) supplied by DEC, and uses cables and interface signals identical to those used in DEC memory modules. The unit may be installed without change or modification to the DEC software, CPU, memory bus, or I/O structure. High density memory is provided by dynamic MOS RAM devices, and is expandable in 128K-byte increments to 1024K bytes. High speed 790-nanosecond read and write cycle times allow the maximum utilization of Unibus data throughput. The in-1670 system includes error coding and correction (ECC), error monitoring, and error logging.



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FUNCTIONAL DESCRIPTION

The in-1670 semiconductor memory system is specifically designed as an add-on memory for the DEC PDP-11/70 processor. The basic memory device is a monolithic integrated circuit using N-channel MOS transistors. The complete system uses four types of printed circuit cards: 1) control cards containing address and control circuitry; 2) data cards to provide interfacing and parity checking for read and write data; 3) error logger cards to monitor and log data error conditions; and 4) memory cards (MU-167As) for storage. Each memory module contains its own power supply and cooling. All on-line operating sequences are controlled by processor supplied controller signals and by internally generated response signals sent to the processor from the memory, and all system components are engineered to meet or exceed the specifications of similar DEC components. A simplified block diagram of the in-1670 memory system is shown in Figure 1.

Compatibility

The in-1670 is specifically designed for use in PDP-11/70 computer systems as a direct replacement for the DEC-supplied memory module (MK-11), and uses cables and address, data, and interface control signals identical to those in DEC memory modules. The unit may be installed in the DEC central processing unit (CPU) memory cabinet without change or modification to the DEC software, CPU, memory bus, or I/O structure. All system voltages, currents, timing, and I/O signal requirements are compatible with the PDP-11/70.

Capacity

Card Capacity — Each memory card in the in-1670 memory system has a capacity of 64K bytes. Two memory cards make up the basic 128K-byte storage in increments of the in-1670 memory system. A fully expanded memory system contains 1024K bytes. Interleaving is possible between two memory systems with the same capacity.

System Capacity — The storage area of the in-1670 system consists of 16 Intel MU-167A memory system units. Each MU-167A contains 80 Intel 2109 8K dynamic MOS RAMs to provide a capacity of 32K words by 20 bits per card. The 16 MU-167A's in the system are configured to provide 256K words of storage with a double-word 40-bit interface. Thirty-two of the bits are assigned to data and eight of the bits to error correction and coding (ECC). These systems are housed in a chassis along with power supplies and fan assemblies. Up to four such chassis may be mounted in one equipment rack and interfaced in daisy-chain fashion with the processor.

Expandability — Each unit is easily field upgradable to larger capacities with the addition of memory cards or a memory rack containing cards. A diagram showing CPU and memory cabinet dimensions is shown in Figure 2.

System Components

The in-1670 consists of four basic printed circuit cards for memory storage, control, data transfer, and error logging, all housed in a system chassis with power sup-

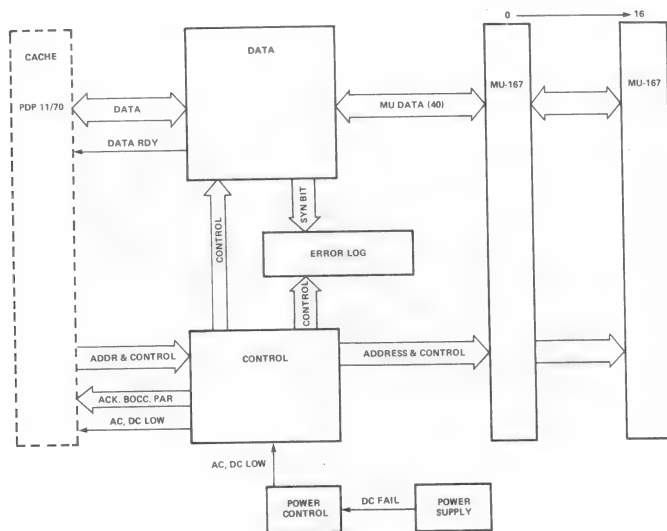


Figure 1. in-1670 Add-On Memory System Block Diagram

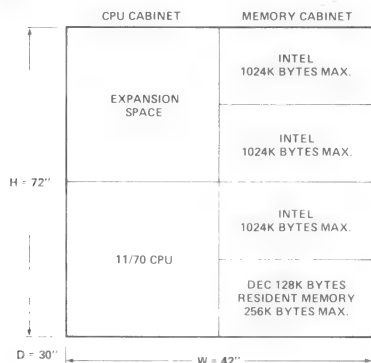


Figure 2. PDP-11/70 CPU Cabinet and in-1670 Add-On Memory Cabinet Dimensions

plies and fan assemblies. Up to four chassis may be mounted in one equipment rack and interfaced in daisy-chain fashion with the processor.

Maintainability

The in-1670 memory system provides convenient controls, reconfiguration switches, and status indicators as standard maintainability features, all located to provide easy maintenance access to the user.

Rear Panel Controls — The following controls are located on the rear panel of the memory module:

- AC circuit breaker
- Three power supply output voltage adjustments

Card Controls — The following controls are located either on the control card or on the error logger card:

- Address select switches to set the starting address for the memory bank
- Memory on-line/off-line switch to disconnect the in-1670 from the PDP-11/70 memory bus
- Reset logic switch
- Error logger on/off switch
- Lamp test

- ECC on/off switch
- Error logger scan switch

Card Indicators — The following indicators are provided either on the control card or on the error logger card:

- Address parity error indicator
- Mismatch error indicator
- Write data parity error indicator
- Address display
- Syndrome bits display
- Single bit mode or double bit mode indicator
- On-line/off-line mode indicator

Reliability

Error Correction Coding — The Intel in-1670 memory system includes error correction coding (ECC) as a standard feature. The ECC logic detects single bit memory errors and automatically corrects a single bit failure prior to read operation. Since most memory errors are due to single bit failures, ECC provides a 10 to 25 times improvement in memory system reliability over systems with parity checking only. During write operations, ECC logic removes parity bits from the input data word and generates error correction code bits to be stored with the data word. When write data is received from the processor, it is checked for correct parity before being written into memory. During a read operation, the word is checked for correct status. The ECC circuitry automatically corrects the incorrect bit should a single bit be detected. A double bit error in the read word is not corrected. For double bit errors, all parity bits sent to the CPU are forced to the error state. This allows the CPU to process double bit errors as parity errors. The ECC logger records the faulty location address.

Quality Control and Assurance — Intel manufactures all the integrated circuit memory devices from which all Intel memory systems, including the plug compatible memories used in the DEC PDP-11 computer family, are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning processes of making the device through the final test and delivery of the system. This assures users of products with proven quality and reliability. In addition, all Intel compatible products are covered by a one-year Intel warranty.

SPECIFICATIONS

Storage Capacity

Up to 1024K bytes in 128K-byte increments

Word Length

16 bits per memory word, plus 8 check bits per double word

Performance

Cycle Time — 750 ns max

Access Time — 555 ns max

Operational Modes

Read

Write

Partial write (1 or 2 bytes)

Interface Characteristics

TTL compatible

36 bidirectional data input/output lines

23 binary address input lines (single ended)

Installation Requirements

All cables and connectors supplied by Intel
1 DEC memory cabinet (21"W x 30"D x 72"H)
1 in-1670 memory card

Notes

1. Installation can be done by the customer or purchased from Intel.
2. Maintenance contracts are available from Intel.

Physical Characteristics

Width — 10.5 in. (26.3 cm)
Height — 10.5 in. (26.3 cm)
Depth — 25.0 in. (77.5 cm)
Weight — Less than 70 lb (54 kg)

Electrical Characteristics

AC Power Requirements

Requirement	115V AC (max)	230V AC (max)
Voltage	90V AC to 140V AC	170V AC to 260V AC
Frequency	45 to 440 Hz single phase	45 to 440 Hz single phase
Input current	6.5A max	3.3A max

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, - 40°C to + 85°C non-operating

Humidity — 10% to 90% non-condensing

Altitude — 10,000 ft max, operating; 40,000 ft max, non-operating

Equipment Supplied

Ribbon cable supplied for installation

Reference Manuals

TM-1670-000 — in-1670 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
SY-1670-128	128K bytes (64K words)	Add-on memory system for PDP-11/70
SY-1670-256	256K bytes (128K words)	Same as above except capacity
SY-1670-384	384K bytes (192K words)	Same as above except capacity
SY-1670-512	512K bytes (256K words)	Same as above except capacity
SY-1670-640	640K bytes (320K words)	Same as above except capacity
SY-1670-896	896K bytes (448K words)	Same as above except capacity
SY-1670-1MB	1024K bytes (512K words)	Same as above except capacity
XF-1670-128	128K bytes	Expansion for in-1670 PDP-11 Add-On Memory System
EX-1670	—	Card extender
XX-1670-001	—	Memory card
XX-1670-002	—	Data interface card
XX-1670-003	—	Control card
XX-1670-004	—	Error logger card
XX-1670-005	—	Terminator board
XX-1670-006	—	Power control card
XX-1670-007	—	I/O cable assembly
XX-1670-008	—	Power supply
XX-1670-009	—	Diagnostic memory test. Includes magnetic tape.
XX-1670-010	—	Branch spare kit containing one each EX-1670 and XX-1670-001 through XX-1670-009



in-4011 PDP*-11 ADD-ON MEMORY SYSTEM

Total hardware and software compatibility with PDP-11

16K words × 18 bits per card basic module capacity

32K-word storage capacity expandable to 128K words in 16K-word increments

Two chassis options

4K MOS RAMs provide high density memory with low system cost

Two-way memory module interleaving

Integral parity control status register (CSR)

Unibus*-compatible interface card and cable

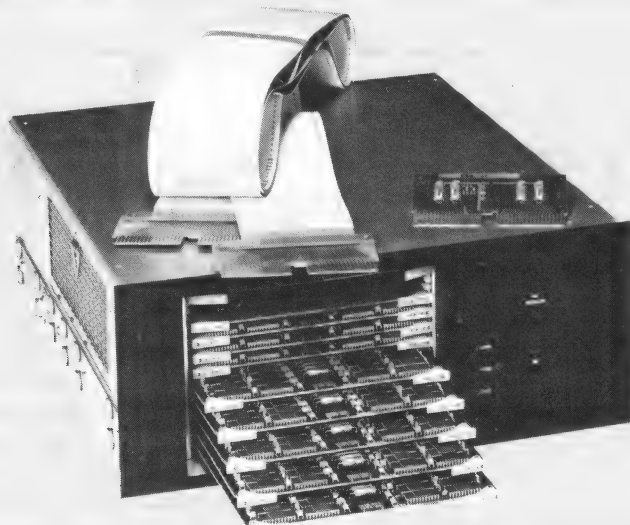
On-board switch selectable addressing

High speed data-transfer rate

- cycle time: 600 ns max
- access time: 500 ns max

MEMORY
SYSTEMS

The Intel in-4011 PDP-11 Add-On Memory System is a plug-compatible memory module designed for use within the DEC*PDP-11 family of computers, offering PDP-11 users the advantages of advanced semiconductor memory design and reliability with high density storage capacity. The complete in-4011 system utilizes four types of printed circuit cards: memory cards, control cards, buffer cards, and a Unibus interface card. All system components are fully hardware and software compatible with the DEC central processing unit (CPU) and may be installed, without change or modification to the DEC software, CPU, memory bus, or input/output structure, by mounting the module directly into a 7-inch section of a DEC memory cabinet. The in-4011 is used in PDP-11 computer systems as a direct replacement for the MT-11 memory module supplied by DEC, and uses Unibus-compatible cables and interface signals identical to those in DEC memory modules. High density memory is provided by 4K dynamic MOS RAM components, and is expandable in 16K-word increments to 128K words. Addressability is also set by on-board DIP switches thus permitting field address select changes. High speed 600-nanosecond read and write cycle times allow the maximum utilization of Unibus data throughput. The in-4011 system includes parity generation and checking. Control signals include parity error detect and DC voltage low detect. The system is housed in a single 7-inch high horizontal mount chassis with power supply and cooling fans included.



FUNCTIONAL DESCRIPTION

The in-4011 is a semiconductor memory system designed to provide add-on memory for the DEC PDP-11 processor, with all system components engineered to meet or exceed the specifications of similar DEC components. The basic memory device is a monolithic integrated circuit using N-channel MOS transistors. The complete system uses four types of printed circuit cards: 1) memory cards for storage; 2) control cards containing address and control circuitry; 3) buffer cards for buffering in expanded multiple card systems; and 4) Unibus interface cards for translating DEC control signals and enabling memory transmission to and from the Unibus. The standard in-4011 128K x 18-bit configuration consists of eight memory cards, one control card, and one Unibus interface card, all housed in a 7-inch horizontal mount chassis with a backplane adapted to accept a standard Unibus cable. A simplified functional block diagram of the in-4011 is shown in Figure 1. Block diagrams of the in-4011 system featuring word lengths of less than nine bits and more than nine bits are shown in Figures 2 and 3, respectively.

Compatibility

The in-4011 is specifically designed for use with the DEC PDP-11 family computer systems as a direct replacement for the DEC supplied MT-11 memory module, and uses cables that are compatible with the DEC Unibus, and address, data, and interface control signals identical to those used in DEC memory modules. The in-4011 is designed to be mounted directly into a 7-inch high section of a standard DEC cabinet, and covered by a standard 7-inch DEC bezel cover panel. All hardware required to install the in-4011 system is supplied by Intel, including slides and a six-foot line cord for AC power input. An eight-foot Unibus cable is provided for interface with the DEC Unibus. The in-4011 cardage configuration is shown in Figure 4.

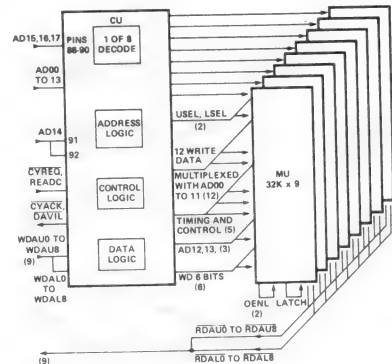


Figure 2. in-4011 System Block Diagram Featuring Word Lengths Less Than Nine Bits

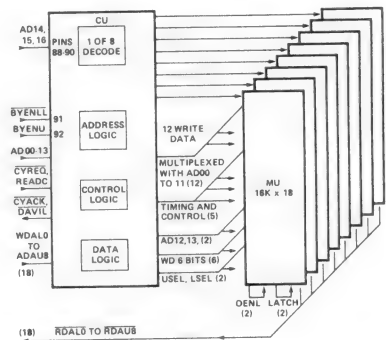


Figure 3. in-4011 System Block Diagram Featuring Word Lengths More Than Nine Bits

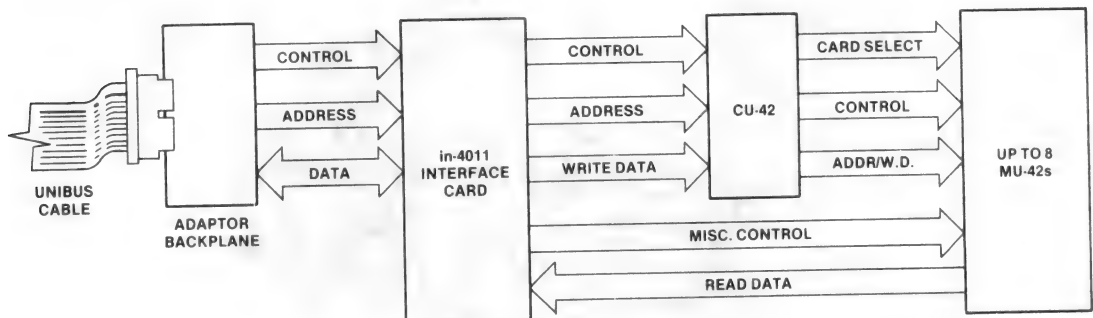


Figure 1. in-4011 Memory System Functional Block Diagram

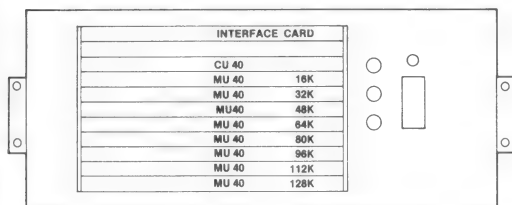


Figure 4. in-4011 Cardcage Configuration

Capacity

Card Capacity — Each memory card in the in-4011 memory module has a capacity of 32 bytes, providing either 16K words x 18 bits or 32K words x 9 bits per card.

System Capacity — The storage area of the fully expanded in-4011 system consists of eight Intel MU-42-816 memory cards, with each group of eight con-

trolled by a single control card. Each MU-42-816 contains 72 Intel 2107B 4096-word x 1-bit dynamic N-channel MOS RAMs arranged in four card columns and 18 card rows to provide a capacity of 16K words x 18 bits per card. The 4096 cells on each memory chip are arranged in two 32 x 64 cell arrays to form a 64 x 64 addressable matrix. One cell stores one bit of information. The eight memory cards in each system are configured to provide a total of 128K words of storage. The system's basic modular capacity of 16K words x 18 bits (or 32K x 9) per card set may be expanded to 128K x 18 or 256K x 9 by adding more memory cards. Separate control cards drive up to eight memory cards each.

Reliability

Intel manufactures all the integrated circuit devices from which all Intel memory systems are produced. Because of this vertical integration, Intel controls the quality of its equipment from the beginning process of making the device through the final test and delivery of the system, thus assuring users of products with proven quality and reliability. In addition, all Intel memory systems products are covered by a one-year Intel warranty.

SPECIFICATIONS

Storage Capacity

32K words per board, expandable to 128K words in 16K increments

Word Length

18 bits per word: 16 bits plus 2 parity bits

Performance

Cycle Time — 600 ns max

Access Times

Read: 500 ns max

Write: 400 ns max

Operational Modes

Read (NDRO)

Write byte

Write word

Refresh

Interface Characteristics

Interface — Unibus compatible with one bus load

Input/Output — TTL compatible

Data Input/Output — 16 bidirectional lines (single ended)

Address Input — 18 binary lines (single ended)

Control Input — 6 lines: master sync, control 1 and 2, address input, DC voltage low, initialize (single ended)

Control Output — 2 lines: slave sync, parity (single ended)

Physical Characteristics

Card

Width: 10.5 in. (26.7 cm)

Height: 8.175 in. (20.8 cm)

Depth: 0.45 in. (1.14 cm)

Weight: Less than 1 lb (2.2 kg)

Unichassis

Width: 19 in. (48.3 cm)

Height: 10.5 in. (26.7 cm)

Depth: 8.5 in. (21.6 cm)

Weight: Less than 70 lb (154 kg)

Note

Typical system of 128K x 18 (8 MUs, 1 CU, 1 interface, 1 chassis) weighs approximately 58 pounds.

Electrical Characteristics

Input Power — 200W max

AC Power Requirements

Voltage (± 10%)	Frequency
115V AC	60 Hz
220V AC	50-60 Hz

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, -40°C to +85°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-4011-000 — in-4011 Technical Manual (SUPPLIED)
TM-40-000 — in-40 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

MEMORY
SYSTEMS**ORDERING INFORMATION**

Model	Capacity	Description
SY-4011-032	32K × 18	Add-on memory for PDP-11/05 through PDP-11/55. Unibus cable and technical manual supplied. This system can be field expanded in increments of 16K words (to a maximum of 128K words) by adding MU-42-816 modules.
SY-4011-048	48K × 18	Same as above except capacity
SY-4011-064	64K × 18	Same as above except capacity
SY-4011-080	80K × 18	Same as above except capacity
SY-4011-096	96K × 18	Same as above except capacity
SY-4011-112	112K × 18	Same as above except capacity
SY-4011-128	128K × 18	Same as above except capacity
MU-42-816	16K × 18	Expansion module for in-4011 systems
CU-42	—	Control card
XX-4011-001	—	Unibus cable
XX-4011-002	—	Unibus I/O card
XX-4011-003	—	in-4011 power supply



in-4711 PDP*-11 ADD-IN MEMORY SYSTEM

Total hardware and software compatibility with PDP-11

On-board switch selectable addressing

16K-word x 18-bit capacity

Optional jumper selectable timing

Single card contains all address and control circuitry

High speed data transfer rate

- cycle time: 600 ns max
- access time: 250-450 ns max

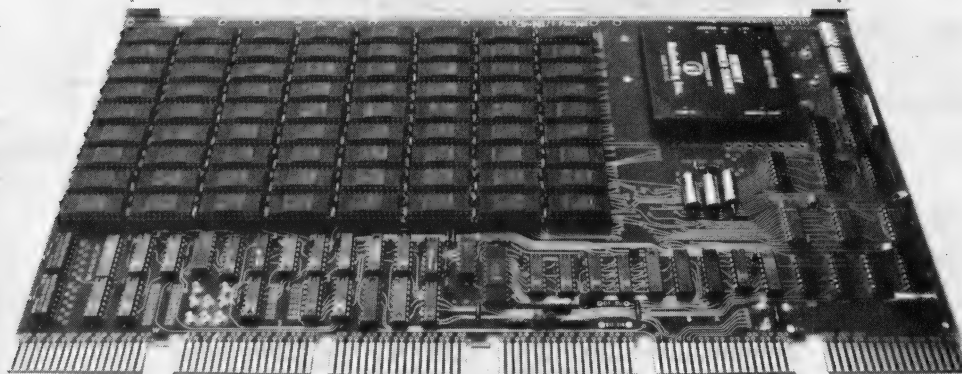
4K MOS RAMs provide high density memory with low system cost

Low power dissipation for higher system reliability

Two-way memory module interleaving

The Intel in-4711 PDP-11 Add-In Memory System is a plug-compatible memory module designed for use in the DEC* PDP-11 family of computers, offering PDP-11 users the advantages of advanced semiconductor memory design and reliability with high density storage capacity. The in-4711 is used with PDP-11/04, 11/05, 11/34, 11/35, 11/40, 11/45, and 11/50 computers, and is compatible with the PDP-11 Unibus*. For compactness, each in-4711 memory system module provides 16K words plus parity, as well as all address and control circuitry, on a single Unibus compatible printed circuit card occupying a single PDP-11 card slot. All system components are fully hardware and software compatible with PDP-11 systems and may be installed, without change or modification to either the computer or the module, by plugging the module directly into the PDP-11 system unit card slot. High density memory is provided by 4K dynamic MOS RAM components. Memory module interleaving is controlled by on-board dual-in-line package (DIP) selectable switching. Addressability is also set by on-board DIP switches, thus permitting address select changes. High speed 600-nanosecond read and write cycle times allow the maximum utilization of Unibus data throughput. The in-4711 is designed for low power dissipation and consumption, resulting in improved system reliability.

MEMORY
SYSTEMS



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FUNCTIONAL DESCRIPTION

The in-4711 semiconductor memory module consists of a single printed circuit card designed to fit into a DEC PDP-11 system unit printed circuit card slot, and containing all circuitry required for memory operation, including data circuitry, address circuitry, mode enable and byte control logic, timing logic, control logic, refresh control circuitry, a DC-DC converter for standard Unibus operation, a voltage regulator for the modified Unibus operation, and a memory storage area. All system components are engineered to meet or exceed the specifications of similar DEC components. A block diagram of the in-4711 memory system is shown in Figure 1.

Compatibility

The in-4711 is applicable to a broad spectrum of DEC PDP-11 computer configurations. These PDP-11 configurations provide various power supply voltages to operate the in-4711; thus, the in-4711 must be adapted to match the PDP-11 prior to shipment. Table 1 specifies the in-4711 model number and the applicable PDP-11 type for a 16K x 18 memory board. Card installation also varies with the model of PDP-11, as well as with the amount of initial memory capacity and the amount of memory added. Figures 2 and 3 shown three typical

installations. Figure 2 shows two horizontal mount positions: the first typically used for PDP-11/04 where slot 1 is generally allocated to a processor card and slot 2 to a bootstrap device or front panel emulator, leaving slots 3 and 4 available for memory cards; and the other typically used for PDP-11/34 where slot 1 is generally allocated to a processor card, slot 2 to a memory management card,

in-4711 Model	PDP-11 Type
in-4711/003	PDP-11/05, 11/10, 11/15, 11/35, 11/40, 11/45, 11/50, 11/55 with MF11-L or MF11-LP memory backplane with parity
in-4711/011	PDP-11/04, 11/34, with semiconductor memory and parity backplane
in-4711/027	PDP-11/04, 11/34 with core memory and parity backplane
Note The in-4711 does not operate in the DEC MF11-U, MF11-UP, DD11-A, or DD11-B backplanes. For these systems the in-4011 add-on memory is used to expand the PDP-11 memory. The in-4711 does operate in the DD11-C, DD11-CK, DD11-D, DD11-DK, DD11-P, and DD11-PK backplanes.	

Table 1. PDP-11 Computer Configurations

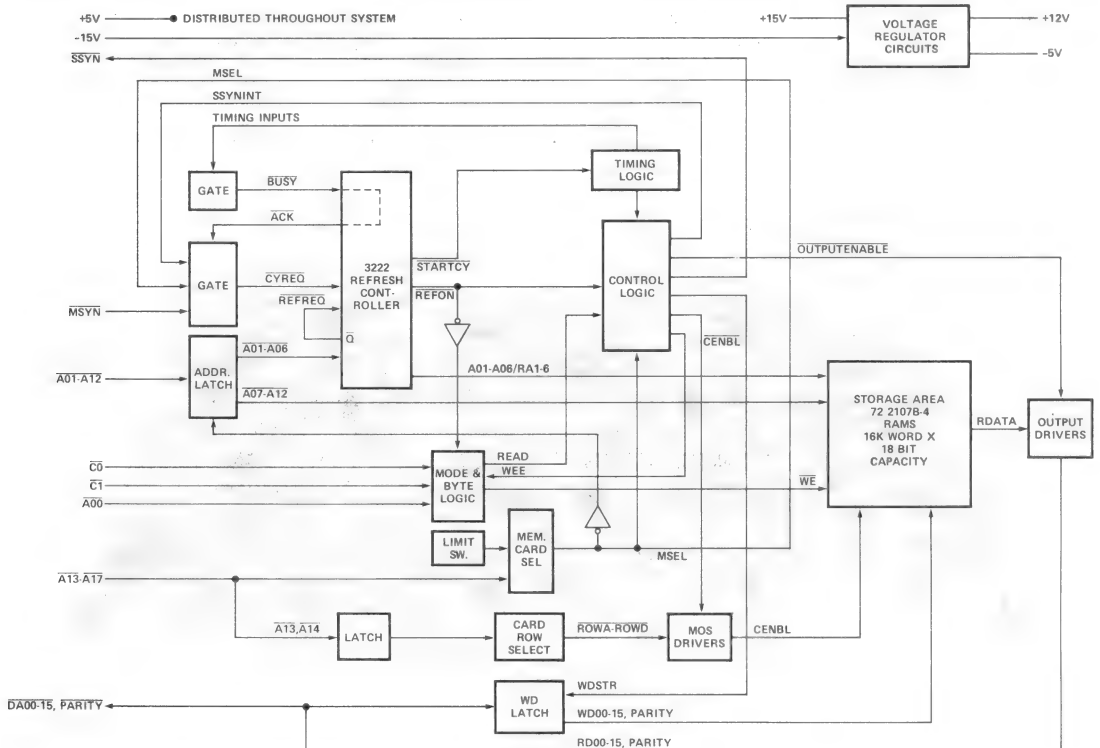


Figure 1. in-4711 Memory System Block Diagram

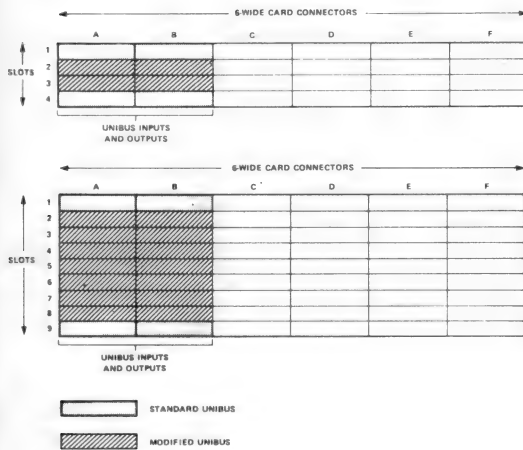


Figure 2. Typical in-4711 Horizontal Mount Installation

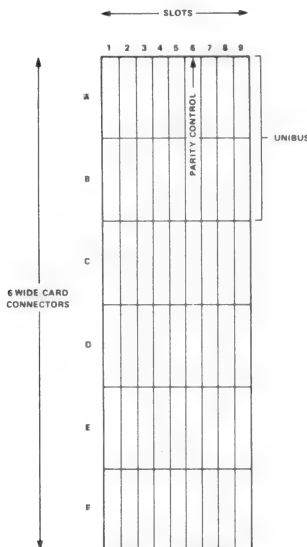


Figure 3. Typical in-4711 Vertical Mount Installation

and slots 3 through 8 to memory cards. Figure 3 shows a vertical mount system used with PDP-11/35, PDP-11/40, and PDP-11/45 where a backplane provides for a parity option and all slots may be used for memory cards, with the exception of slot 6, where two connectors are reserved for parity control if parity is provided. The in-4711 is specifically designed as a direct replacement

for DEC-supplied memory modules and consequently uses cables and interface control, address, and data signals identical to those used in DEC memory modules. The unit may be installed in the DEC central processing unit (CPU) memory cabinet without change or modification to the DEC software, CPU, memory bus, or input/output structure. All system voltages, currents, timing, and I/O signal requirements are compatible with all models of the PDP-11 computer.

Capacity

Each memory card in the in-4711 memory module has a basic capacity of 16K words by 18 bits, with a word consisting of two 8-bit data bytes (upper and lower) plus one parity bit per byte. The card may be depopulated to provide 8K words of storage with either one 16-bit or one 18-bit data word. Non-interleaved memories operate on 4K boundaries, with interleaving performed on 16K boundaries. The memory storage area consists of 72 Intel 2107 4K \times 1 dynamic N-Channel MOS RAM silicon gate memory chips.

Addressability

Address Circuitry — The in-4711 memory address circuitry consists of 18 address inputs supplied to the memory by the DEC processor, an Intel 3222 refresh controller for generating and multiplexing low-order internal chip and refresh addresses, an Intel 3404 latch for latching and decoding address input for the card row select signal, and two Intel MOS drivers for transferring address segments as full data words to the memory.

Address Range Selection — The address range for each module is set by on-board dual-in-line package (DIP) switches. Memory module starting and ending addresses are both selectable to any 4K boundary. Each memory module provides addressing inputs to allow expansion to 128K words and will operate with a DEC memory management unit when the total system memory is expanded beyond 28K words.

Address Selection — Address selection in the in-4711 takes place on several levels. Of the 18 address inputs received from the processor one is used for byte control, twelve are internal chip addresses, two are used to implement memory module interleaving, two are card row addresses, and three are card select addresses. The 18-bit address format is shown in Figure 4.

Byte Control — The in-4711 memory may be addressed in a variety of ways under control of the byte control address input. The memory is capable of performing either full word operations (read or write two bytes, upper and lower) or byte operations, during which data is written into either the upper or lower byte while the other byte remains unselected. These operations are enabled by the appropriate combination of two control signals (C1, C0), the write enable signal, and the lowest order address received from the processor, as follows: When C1 is high, a read operation is performed on the full word (i.e., both bytes). When C1 is low and C0 is high, a write operation is performed on the full word. When C1 and C0 are both low with the address input

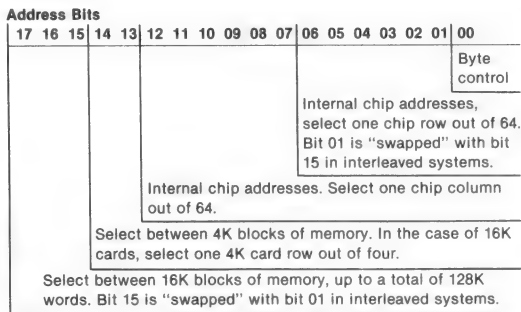


Figure 4. in-4711 Address Format

(A00) low, a write operation is performed on the upper byte; with A00 high, on the lower byte. During refresh operations, the refresh-on signal goes high and forces a read operation on both bytes. These byte control operations are summarized in Table 2.

Timing

Timing signals for the memory are generated by two 200-nanosecond delay lines with individual jumpers. The lines are started by a start signal output from the refresh controller at the initiation of each normal memory cycle or refresh cycle. A high-going pulse propagates through the first line, then through the second line, with the output from the first line buffered to pro-

vide the drive required for the second line. Taps are taken at 20-nanosecond intervals to supply the timing pulses needed for other circuit functions. Timing is jumper selectable, with the special timing for specific applications available on request.

Signal				Operation	
C1	C0	A00	REFON	Upper Byte	Lower Byte
H	X	X	X	Read	Read
L	H	X	L	Write	Write
L	L	L	L	Write	—
L	L	H	L	—	Write
X	X	X	H	Read (refresh)	Read (refresh)

Table 2. in-4711 Byte Control Operations

Reliability

The in-4711 is designed for low power dissipation. When operating at full speed in a PDP-11/34, the in-4711 dissipates 17.0 watts, in standby, 9.5 watts, resulting in a cooler running system, an increased margin for power supply operation, and improved system reliability. Since the in-4711 dissipates less power than the equivalent DEC memory, no special provisions are necessary for cooling. Each memory card is fully tested in a temperature cycling environment. Because of the 100% burn-in performed on each card, the user is assured of receiving Intel's proven quality and reliability. In addition, all Intel PDP-11 compatible products are covered by a one year Intel warranty.

SPECIFICATIONS

Storage Capacity

16K words per card

Word Length

16 bits plus 2 parity bits

Performance

Cycle Time — 600 ns max

Access Time

Read: 450 ns max

Write: 320 ns max

Operational Modes

Read

Write

Read byte

Write byte

Interface Characteristics

Interface — Unibus compatible, 1 bus load

Address Input — 18 binary lines (single ended)

Data Input/Output — 18 bidirectional lines (single ended)

Control Input — 3 lines (single ended)

Control Output — 1 line (single ended)

Physical Characteristics

Width — 15.4 in. (39.1 cm)

Height — 0.345 in. (0.09 cm)

Depth — 8.5 in. (21.6 cm)

Weight — Less than 2 lbs (0.9 kg)

Electrical Characteristics

DC Power Requirements

in-4711 Model No.	Operational	Standby
CM-4711-003	23.0W	15.5W
CM-4711-011, CM-4711-027	17.0W	9.5W

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, -40°C to +125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-4711-000 — in-4711 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-4711-011	16K x 18	Add-in memory card for PDP-11/34 with original semiconductor (MS11) memory
CM-4711-027	16K x 18	Add-in memory card for PDP-11/04 and PDP-11/34 with original core (MM11) memory
CM-4711-003	16K x 18	Add-in memory card for PDP-11/05, 11/10, 11/15, 11/35, 11/40, 11/45, 11/50, and 11/55 with MF-11L or MF-11LP backplanes only



in-5004 LSI-11 ADD-IN MEMORY CARD

MEMORY
SYSTEMS

Double width card size: 5 × 8.5 inches

Total hardware and software compatibility with LSI-11 and PDP-11/03

16K, 24K, or 32K words per card storage capacity

Optional 18-bit word length for byte parity

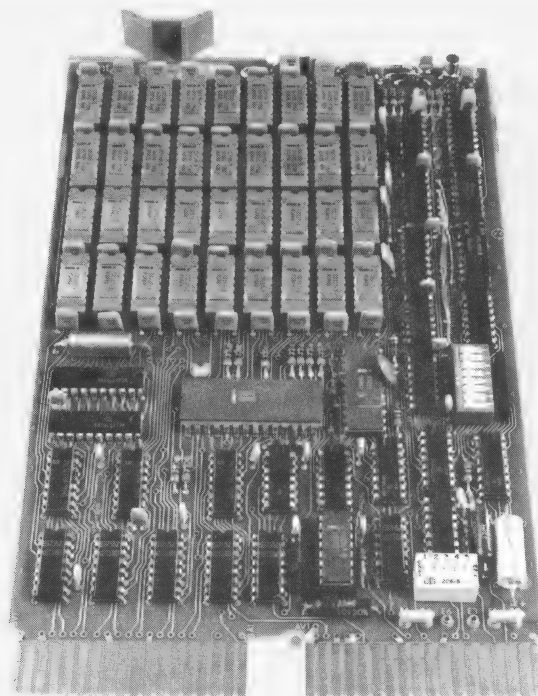
Dynamic MOS RAMs provide high density memory with low system cost

On-board switch selectable addressing

On-board refresh

Battery backup capability

The Intel in-5004 LSI-11 Add-In Memory Card is a plug-compatible memory module designed for use with DEC* LSI-11, LSI-11/2, and PDP*-11/03 microcomputer systems. Utilizing Intel dynamic MOS RAM devices, the in-5004 is available in 16K, 24K, and 32K-word × 16-bit capacities. An optional 18-bit word length is available for byte parity. The in-5004's on-board refresh circuitry may be user disabled in applications requiring an optional external refresh operation. Repositioning the appropriate jumpers will also reconfigure the in-5004 to accept external battery backup voltage inputs. Address segments of the in-5004 are switch selectable from 0 to 32K, in 4K increments. For simplified installation, each 4K segment is enabled by a single switch. A 30K or 31K upper address limit may also be selected for maximum memory utilization.



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SPECIFICATIONS

Storage Capacity

16K, 24K, or 32K words

Word Length

16 bits per word with optional 18-bit word length available for byte parity

Performance

Cycle Time — 550 ns max

Access Time

Read: 250 ns typ, 325 ns max (BSYNCL to BRPLY)

Write: 150 ns typ, 200 ns max (BDOUTL to BRPLY)

Operational Modes

Read

Write

Read-modify-write

Physical Characteristics

Width — 8.5 in. (21.3 cm)

Length — 5 in. (12.7 cm)

Electrical Characteristics

DC Power Requirements

Power ($\pm 5\%$)	Operating (max)	Standby (max)
System Power		
+5V +12V	0.9A typ (1.4A) 0.35A 11W	0.9A typ (1.4A) 0.075A 8W
Battery Backup Power	0.3A typ (0.50A) 0.075A	
+5V +12V		

Environmental Characteristics

Temperature — 0°C to +50°C operating ambient,
–40°C to +125°C non-operating

Relative Humidity — Up to 90% non-condensing

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

Reference Manuals

TM-5004-000 — in-5004 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5004-616	16K \times 16	Add-in memory card for LSI-11, LSI-11/2, and PDP-11/03. User selectable on-board refresh and battery backup modes
CM-5004-624	24K \times 16	Same as above except capacity
CM-5004-632	32K \times 16	Same as above except capacity
CM-5004-816	16K \times 18	Same as above except capacity
CM-5004-824	24K \times 18	Same as above except capacity
CM-5004-832	32K \times 18	Same as above except capacity



in-5034

PDP*-11/04, 11/34 ADD-IN MEMORY CARD

MEMORY
SYSTEMS

Total hardware and software compatibility with PDP-11/04 and PDP-11/34

16K, 32K, 48K, or 64K words × 18 bits per board storage capacity

Single hex height card contains all address and control circuitry

8K and 16K MOS RAMs provide high density memory with low system cost

On-board switch selectable addressing

On-board parity checking and generation

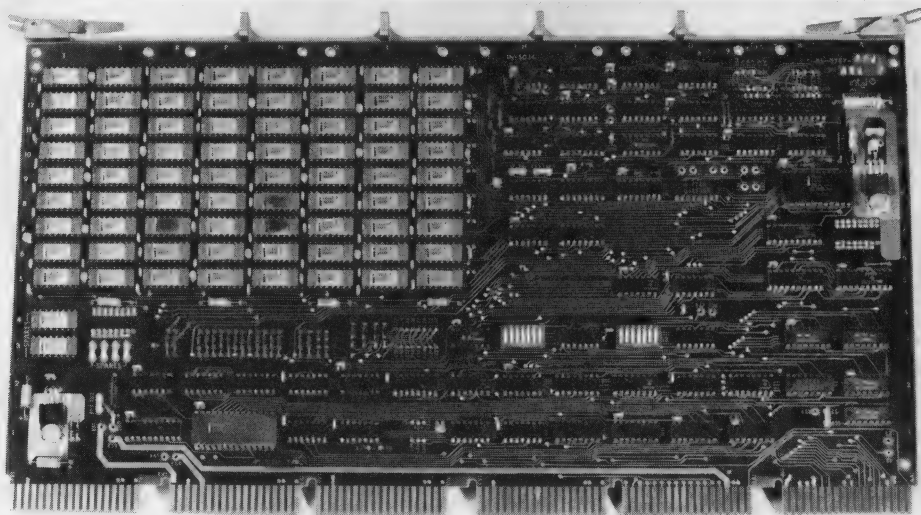
On-board control status register (CSR)

Battery backup capability

Low power dissipation for higher system reliability

Spare on-board memory chips

The Intel in-5034 PDP-11/04, 11/34 Add-In Memory Card is a plug-compatible memory module designed for use with any DEC* PDP-11/04 or PDP-11/34 modified Unibus* slot. The complete in-5034 memory system, with all address and control circuitry, is contained on a single hex height printed circuit card requiring only one modified Unibus slot. All system components are fully hardware and software compatible with PDP-11 systems and may be installed, without change or modification to the DEC software, CPU, memory bus, or input/output structure. High density memory is provided by 16K dynamic MOS RAM components, and is expandable in 16K-word increments to 64K words. High speed 600-nanosecond read and write cycle times allow maximum utilization of modified Unibus throughput. The system provides on-board parity checking and generation and an on-board control status register (CSR). The parity check and the CSR function perform for the in-5034 memory the equivalent of DEC's parity controller module function. Dual-in-line package (DIP) switches on the module select the desired Unibus address ranges and provide the addressing inputs required to expand memory capacity to 128K words. Two pre-tested memory devices are plugged into on-board sockets for use as spares to replace any failing memory devices in the field. Provisions are included on the card to accept external battery backup voltage inputs. The in-5034 switches to refresh cycles upon detection of a power failure, and retains memory content when provided +5V, +15V, and -15V battery backup voltages. The system is also designed for low power dissipation and consumption, resulting in improved system reliability.



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FUNCTIONAL DESCRIPTION

The CM-5034 semiconductor memory module consists of a single hex-height printed circuit card specifically designed to plug into a modified Unibus slot, and containing all circuitry required for memory operation, including data circuitry, address circuitry, mode enable and byte control logic, timing logic, control logic, refresh control circuitry, a control status register, a memory storage area, and a parity generator and checker. All operating sequences are controlled by processor supplied signals and by internally generated response signals sent to the processor from the memory. All system components are engineered to meet or exceed the specifications of similar DEC components. A simplified block diagram of the in-5034 memory card is shown in Figure 1.

Compatibility

The in-5034 is specifically designed for use with the DEC PDP-11 family of computer systems, and is fully compatible with all PDP-11/04 and PDP-11/34 computers. The CM-5034 memory module consists of one modified Unibus compatible printed circuit card assembly that plugs directly into a single system unit card slot. The system unit slot may be any of slots 2 through

8 of PDP-11/34 or either of slots 2 or 3 of PDP-11/04, as shown in Figure 2. The in-5034 uses cables and interface control, address, and data signals identical to those used in DEC memory modules. The unit may be installed in the DEC central processing unit (CPU) memory cabinet without change or modification to the DEC software, CPU, memory bus, or I/O structure. Jumper options are provided to select compatibility with either the core or semiconductor memory, to select or deselect the battery backup capability, and to enable or disable the control status register. All other system voltages, currents, timing, and I/O signal requirements are compatible with both the PDP-11/04 and PDP-11/34.

Capacity

Each memory card has a basic maximum capacity of 64K words by 18 bits, with one word consisting of two 8-bit data bytes (upper and lower) plus one parity bit per byte, i.e., 16 bits plus two parity bits per card. The card may be depopulated to provide 16K, 32K or 48K words of storage, as required. The storage area in the memory consists of 72 Intel 8K or 16K dynamic N-channel MOS RAM silicon gate memory chips. The 8K memory chip has a capacity of 8K words by one bit; the 16K, a capacity of 16K words by one bit. The in-5034 memory capacity may be expanded in 16K-word increments to a total of

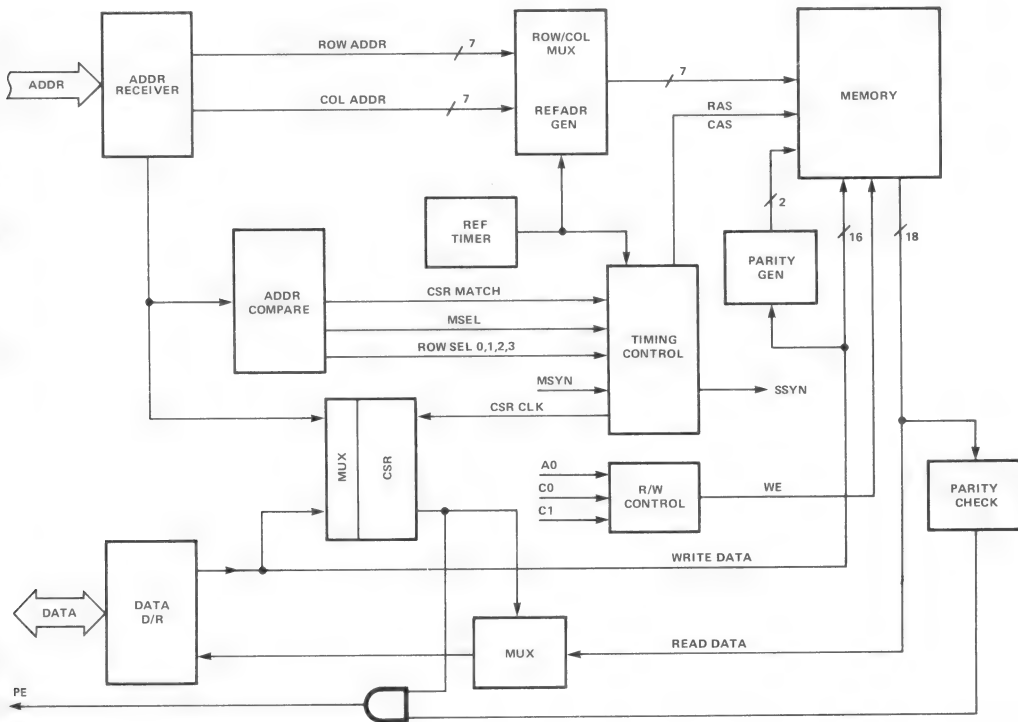


Figure 1. in-5034 Memory/Card Block Diagram

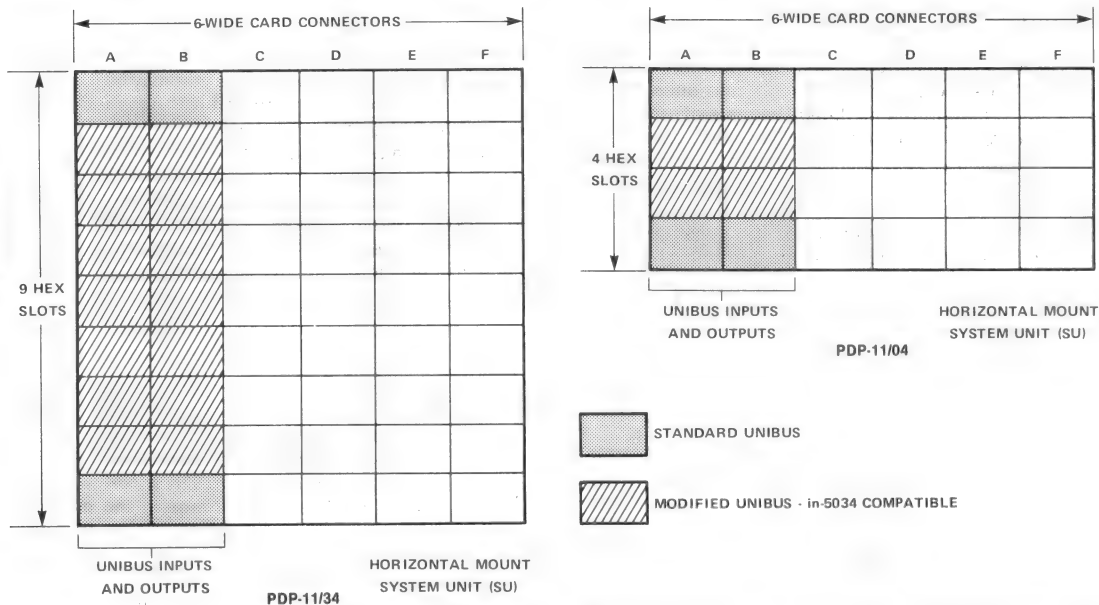


Figure 2. in-5034 Installation in PDP-11/34 and PDP-11/04 System Unit Card Slots

64K words. However, use of a total memory capacity exceeding 28K words requires the use of a DEC-supplied memory management unit.

Addressability

The address range for each module is set by on-board dual-in-line package (DIP) switches. The memory module starting address is selectable to any 8K boundary and the ending address is selectable to any 4K boundary. Each memory module provides addressing inputs to allow expansion to 128K words, although normally the upper 8K of address space must be deselected for I/O device and register addresses. A DEC memory management unit is required when the total system memory is expanded beyond 28K words. The control status register address of each memory board is determined by its starting address (set by DIP switches).

SPECIFICATIONS

Storage Capacity

16K, 32K, 48K, or 64K words per card

Word Length

16 bits plus 2 parity bits

Performance

Cycle Time — 600 ns max

Access Time

Read: 410 ns max

Write: 320 ns max

Reliability

The in-5034 is designed for low power dissipation. When operating at full speed in a PDP-11/04 or PDP-11/34, the 64K in-5034 dissipates 87 BTUs/hour, in standby 43 BTUs/hour, and in the battery backup mode 17 BTUs/hour, resulting in a cooler running system, an increased margin for power supply operation, and improved system reliability. Since the in-5034 dissipates less power than the equivalent DEC core or semiconductor memory, no special provisions are necessary for cooling. Each memory card is fully tested in a temperature cycling environment. Because of the 100% burn-in performed on each card, the user is assured of receiving Intel's proven quality and reliability. In addition, all Intel compatible products are covered by a one-year Intel warranty.

Operational Modes

Read

Write

Read byte

Write byte

Interface Characteristics

Interface — Modified Unibus compatible, 1 bus load

Address Input — 18 binary lines (single ended)

Data Input/Output — 18 bidirectional lines (single ended)

Control Input — 3 lines (single ended)

Control Output — 1 line (single ended)

Physical Characteristics

Width — 15.4 in. (39.1 cm)
Height — 0.374 in. (0.09 cm)
Depth — 8.5 in. (21.6 cm)
Weight — Less than 3 lb (1.3 kg)

Electrical Characteristics**DC Power Requirements**

Active	Standby	Battery Backup
$V_{CC} + 5V \pm 5\%$ at 2A	2A	0.5A
$V_{DD} + 15V^1 \pm 5\%$ at 0.7A	0.1A	0.1A
$V_{DD} + 20V^2 \pm 5\%$		
$V_{BB} - 15V \pm 5\%$ at 30 mA	20 mA	20 mA
Notes 1. Semiconductor backplane 2. Core Backplane		

Environmental Characteristics

Temperature — 0°C to 50°C operating ambient, -40°C to +125°C non-operating

Relative Humidity — Up to 90% with no condensation

Altitude — 10,000 ft max, operating; 50,000 ft max, non-operating

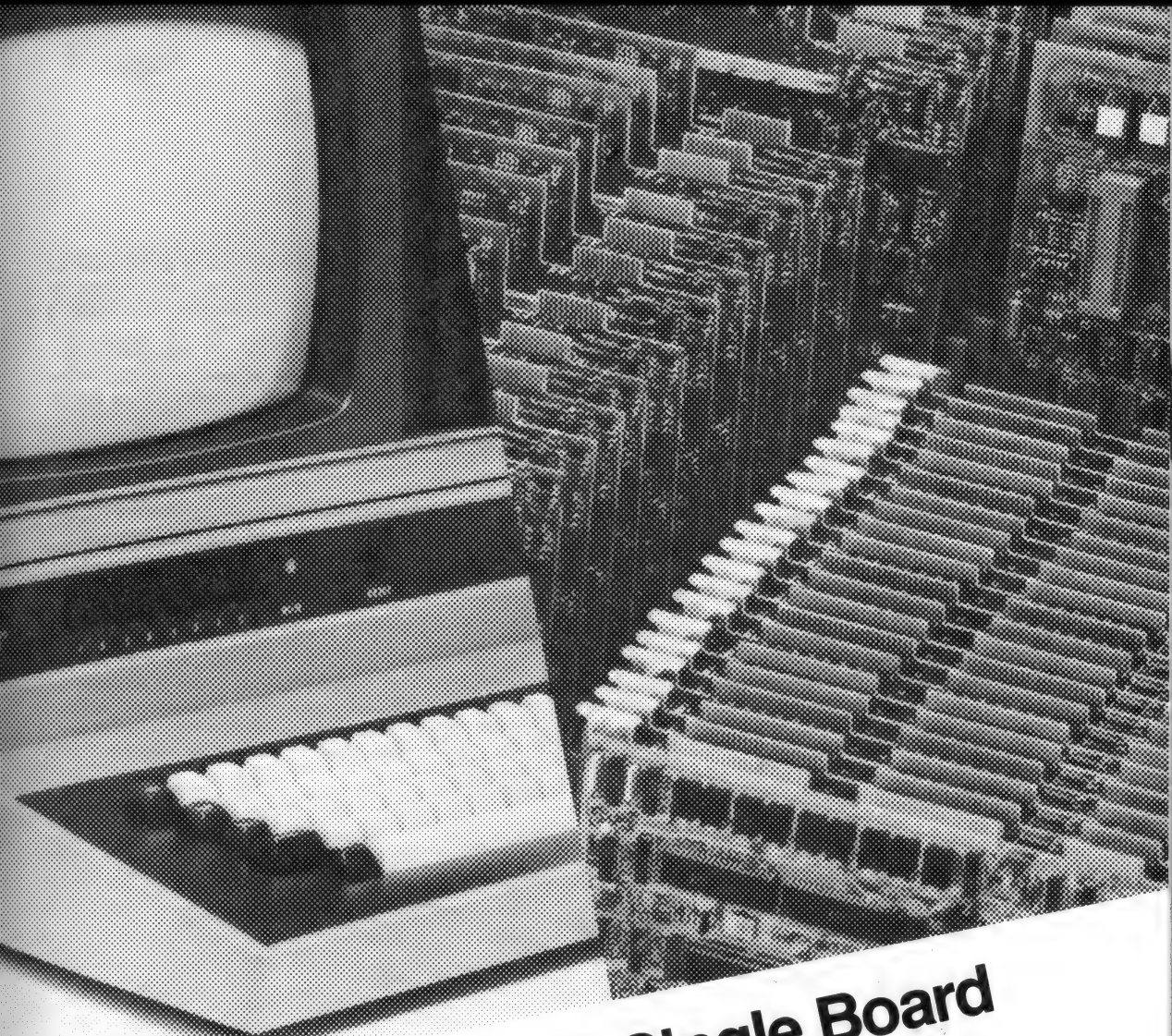
Reference Manuals

TM-5034-000 — in-5034 Technical Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative.

ORDERING INFORMATION

Model	Capacity	Description
CM-5034-816	16K × 18	Add-in memory card for PDP-11/04 and PDP-11/34
CM-5034-832	32K × 18	Same as above except capacity
CM-5034-848	48K × 18	Same as above except capacity
CM-5034-864	64K × 18	Same as above except capacity



4 Single Board Computers

SINGLE BOARD COMPUTERS

INTRODUCTION

The nucleus of the OEM computer product line is formed by the iSBC 80 single board computers and System 80 packaged systems. Each Intel single board computer provides all the resources of a full computer (i.e., CPU, read/write memory, read only memory, parallel I/O, and serial I/O) on a single printed circuit board. The System 80/10 and 80/20-4 extend these capabilities into low cost, fully packaged, RETMA rack-mountable computers. The Intel single board computers and systems are supported by a complete line of memory, parallel and serial digital I/O, analog I/O expansion boards, and peripheral and DMA controllers, all of which are all compatible with the standard Intel bus — the MULTIBUS. This section provides information and specifications for Intel's iSBC single board computers, as well as the iSBC 310 High Speed Mathematics Unit.

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iSBC 80/20 and iSBC 80/20-4 Single Board Computers	4-19
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iSBC 310 High Speed Mathematics Unit	4-34



iSBC 80/04 SINGLE BOARD COMPUTER

8085 CPU used as central processor

256 bytes of static read/write memory

Sockets for 4K bytes of erasable reprogrammable or masked read only memory

22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Optimized for stand-alone applications with provisions for on-board +5V regulator, heat sink, and mounting holes for attachment to user's equipment

Programmable 14-bit binary timer

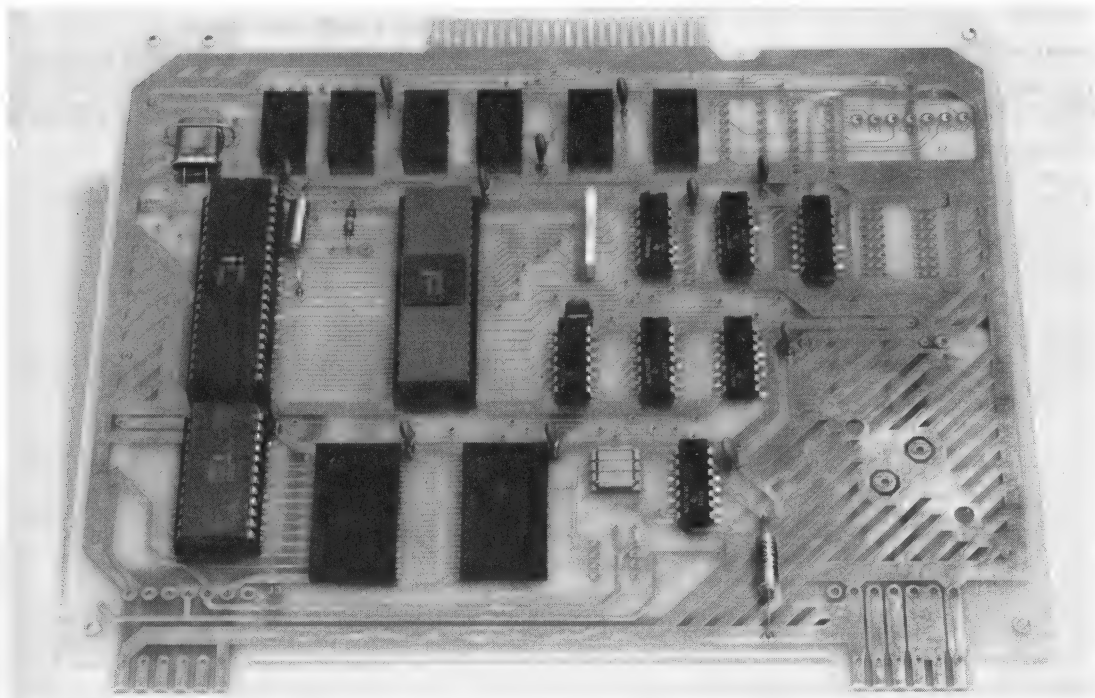
TTL serial I/O interface with hole patterns for RS232C line drivers and receivers

Four-level vectored interrupt

Upward compatibility with iSBC 80/05

Single +5V power supply

The iSBC 80/04 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/04 is a complete computer system on a single 6.75 x 7.85-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, and programmable timer all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085 CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/04. The 8085 CPU is directly software compatible with the popular Intel 8080A CPU. The 8085 contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of iSBC 80/04 functional components is shown in Figure 1.

Memory Addressing

The 8085 CPU has a 16-bit program counter which allows addressing of up to 65,536 bytes of memory. An external stack, located within any portion of iSBC 80/04 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/04 contains 256 bytes of read/write memory using the Intel 8155 RAM/IO/Timer. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2316E masked ROMs. Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 8708 EPROMs or Intel 8308 masked ROMs.

Parallel I/O Interface

The iSBC 80/04 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155

RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Stand-Alone Applications

The iSBC 80/04 is designed to be a cost-effective solution for applications requiring a self-contained computer on a single board without the need for external memory or I/O options. In order to help minimize power supply cost in small systems, the iSBC 80/04 includes provision for an on-board +5V regulator allowing unregulated voltage to be connected directly on the board. Regulated DC voltages are applied to the board through two 12-pin edge connectors which mate with flat, woven, or round cables. The iSBC 80/04 also includes pins that will accept MOLEX-type connectors for connection of regulated DC voltages. Mounting holes are provided in the corners of the iSBC 80/04 board which permit direct attachment to the user's equipment, thereby eliminating the need for cardcage and back-plane.

Compatibility with iSBC 80/05

The iSBC 80/04 is fully upward compatible with the iSBC 80/05 Single Board Computer. Pin assignments for parallel I/O, serial I/O, and regulated DC voltages are

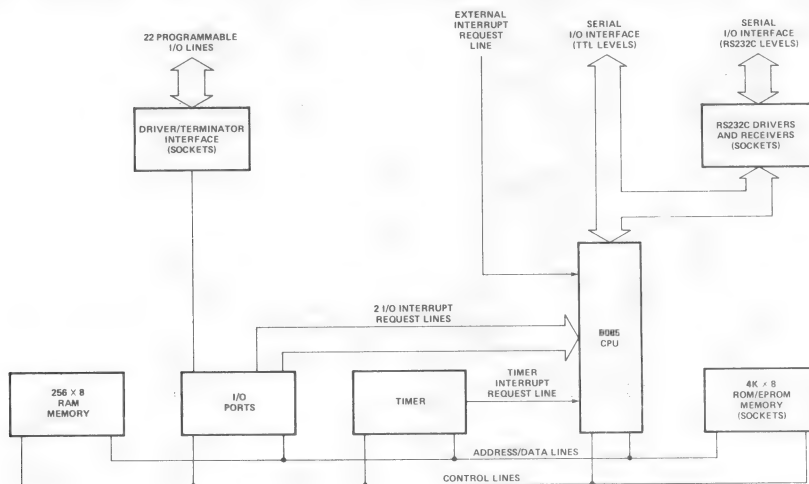


Figure 1. iSBC Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X ^{1,3}
4	3	X		X		X ^{2,3}

Notes

- Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
- Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.
- If both ports 1 and 2 are used in "latched & strobed" mode, they must be both input or both output ports.

Table 1. Input/Output Port Modes of Operation

identical to those of the ISBC 80/05. Additionally, software developed for the ISBC 80/04 will execute directly in the ISBC 80/05. In addition to the ISBC 80/04 features, the ISBC 80/05 contains a total of 512 bytes of read/write memory, allows for expansion of memory and I/O capacity, and provides full MULTIBUS arbitration control for multimaster applications.

Programmable Timer

The ISBC 80/04 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO-Timer. The systems designer simply configures the timer via software to meet system requirements. Whenever a given timer delay is needed, software commands to the programmable timer select the desired functions. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out remains high until one-half the count has been completed, and goes low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Table 2. Programmable Timer Functions

Serial I/O Interface

The ISBC 80/04 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085 CPU. These functions are controlled exclusively by software through execution of the 8085 RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the ISBC 80/04 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible, and hole patterns are provided on the board for optional installation of RS232C line drivers and receivers.

Interrupt Capability

The ISBC 80/04 takes advantage of the powerful interrupt processing capability of the 8085 CPU. Interrupt requests are routed to four interrupt inputs of the 8085 CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 26₁₆, RST 7.5: 3C₁₆, RST 6.5: 34₁₆, RST 5.5: 2C₁₆). A single 8085 jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085 CPU.

Interrupt Generation — The ISBC 80/04 accepts interrupts from four sources. An interrupt is automatically generated by the programmable interval timer/event counter upon completion of the selected function. Two interrupts are automatically generated by the I/O ports section of the 8155 when ports 1 or 2 of the 8155 are programmed to operate in the "latched and strobed" mode (see Table 1). The fourth interrupt source is available to the user and should be used to inform the 8085 CPU of catastrophic errors such as power failure. This user-defined source is connected to the trap input of the 8085 CPU.

Systems Development Capability

The development cycle of the iSBC 80/04-based products may be significantly reduced using an Intel microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/04 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/04.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intel microcomputer development system option. PL/M provides the

capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intel system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — $2.03 \mu\text{s}$, $\pm 0.1\%$

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — 0-0FFF_H

RAM — 3F00_H

Memory Capacity

ROM/EPROM — 4K bytes (sockets only)

RAM — 256 bytes

I/O Addressing

On-Board Programming I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 3 & 4	8155 Ports	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Serial Communications Characteristics

SID and SOD functions of the 8085 CPU are used for serial I/O. Controlled by software through RIM and SIM instructions of the 8085 CPU. Baud rate determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085 CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Condition	Interrupt Input	Memory Address	Priority	Type
User-defined	TRAP	24 ₁₆	Highest	Non-maskable
Timer	RST 7.5	3C ₁₆	↑	Maskable
I/O Port 2	RST 6.5	34 ₁₆	↓	Maskable
I/O Port 1	RST 5.5	2C ₁₆	Lowest	Maskable

Timer

Input Frequency Reference — $122.88 \text{ kHz} \pm 0.1\%$ (8.14 μs period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter	
	Min	Max
Programmable pulse	8.14 μs	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μs	133.33 ms

Interfaces

Parallel I/O — All signals TTL compatible

Interrupt Request — All TTL compatible (active-low)

Serial I/O — TTL; hole patterns available for user installation of RS232C line drivers and receivers

System Clock (8085 CPU)

$1.996 \text{ MHz} \pm 0.1\%$

Connectors

Interface	Pins (no.)	Center (in.)	Mating Connectors ¹
Voltages	+5V, +12V, -5V ²	12 double-sided	CDC VPB01E06D00A1
		7 single-sided	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 09-50-0106 Pin Molex 15-04-0219 Key AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key
	+5V, -12V ³	12 double-sided	CDC VPB01E06D00A1
		7 single-sided	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key AMP 87149-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key
	Unregulated +5V	2 single-sided	Molex 09-65-1021 Connector Molex 09-50-7021 Connector Molex 08-50-0106 Pin
			AMP 87194-1 Connector AMP 2-87025-5 Connector AMP 87023-1 Pin
Parallel I/O	50 double-sided	0.1	3M 3416-000 (flat cable) or TI H312125 (round cable)
Serial I/O	7 single-sided	0.156	Molex 09-65-1021 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 87023-1 Pin AMP 87116-2 Key

Notes

- Connectors and pins from a given vendor may only be used with connectors and pins from the same vendor.
- A single 86-contact edge-on connector (CDC VPB01E43A00A1) may be used to connect the two groups of regulated voltages (i.e., +5V, +12V, -5V, and +5V, -12V).
- Required only when RS232C line drivers and receivers are used.

Line Drivers and Terminators

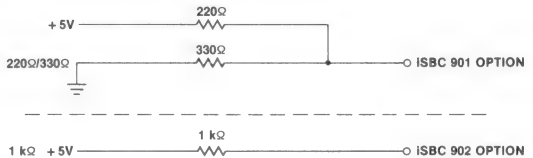
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the ISBC 80/04:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220Ω/330Ω divider and 1 kΩ pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the ISBC 80/04:

RS232C Driver — National DS1488 or TI SN75188

RS232C Receiver — National DS1490 or TI SN75189

Sockets

Sockets may be installed in the hole patterns provided for the RS232C drivers and receivers. The following sockets are compatible with the ISBC 80/04: TI C93-14-02 and SCANBE US-2-14-160-N-B.

Compatible Voltage Regulator

National LM 323 — 3A, 5V Positive Regulator

Fairchild μA7805 KM — 1A, 5V Positive Regulator

Compatible Heat Sink

IERC — LA Series or

AAVID Engineering, Inc. — Series 5051

Physical Characteristics

Width — 7.85 in. (19.94 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 6.0 oz (169.9 gm)

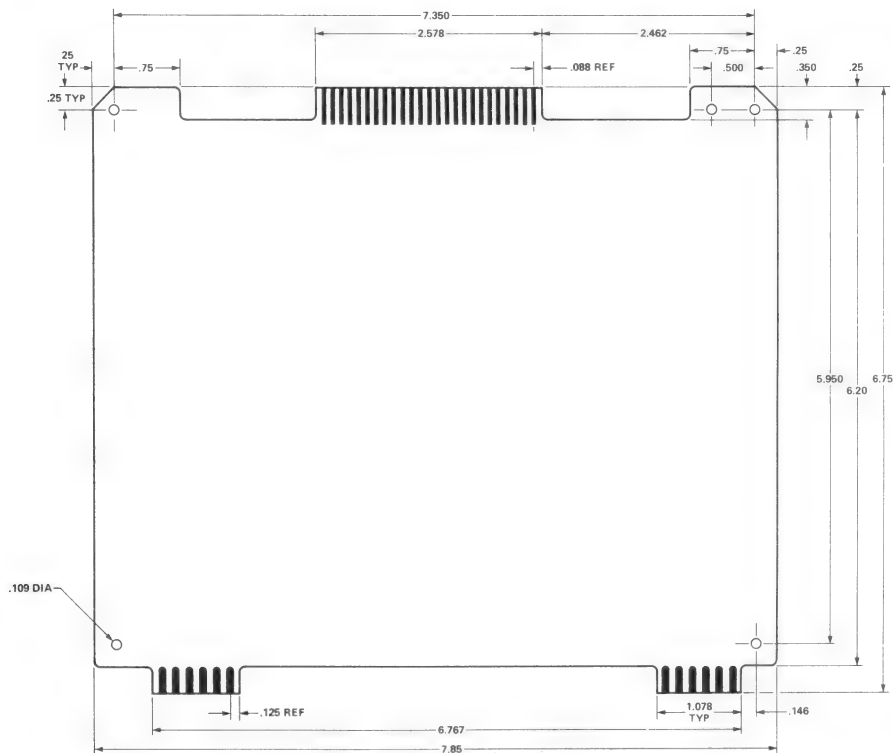


Figure 2. ISBC 80/04 Dimensions

Electrical Characteristics

DC Power Requirements

Voltage ($\pm 5\%$)	Without PROM ¹ (max)	With 2716 EPROM ² (max)	With 8708 EPROM ³ (max)
$V_{CC} = +5V$	$I_{CC} = 600 \text{ mA}$	1.45A	1.25A
$V_{DD} = +12V$ ⁴	$I_{DD} = 0$	7 mA ⁵	137 mA
$V_{BB} = -5V$ ⁴	$I_{BB} = 0$	0	90 mA
$V_{AA} = -12V$ ⁵	$I_{AA} = 0$	23 mA ⁵	23 mA ⁵

Notes

- Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
- With two Intel 2716 EPROMs and 220 Ω /330 Ω terminators installed for 22 input ports; all terminator inputs low.
- With two Intel 8708 EPROMs and 220 Ω /330 Ω terminators installed for 22 input ports; all terminator inputs low.
- Required for 8708 EPROMs.
- Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manuals

9800482 — ISBC 80/04 Hardware Reference Manual
(NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/04	Single board computer



iSBC 80/05 SINGLE BOARD COMPUTER

8080 CPU used as central processor

512 bytes of static read/write memory

Sockets for 4K bytes of erasable reprogrammable or masked read only memory

22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Full MULTIBUS control logic allowing up to 16 masters to share system bus

Programmable 14-bit binary timer

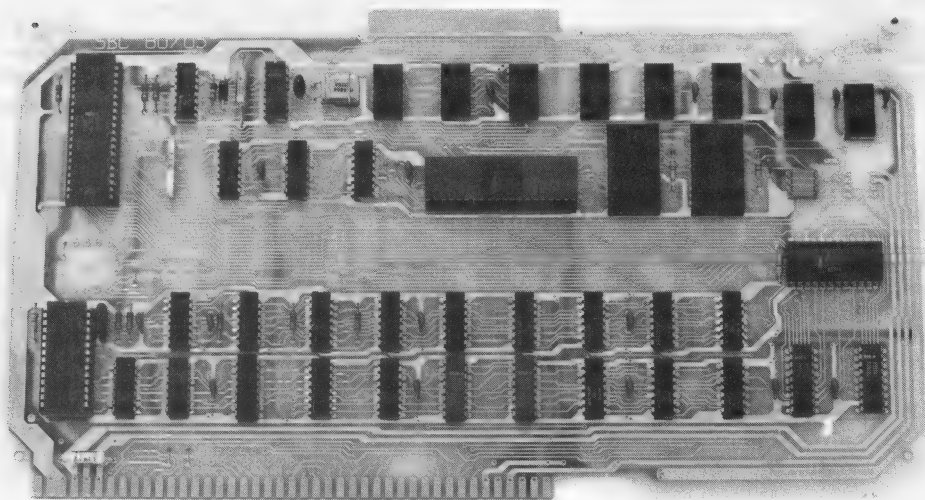
TTL serial I/O interface with sockets for RS232C line drivers and receivers

Four-level vectored interrupt

Fully compatible with optional iSBC expansion boards and peripherals

Single +5V power supply

The iSBC 80/05 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/05 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, programmable timer, MULTIBUS control logic, and bus expansion buffers all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085 CPU, fabricated on a single LSI chip, is the central processor for the ISBC 80/05. The 8085 CPU is directly software compatible with the popular Intel 8080A CPU. The 8085 contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of ISBC 80/05 functional components is shown in Figure 1.

Memory Addressing

The 8085 CPU has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The ISBC 80/05 contains 512 bytes of read/write memory using Intel's low power static RAMs. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 2316E masked ROMs. Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 8708 EPROMs or Intel 8308 masked ROMs.

Parallel I/O Interface

The ISBC 80/95 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to con-

figure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 40-pin edge connector that mates with flat, woven, or round cable.

Multimaster Capability

The ISBC 8085 is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share systems tasks with communication over the system bus), the ISBC 80/05 provides full MULTIBUS arbitration control logic. This control logic allows up to three bus masters (i.e., any combination of ISBC 80/05, ISBC 80/20, DMA controller, diskette controller, etc.) to share the system bus in serial (daisy-chain) priority fashion, and up to 16 masters may share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the ISBC 80/05 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and for transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to

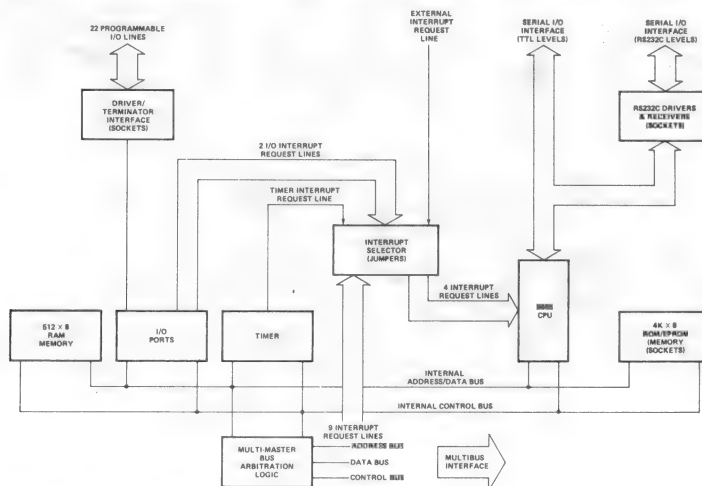


Figure 1. ISBC 80/05 Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X ^{1,3}
4	3	X		X		X ^{2,3}
Notes						
1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.						
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.						
3. If both ports 1 and 2 are used in "latched and strobed" mode, they must be both input or both output ports.						

Table 1. Input/Output Port Modes of Operation

gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timer

The ISBC 80/05 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO/Timer. The system designer simply configures the timer via software to meet system requirements. Whenever a given time delay is needed, software commands to the programmable timer select the desired function. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Serial I/O Interface

The ISBC 80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085 CPU. These functions are controlled exclusively by software through execution of the 8085 RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the ISBC 80/05 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible and sockets are provided on the board for optional connection of RS23C line drivers and receivers.

Interrupt Capability

The ISBC 80/05 takes advantage of the powerful interrupt processing capability of the 8085 CPU. Interrupt requests are routed to the four interrupt inputs of the 8085 CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 24₁₆, RST 7.5: 3C₁₆, RST 6.5: 34₁₆, RST 5.5: 2C₁₆). A single 8085 jump

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out will remain high until one-half the count has been completed, and go low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Table 2. Programmable Timer Functions

instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085 CPU.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the ISBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combinations boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding sin-

gle or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Systems Development Capability

The development cycle of iSBC 80/05-based products may be significantly reduced using an Intel microcomputer development system. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/05 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/05.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intel microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intel microcomputer system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 2.03 μ s, $\pm 0.1\%$

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — 0-0FFF_H

RAM — 3E00_H

Memory Capacity

On-Board ROM/EPROM — 4K bytes (with Intel 2716) or 2K bytes (with Intel 8708)

On-Board RAM — 512 bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combination of RAM, ROM, and PROM

I/O Addressing

On-Board Programmable I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 Ports 3 & 4	8155 Port	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Note

The iSBC 80/05 may be expanded to 1102 programmable input/output lines by using optional iSBC 80 I/O boards.

Serial Communications Characteristics

SID and SOD functions of the 8085 CPU are used for serial I/O. They are controlled by software through RIM

and SIM instructions of the 8085 CPU. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085 CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Interrupt Input	Memory Address	Priority	Type
TRAP	2416	Highest	Non-maskable
RST 7.5	3C16	\updownarrow	Maskable
RST 6.5	3416		Maskable
RST 5.5	2C16		Maskable
		Lowest	

Timer

Input Frequency Reference — 122.88 kHz $\pm 0.1\%$ (8.14 μ s period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter	
	Min	Max
Programmable pulse	8.14 μ s	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μ s	133.33 ms

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Request — All TTL compatible (active-low)

Serial I/O — TTL; sockets available for RS232C line drivers and receivers

System Clock (8085 CPU)

1.996 MHz $\pm 0.1\%$

Connectors

Interface	Lines (qty)	Centers (in.)	Mating Connector
Bus	50 double-sided	0.156	CDC VPB01E43A00A1
Parallel I/O	50 double-sided	0.1	3M 3415-000 or TI H312125
Serial I/O ¹	7 single-sided	0.1	Molex 09-65-1071 Connector Molex 09-50-7071 Connector Molex 08-50-0106 Pin Molex 15-04-0219 Key
			AMP 87194-6 Connector AMP 3-87025-4 Connector AMP 878023-1 Pin AMP 87116-2 Key

Note

1. Connectors and pins from one vendor may only be used with connectors and pins from the same vendor.

Line Drivers and Terminators

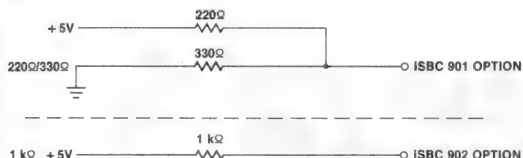
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/05:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220 Ω /330 Ω divider and 1 k Ω pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the iSBC 80/05:

RS232C Driver — National DS1488 or TI SN75188

RS232C Receiver — National DS1490 or TI SN75189

Physical Characteristics

Width — 12.00 in. (30.49 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12.0 oz (339.8 gm)

Electrical Characteristics

DC Power Requirements

Voltage ($\pm 5\%$)	Without PROM ¹ (max)	With 2716 EPROM ² (max)	With 8708 EPROM ³ (max)
$V_{CC} = +5V$	$I_{CC} = 1.80 \text{ mA}$	2.65A	2.45A
$V_{DD} = +12V$ ⁴	$I_{DD} = 0$	7 mA ⁵	137 mA
$V_{BB} = -5V$ ⁴	$I_{BB} = 0$	0	90 mA
$V_{AA} = -12V$ ⁵	$I_{AA} = 0$	23 mA ⁵	23 mA ⁵

Notes

- Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
- With two Intel 2716 EPROMs and 220 Ω /330 Ω terminators installed for 22 input ports; all terminator inputs low.
- With two Intel 8708 EPROMs and 220 Ω /330 Ω terminators installed for 22 input ports; all terminator inputs low.
- Required for 8708 EPROMs.
- Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C.

Reference Manuals

9800483 — iSBC 80/05 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/05	Single board computer



iSBC 80/10A SINGLE BOARD COMPUTER

iSBC
COMPUTERS

8080A CPU used as central processor

1K bytes of read/write memory

**Sockets for 8K bytes of programmable
or masked read only memory**

**48 programmable parallel I/O lines with
sockets for interchangeable line drivers
and terminators**

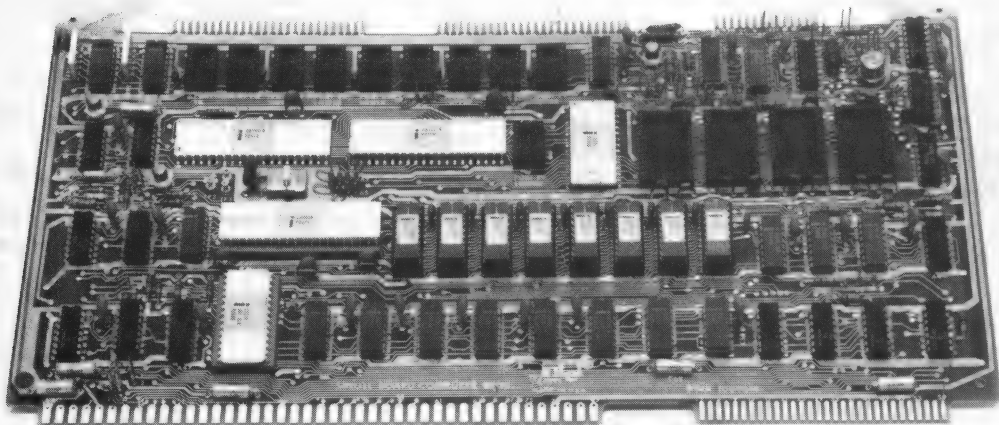
**Programmable synchronous/asyn-
chronous communications interface
with selectable teletypewriter or RS232C
compatibility**

Six interrupt request lines

**Compatible with optional memory and
I/O expansion boards**

**Bus drivers for memory and I/O
expansion**

The iSBC 80/10A is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/10A is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, bus control logic, and drivers all reside on the board.



Parallel I/O Interface

The ISBC 80/10A contains 48 programmable parallel I/O lines implemented using two Intel 8255A programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable or round cable.

Serial I/O Interface

A programmable communications interface using the Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper selectable TTY or

and framing error detection are all incorporated in the USART. The inclusion of jumper selectable TTY or



Figure 1. ISBC 80/10A Block Diagram Showing Functional Components

RS232C compatible interfaces on the board, in conjunction with the USART, provides a direct interface to teletypes, CRTs, RS232 compatible cassettes, and asynchronous and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 25-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt Capability

Interrupt requests may originate from six sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38₁₆.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the ISBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or com-

bination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Real-Time Software

Intel's RMX/80 Real-Time Multi-Tasking Executive software, specifically designed for Intel iSBC 80 single board computers, provides the capability to monitor and control multiple asynchronous external events. The RMX/80 executive, which synchronizes and controls the execution of multiple tasks, resides in 2K bytes of on-board EPROM or ROM. Optional linkable and relocatable modules for teletypewriter and CRT control, a diskette file system, a high speed math unit, and analog subsystems are also available.

System Development Capability

The development cycle of iSBC 80/10A-based products may be significantly reduced using an Intel microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/10A system software. An optional diskette operating system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-80) option provides the capability of developing and debugging software directly on the iSBC 80/10A.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intel microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or

Port	Lines (qty)	Mode Of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	8	X		X		X ¹
4	8	X		X		
5	8	X		X		
6	4	X		X		
	4	X		X		

Notes
Port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level

FORTRAN-80 programming language is also available as a resident option of the Inteltec system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.95 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0—IFFF (using 2716 EPROMs or 2316E ROMs); 0—OFFF (using 8708 or 2758 EPROMs, or 8308 ROMs)

On-Board RAM — 3C00—3FFF

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 1K bytes

Off-Board Expansion — Up to 65,536 bytes using user specified combinations of RAM, ROM, and EPROM.

Note

ROM/EPROM may be added in 1K-byte (with 8708/2758/8038) or 2K-byte (with 2716/2316E) increments.

I/O Addressing

On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1	8255 No. 2	USART	USART
	1	2	3	4	5	6	No. 1 Control	No. 2 Control	Data	Control
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note

Expansion to 1128 programmable I/O lines can be accomplished using optional boards.

Serial Baud Rates

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)			
	Synchronous		Asynchronous (Program Selectable)	
			+ 16	+ 64
307.2	—	—	19200	4800
153.6	—	—	9600	2400
76.8	—	—	4800	1200
38.4	38400	—	2400	600
19.2	19200	—	1200	300
9.6	9600	—	600	150
6.98	6980	—	—	110
4.8	4800	—	300	75

Serial Communication Characteristics

Synchronous — 5–8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Single-level with on-board logic that automatically vectors processor to location 38₁₆ using a restart instruction (RESTART 7). Interrupt requests may originate from user specified I/O (2), the programmable peripheral interface (2), or USART (2).

INTERFACES

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C or a 20 mil current loop TTY interface (jumper selectable)

Interrupt Requests — All TTL compatible (active-low)

System Clock

2.048 MHz \pm 0.1%

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43D00A1 Wire-wrap
Parallel I/O (2)	50	0.1	3M 3415-000 or TI H312125 Flat Pins
Serial I/O	26	0.1	3M 3462-0001 or AMP 88106-1 Flat

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 14 oz (484.4 gm)

Electrical Characteristics

DC Power Requirements

Voltage ($\pm 5\%$)	Without EPROM ¹ (max)	8708 EPROM ² (max)	With 2758 or 2716 EPROM ³ (max)
$V_{CC} = +5V$	$I_{CC} = 2.9A$	4.0A	4.4A
$V_{DD} = +12V$	$I_{DD} = 150\text{ mA}$	400 mA	150 mA
$V_{BB} = -5V$	$I_{BB} = 2\text{ mA}$	200 mA	2 mA
$V_{AA} = -12V$	$I_{AA} = 175\text{ mA}^4$	175 mA ⁴	175 mA ⁴

Notes

- Does not include power required for optional ROM/EPROM, I/O drivers, and I/O Terminators.
- With four Intel 8708 EPROMs and 220 Ω /330 Ω terminators installed for 48 input lines; all terminator inputs low.
- With four Intel 2758 or four 2716 EPROMs and 220 Ω /330 Ω terminators installed for 48 input ports; all terminator inputs low.
- Required for RS232C drivers only.

Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 80/10A:

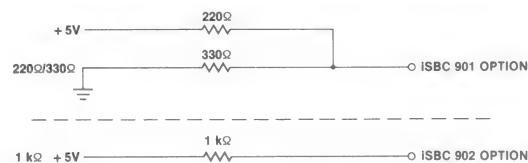
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Port 1 has 25 nA totem pole drivers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	25
Address	Tri-state	25
Commands	Tri-state	25

Environmental Characteristics

Operating Temperature — 0°C to 5°C

Equipment Supplied

iSBC 80/10A Single Board Computer
iSBC 80/10A Schematics

Reference Manuals

9800230 — iSBC 80/10 and iSBC 80/10A Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SBC 80/10A Single board computer



iSBC 80/20, iSBC 80/20-4 SINGLE BOARD COMPUTERS

8080A CPU used as central processor

2K bytes (iSBC 80/20) or 4K bytes (iSBC 80/20-4) of static read/write memory

Sockets for up to 8K bytes of erasable reprogrammable or masked read only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable synchronous/asynchronous RS232C compatible serial interface with fully software selectable baud rate generation

Full MULTIBUS control logic allowing up to 16 masters to share system bus

Two programmable 16-bit BCD and binary timers

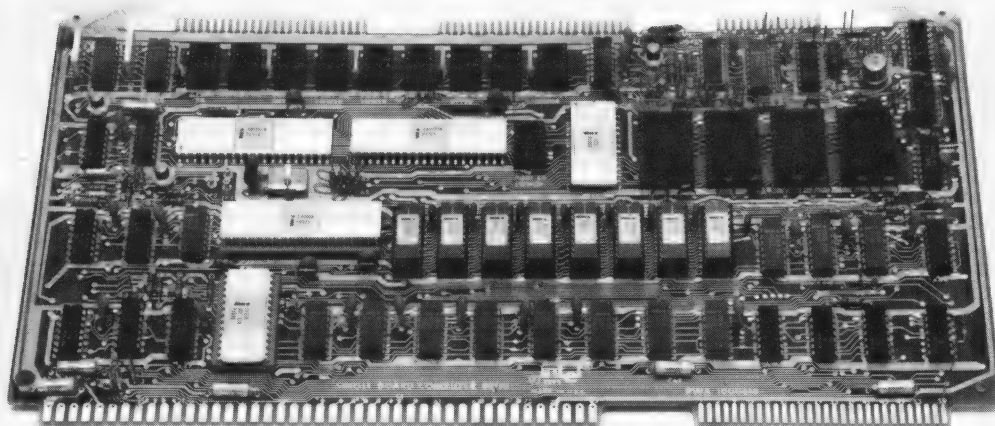
Eight-level programmable interrupt control

Compatible with optional memory and I/O expansion boards

Auxiliary power bus, memory protect, and power-fail interrupt control logic provided for battery backup RAM requirements

iSBC
COMPUTERS

Each iSBC 80/20 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. Each iSBC 80/20 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic, two programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on each board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for each ISBC 80/20. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum instruction execution time is 1.86 microseconds. A block diagram of ISBC 80/20 and ISBC 80/20-4 functional components is shown in Figure 1.

Memory Addressing

The 8080A has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The ISBC 80/20 contains 2K bytes and the ISBC 80/20-4 contains 4K bytes of static read/write memory using Intel low power static RAMs. All on-board RAM read and write operations are performed at maximum processor speed. Power for on-board RAM memory is provided on an auxiliary power bus, and memory protect logic is included, for battery backup RAM requirements. Sockets for up to 8K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 1K-byte increments using Intel 8708 erasable and electrically reprogrammable ROMs

(EPROMs) or Intel 8308 masked ROMs, or read only memory may be added in 2K-byte increments using Intel 2716 EPROMs or Intel 2316E masked ROMs. All on-board ROM read operations are performed at maximum processor speed.

Parallel I/O Interface

Each ISBC 80/20 contains 48 programmable parallel I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of the unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round cable.

Serial I/O Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on these boards. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., syn-

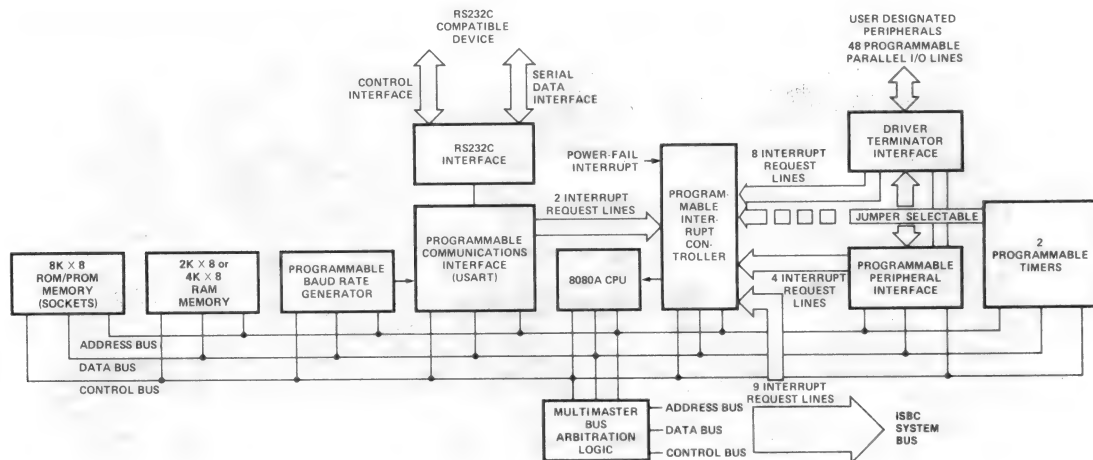


Figure 1. ISBC 80/20 and ISBC 80/20-4 Block Diagram Showing Functional Components

chronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable. The ISBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The ISBC 530 may be used to interface either ISBC 80/20 or ISBC 80/20-4 to teletypewriters or other 20 mA current loop equipment.

Multimaster Capability

Each ISBC 80/20 is a full computer on a single board with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the ISBC 80/20's provide full MULTIBUS arbitration control logic. This control logic allows up to three ISBC 80/20's or high speed controllers to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters may share the system bus with the addition of an external priority network. Once bus control is attained, a bus bandwidth of up to 5M bytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data words per second. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

Each ISBC 80/20 provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or outputs from the 8255 programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the ISBC 80/20 RS232C USART serial port. In utilizing either ISBC 80/20, the systems designer simply

Port	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X		
2	8	X	X	X	X		
3	4	X		X		X ¹	
	4	X		X		X ¹	
4	8	X	X	X	X		
5	8	X	X	X	X		
6	4	X		X		X ²	
	4	X		X		X ²	

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly".

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 2. Programmable Timer Functions

Interrupt Capability

Operation and Priority Assignments — An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers,

the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the interrupt mask register of the PIC.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Addressing — The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8080 jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation — Interrupt requests may originate from 26 sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and eight interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Power-Fail Control — Control logic is also included for generation of a power-fail interrupt which works in conjunction with the AC-low signal from iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compati-

ble expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Real-Time Software

Each iSBC 80/20 is totally compatible with Intel's RMX/80 Real-Time Multi-Tasking Executive. iSBC 80/20-based user programs (tasks) can take advantage of the RMX/80 executive to do all necessary scheduling, intertask communication, and memory space allocation. RMX/80 also provides standard I/O support software such as disk file handling, Intel analog board handling, and terminal handling.

System Development Capability

The development cycle of iSBC 80/20-based products may be significantly reduced using an Intel microcomputer development system. The resident macroas-

sembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/20 system software. An optional diskette operating System provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-80) option provides the capability of developing and debugging software directly on the iSBC 80/20.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intel microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTAN-80 programming language is also available as a resident option of the Intel system. The FORTAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.86 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0—0FFF (8708) or 0—1FFF (2716).

On-Board RAM — 2K bytes (iSBC 80/20) or 4K bytes (iSBC 80/20-4) ending on a 16K boundary (e.g., 3FFF_H, 7FFF_H, BFFF_H, ... FFFF_H).

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 2K bytes (iSBC 80/20) or 4K bytes (iSBC 80/20-4)

Off-Board Expansion — Up to 65,536 bytes in user specified RAM, ROM, and EPROM

Note

ROM/EPROM may be added in 1K or 2K byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1)

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6	E7	EB	EC	ED
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note

Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

Serial Communications Characteristics

Synchronous — 5–8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous
153.6	—	+ 16 + 64
76.8	—	9600 2400
38.4	38400	4800 1200
19.2	19200	2400 600
9.6	9600	1200 300
4.8	4800	600 150
2.4	2400	300 75
1.76	1760	150 —
		110 —

Note

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

Note

Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

Interrupts

Register Addresses (hex notation, I/O address space)

DA Interrupt request register
DA In-service register
DB Mask register
DA Command register
DB Block address register
DA Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Timers

Register Addresses (hex notation, I/O address space)

DF Control register
DC Timer 1
DD Timer 2

Note

Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference	Event Rate
1.0752 MHz \pm 0.1% (0.930 μ s period, nominal)	1.1 MHz max

Note

Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Programmable one-shot	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-wave rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Software triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Hardware triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

System Clock (8080A CPU)

2.1504 MHz \pm 0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/20.

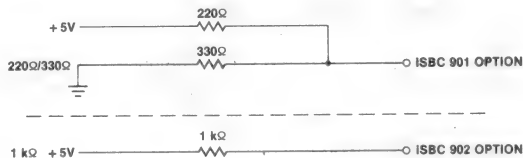
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 20 mA totem-pole bidirectional drivers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.26 cm)

Weight — 14 oz (397.6 gm)

Electrical Characteristics**DC Power Requirements**

Voltage ($\pm 5\%$)	Without PROM ¹ (max)	With 4KPROM ² (max)	With iSBC530 ³ (max)	RAM Only ⁴ (max)	With 8KPROM ⁵ (max)
V _{CC} = +5V	I _{CC} = 4.0A	4.9A	4.9A	1.1A	5.2A
V _{DD} = +12V	I _{DD} = 90mA	350 mA	450 mA	—	90 mA
V _{BB} = -5V	I _{BB} = 2 mA	180 mA	180 mA	—	2 mA
V _{AA} = -12V	I _{AA} = 20mA	20 mA	120 mA	—	20 mA

Notes

- Does not include power required for optional PROM, I/O drivers, and I/O terminators.
- With four 8707 EPROMs and 220 Ω /330 Ω input terminators installed for 32 I/O lines, all terminator inputs low.
- With four 8708 EPROMs, 220 Ω /330 Ω input terminators installed for 32 I/O lines, all terminator inputs low, and iSBC 530 Teletypewriter Adapter drawing power from serial port connector.
- RAM chips powered via auxiliary power bus current level given applies for iSBC 80/20 or iSBC 80/20-4.
- With four 8716 EPROMs and eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°C.

Reference Manuals

98-317C — iSBC 80/20, iSBC 80/20-4 Hardware Reference (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

iSBC
COMPUTERS

ORDERING INFORMATION

Part Number	Description
SBC 80/20	Single Board Computer with 2K bytes RAM
SBC 80/20-4	Single Board Computer with 4K bytes RAM

iSBC 80/30 SINGLE BOARD COMPUTER

iSBC
COMPUTERS

8085A CPU used as central processing unit

16K bytes of dual port dynamic read/write memory with on-board refresh

Sockets for up to 8K bytes of read only memory

Sockets for 8041/8741 Universal Peripheral Interface and interchangeable line drivers and line terminators

24 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable synchronous/asynchronous RS232C compatible serial interface with fully software selectable baud rate generation

Full MULTIBUS control logic allowing up to 16 masters to share the system bus

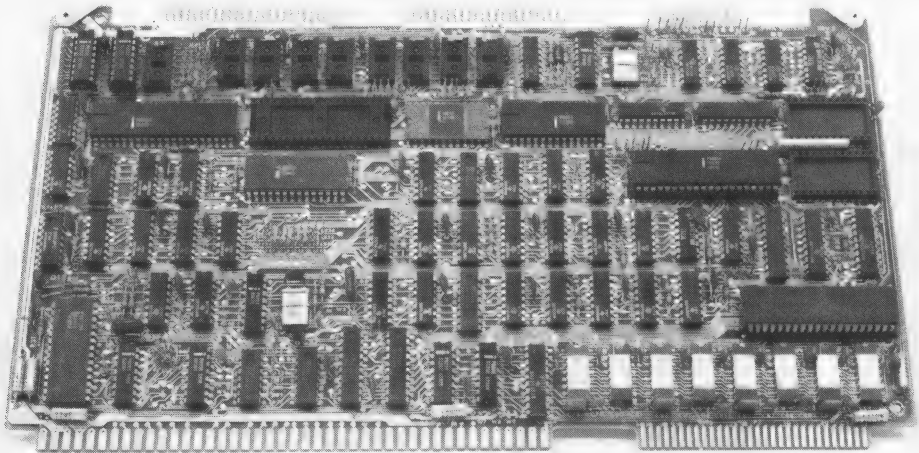
12 levels of programmable interrupt control

Two programmable 16-bit BCD or binary counters

Auxiliary power bus, memory protect, and power-fail interrupt control logic for RAM battery backup

Compatible with optional iSBC 80 CPU, memory, and I/O expansion boards

The iSBC 80/30 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical self-contained computer-based solutions for OEM applications. The iSBC 80/30 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, universal peripheral interface capability, I/O ports and drivers, serial communications interface, priority interrupt logic, programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on the board.



FUNCTIONAL DESCRIPTION

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the ISBC 80/30. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of ISBC 80/30 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Bus Structure

The iSBC 80/30 has an internal bus for all on-board memory and I/O operations and a system bus (i.e., the MULTIBUS) for all external memory and I/O operations. Hence, local (on-board) operations do not tie up the system bus, and allow true parallel processing when several bus masters (i.e., DMA devices, other single board computers) are used in a multimaster scheme. A block diagram of the iSBC 80/30 functional components is shown in Figure 1.

RAM Capacity

The iSBC 80/30 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 80/30 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the iSBC 80/30 or from any other bus master interfaced via the

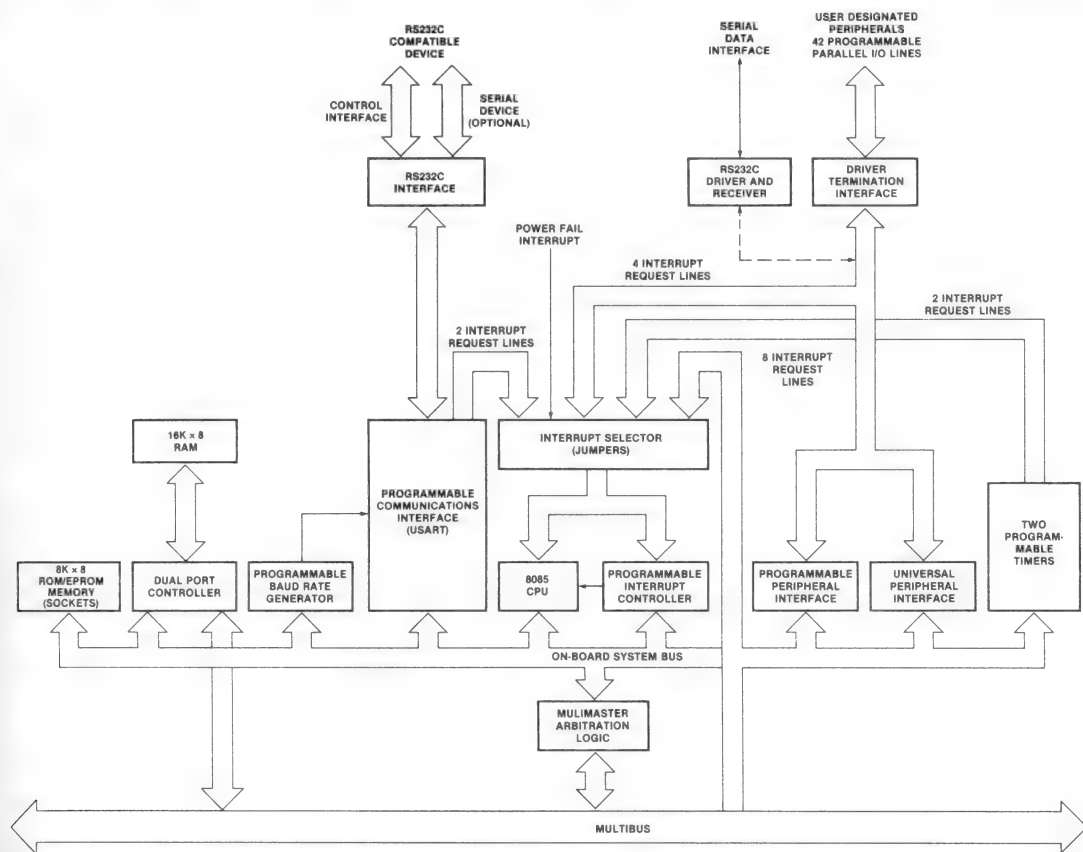


Figure 1. ISBC 80/30 Single Board Computer Block Diagram

MULTIBUS. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for any other concurrent operations (e.g., DMA data transfers) requiring the use of the MULTIBUS. Dynamic RAM refresh is accomplished automatically by the ISBC 80/30 for accesses originating from either the CPU or via the MULTIBUS. Memory space assignment can be selected independently for on-board and MULTIBUS RAM accesses. The on-board RAM, as seen by the 8085A CPU, may be placed anywhere within the 0- to 64K-address space. The ISBC 80/30 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to reserve 8K- and 16K-byte segments of on-board RAM for use by the 8085A CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory are provided on the ISBC 80/30 board. Read only memory may be added in 1K-byte increments up to a maximum of 2K bytes using Intel 8708 or 2758 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs; in 2K-byte increments up to a maximum of 4K bytes using Intel 2716 EPROMs or Intel 2316E masked ROMs; or in 4K-byte increments up to 8K bytes maximum using Intel 2332 ROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

Parallel I/O Interface

The ISBC 80/30 contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchange-

able I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Universal Peripheral Interface (UPI)

The ISBC 80/30 provides sockets for a user supplied Intel 8041/8741 Universal Peripheral Interface (UPI) chip and the associated line drivers and terminators for the UPI's I/O ports. The 8041/8741 is a single chip micro-computer containing a CPU, 1K bytes of ROM (8041) or EPROM (8741), 64 bytes of RAM, 18 programmable I/O lines, and an 8-bit timer. Special interface registers included in the chip allow the 8041 to function as a slave processor to the ISBC 80/30's 8085A CPU. The UPI allows the user to specify algorithms for controlling user peripherals directly in the chip, thereby relieving the 8085A for other system functions. The ISBC 80/30 provides an RS232C driver and an RS232C receiver for optional connection to the 8041/8741 in applications where the UPI is programmed to handle simple serial interfaces. For additional information, including 8041/8741 instructions, refer to the UPI-41 User's Manual.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the ISBC 80/30. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM By-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each

Port	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X ¹
	4	X		X			X ¹

Note

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 80/30 to teletypewriters or other 20 mA current loop equipment.

Multimaster Capability

The iSBC 80/30 is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 80/30 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/30's or other bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/30 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/30 provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, and to the 8041/8741 Universal Programmable Interface, or may be routed as inputs to the 8255A and 8041/8741 chips. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 80/30 RS232C USART serial port. In utilizing the iSBC 80/30, the systems

designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 2. Programmable Timer Functions

Interrupt Capability

The iSBC 80/30 provides vectored for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A CPU and represent the four highest priority interrupts of the iSBC 80/30. Requests are routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority) and each input generates a unique memory address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A jump instruction at each of these addresses then provides linkage to interrupt ser-

vice routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Request Generation — Interrupt requests may originate from 18 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers and by the universal periph-

eral interface, eight additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and two interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the ISBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating point arithmetic capabilities may be added by using the ISBC 310 High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and card-cages are available to support multiboard systems.

Real-Time Software

Intel's RMX/80 Real-Time Multi-Tasking Executive software, specifically designed for Intel ISBC 80 single board computers, provides the capability to monitor and control multiple asynchronous external events. The RMX/80 executive, which synchronizes and controls the execution of multiple tasks, is provided as a linkable and relocatable module requiring only 2K bytes of memory space. Optional linkable and relocatable modules for teletypewriter and CRT control, diskette file system, high speed math unit, and analog subsystems are also available.

System Development Capability

The development cycle of ISBC 80/30-based products may be significantly reduced using the Intellec series microcomputer development systems. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of ISBC 80/30 system software. An optional diskette operating system provides a relocating macroassembler, relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the ISBC 80/30.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the inteltec system. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 subset language specification. The FORTRAN-80 compiler produces relocatable object code that may be easily linked with other FORTRAN-80, PL/M, or assembly language program modules. This gives the user wide flexibility in developing software by using the best software tool for a particular functional module within the user's application.

piler produces relocatable object code that may be easily linked with other FORTRAN-80, PL/M, or assembly language program modules. This gives the user wide flexibility in developing software by using the best software tool for a particular functional module within the user's application.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.45 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-07FF (using 8708 or 2758 EPROMs or 8308 ROMs); 0-0FFF (using 2716 EPROMs or 2316E ROMs); 0-1FFF (using 2332 ROMs)

On-Board RAM — 16K bytes of dual port RAM starting on a 16K boundary. One or two 8K-byte segments may be reserved for CPU use only.

Memory Capacity

On-Board Read Only Memory — 8K bytes (sockets only)

On-Board RAM — 16K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM

Note

Read only memory may be added in 1K, 2K, or 4K-byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1)

Port	8255A				8041/8741		USART	
	1	2	3	Control	Data	Control	Data	Control
Address	E8	E9	EA	EB	E4 or E6	E5 or E7	EC	ED

I/O Capacity

Parallel — 42 programmable lines using one 8255A (24 I/O lines) and an optional 8041/8741 (18 I/O lines)

Serial — 2 programmable lines using one 8251A and an optional 8041/8741 programmed for serial operation

Note:

For additional information on the 8041/8741, refer to the UPI-41 User's Manual (Publication 9800504).

Serial Communications Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5—8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous
153.6	—	÷ 16 9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
2.4	2400	150 —
1.76	1760	110 —

Note

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Interrupts

Addresses for 8259A Registers (Hex notation, I/O address space)

DA Interrupt request register

DA In-service register

DB Mask register

DA Command register

DB Block address register

DA Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels routed to 8085A CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C	↕	Maskable
RST 6.5	34		Maskable
RST 5.5	2C		Maskable
		Lowest	

Timers

Register Addresses (Hex notation, I/O address space)

DF Control register

DC Timer 0

DD Timer 1

DE Timer 2

Note

Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference: 2.46 MHz \pm 0.1% (0.041 μ s period, nominal); 1.23 MHz \pm 0.1% (0.81 μ s period, nominal); or 153.60 kHz \pm 0.1% (6.51 μ s period nominal).

Note

Above frequencies are user selectable

Event Rate: 2.46 MHz max

Note

Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.63 μ s	427.1 ms	3.26 μ s	466.50 min
Programmable one-shot	1.63 μ s	427.1 ms	3.26 μ s	466.50 min
Rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-wave rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software triggered strobe	1.63 μ s	427.1 ms	3.26 μ s	466.50 min
Hardware triggered strobe	1.63 μ s	427.1 ms	3.26 μ s	466.50 min

Interfaces

MULTIBUS — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

System Clock (8085A CPU)

2.76 MHz \pm 0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

I/O Drivers— The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/30.

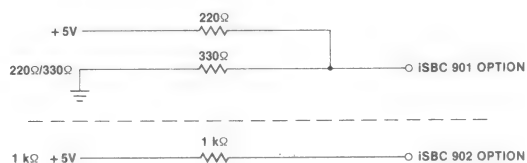
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 18 oz. (509.6 gm)

Electrical Characteristics**DC Power Requirements**

Configuration	Current Requirements			
	$V_{CC} = +5V$ $\pm 5\%(\text{max})$	$V_{DD} = +12V$ $\pm 5\%(\text{max})$	$V_{BB} = -5V$ $\pm 5\%(\text{max})$	$V_{AA} = -12V$ $\pm 5\%(\text{max})$
Without EPROM ¹	$I_{CC} = 3.5A$	$I_{DD} = 220 \text{ mA}$	$I_{BB} = -$	$I_{AA} = 50 \text{ mA}$
With 8041/8741 ²	3.6A	220 mA	—	50 mA
RAM only ³	350 mA	20 mA	2.5 mA	—
With iSBC 530 ⁴	3.5A	320 mA	—	150 mA
With 2K EPROM ⁵ (using 8708)	4.4A	350 mA	95 mA	40 mA
With 2K EPROM ⁵ (using 2758)	4.6A	220 mA	—	50 mA
With 4K EPROM ⁵ (using 2716)	4.6A	220 mA	—	50 mA
With 8K EPROM ⁵ (using 2332)	4.6A	220 mA	—	50 mA

Notes

- Does not include power required for optional EPROM/ROM, 8041/8741, I/O drivers, and I/O terminators.
- Does not include power required for optional EPROM/ROM, I/O drivers and I/O terminators.
- RAM chips powered via auxiliary power bus
- Does not include power required for optional EPROM/ROM, 8041/8741, I/O drivers, and I/O terminators. Power for iSBC 530 is supplied through the serial port connector.
- Includes power required for two EPROM/ROM chips, 8041/8741 and 220 Ω /330 Ω input terminators installed for 34 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800611 — iSBC 80/30 Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/30	Single Board Computer with 16K bytes RAM

iSBC 310 HIGH SPEED MATHEMATICS UNIT

Provides iSBC 80 high speed mathematical functions

Performs functions independently and concurrently with iSBC 80 single board computer functions

Fixed point integer arithmetic

- 16- and 32-bit format
- Multiply and divide
- Extended divide

Floating point arithmetic

- Intel standard 32-bit format
- Add, subtract, multiply, divide
- Square and square root

Compare and test operation

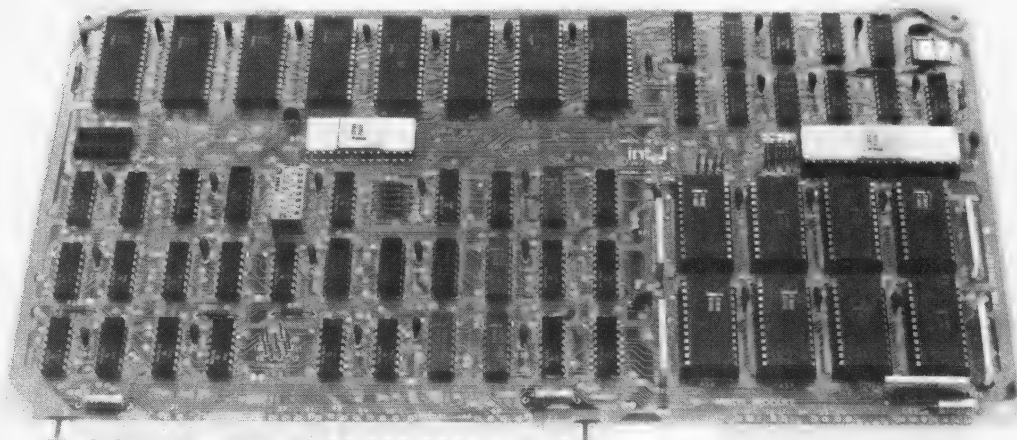
- Relative to zero
- Relative to floating point constant

Float-to-fix and fix-to-float conversions

Multimaster access — multiple masters may access iSBC 310 via system bus

Single +5V power requirement

The iSBC 310 High Speed Mathematics Unit is a member of Intel's complete family of OEM computers and expansion modules. The iSBC 310 acts as an intelligent slave processor to one or more iSBC computer masters as it performs its high speed arithmetic functions. It plugs into a standard iSBC 604/614 cardcage to interface directly into any iSBC 80 single board computer. Designed to increase the computational throughput of all computers in the iSBC 80 family, the iSBC 310 utilizes Intel's high speed Series 3000 Bipolar Microprocessor. The iSBC 310 performs arithmetic functions an order of magnitude faster than is possible with software routines. Standard operations include floating point add, subtract, multiply, divide, square, and square root; fixed point integer multiply, divide, and extended divide; and conversions between fixed and floating point representations, as well as test, compare, and argument exchange.



FUNCTIONAL DESCRIPTION

ISBC 80 single board computers communicate with the ISBC 310 using I/O and memory read/write commands. To pass arguments from the ISBC 80 to the ISBC 310, a memory write command is used for each byte to be loaded into the ISBC 310's working registers. An operation command is then given to the ISBC 310 by using an output instruction to pass the appropriate opcode. The mathematics unit will then perform the function independently from the single board computer; therefore, any ISBC 80 can continue to operate while the ISBC 310 is performing its arithmetic operations. Upon completion of its designated operation, the high speed mathematics unit notifies the ISBC 80 via an interrupt or by setting a status bit. The resultant data can then be read by the ISBC 80 via a memory read command to the proper memory address.

Arithmetic Functions

The ISBC 310 provides a full complement of arithmetic functions which operate on 16- and 32-bit unsigned fixed point integers, 32-bit signed fixed point integers, and 32-bit single precision floating point numbers. These functions are detailed in Table 1. The results of

comparison operations are described in the operation results section.

Status Byte

The ISBC 310 may be operated in either an interrupt driven or polled mode. Three status indications are available:

Busy — The ISBC 310 is currently processing an arithmetic command, and cannot respond to further requests.

Complete — The ISBC 310 has completed an operation without error. This line may be connected to an interrupt level via an on-board jumper.

Error — The ISBC 310 has completed an operation which results in an error condition. This line may be connected to an interrupt level via an on-board jumper.

Result Byte

After completion of an operation, a result byte may be read. This byte indicates the error conditions where applicable (see Specifications), and the results of a compare or test operation.

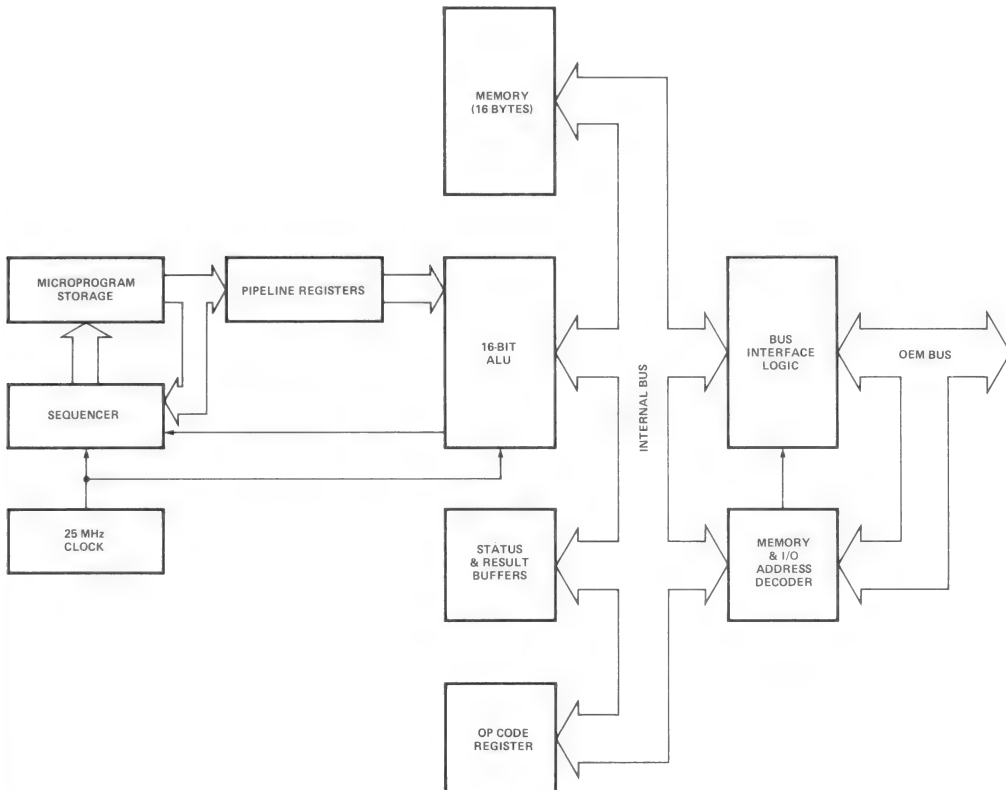


Figure 1. ISBC 310 Block Diagram Showing Functional Components

Operation	Op Code	Max Time ¹ (μ s)	Notes ²
Fixed point multiply (MUL)	0	19	$M_1 = m_1 * m_1$
Fixed point divide (DIV)	1	28	$m_1 = m_1 / M_2$, $m_2 = \text{remainder}$
Extended fixed point divide (EDIV)	E	94	$M_1 = M_1 / m_2$, $M_2 = \text{remainder}$
Floating point multiply (FMUL)	2	91	$X_1 = X_1 * X_2$
Floating point divide (FDIV)	3	102	$X_1 = X_1 / X_2$
Floating point add (FADD)	4	56	$X_1 = X_1 + X_2$
Floating point subtract (FSUB)	5	56	$X_1 = X_1 - X_2$
Square (FSQR)	6	91	$X_1 = X_1^2$
Square root (FSQRT)	7	199	$X_1 = \sqrt{X_1}$
Fixed-to-float-conversion (FLOAT)	8	89	$X_1 = N_1$
Float-to-fixed-conversion (FIX)	9	81	$N_1 = X_1$
Compare (FCOMP)	A	5	Compare X_1 and X_2
Test (FTST)	B	5	Compare X_1 and 0.0
Exchange (EXCH)	F	4	Exchange arguments (fixed or floating)

Notes

1. Does not include register setup time

2. m — 16-bit unsigned fixed point integers; M — 32-bit unsigned fixed point integer; N — 32-bit two's complement signed fixed integer; X — 32-bit single precision floating point number**Table 1. ISBC 310 Arithmetic Functions****SPECIFICATIONS****Arithmetic Functions**

See Table 1

Formats**Single Precision Floating Point (32 Bits)**

Memory Location		
Base Address (M)	$F_7 - F_0$	
$M + 1$	$F_{15} - F_8$	
$M + 2$	E_0	$F_{22} - F_{16}$
$M + 3$	S	$E_7 - E_1$

where: S = sign bit

0 = positive

1 = negative

 $E_2 - E_0$ = biased exponent (8 bits) (bias = $7F_H$) $F_{22} - F_0$ = fraction (23 bits)**Note**

F is always normalized (i.e., a "1" is assumed in the highest bit position), yielding an effective 24-bit fraction.

Fixed Point Integer (16-Bit)

Memory Location	
Base Address (M)	$F_7 - F_0$
$M + 1$	$F_{15} - F_8$

where:

 $F_{15} - F_0$ = 16-bit integer**Extended Precision Integer**

Memory Location		
Base Address (M)	$F_7 - F_0$	
$M + 1$	$F_{15} - F_8$	
$M + 2$	$F_{23} - F_{16}$	
$M + 3$	S	$F_{30} - F_{24}$

where: S = sign bit

 $F_{30} - F_0$ = two's complement integer**Result Byte**

Contains the following information:

7	6	5	4	3	2	1	0
=	>	<	R	R		ERR	

where: R is reserved for future use

= is equal (for FCOMP and FTST)

> is greater than (for FCOMP and FTST)

< is less than (for FCOMP and FTST)

and: ERR is a 3-bit error code that specifies one of the following error conditions:

- 000 No error
- 001 Divide by zero
- 010 Square root of negative number
- 011 Overflow
- 100 Underflow
- 101 First argument valid
- 110 Second argument valid
- 111 Reserved

Status Byte

Contains the following information:

7	6	5	4	3	2	1	0
R	R	R	R	R	E	C	B

where: R is reserved for future use
 B is busy
 C is operation complete without error
 E is operation complete with error

Addressing

I/O Addressing — Used to pass operation codes, memory address boundaries, and result and status bytes between host processor and ISBC 310.

Port Address	Output	Input
Base (P)	OP CODE	R
P + 1	MEM LOW	Result byte
P + 2	MEM HIGH	R
P + 3	R	R
P + 4	R	R
P + 5	R	R
P + 6	R	R
P + 7	R	Status byte

where: P = I/O base address of X0 or X8 (where X = any hex digit)

R = reserved for ISBC 310 usage

OP CODE = mathematic commands (see Table 1)

MEM LOW = programmable base address (see Memory Addressing)
 MEM HIGH =

Memory Addressing — Sixteen memory locations are used; the first eight are used for argument/result storage; the second eight are reserved for future use. Memory addresses are assigned from the host processor via an I/O output instruction (see I/O Addressing). MEM LOW (the lower address byte) must be X0 (where X is any hex digit). MEM HIGH (the upper address byte) may be any value.

Interrupts

Interrupts are generated on operation complete and operation error. Either one or both interrupts may be

connected to any of the 8 interrupt levels on the ISBC 80 bus via jumper selection.

Bus Interface

All signals are TTL compatible.

Bus Connector

Bus Connector — 86-pin, double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Control Data VPB01E43A00A1

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12 oz (340.5 gm)

Electrical Characteristics**DC Power Requirements**

V _{CC}	I _{CC}
5V ± 5%	6.7A max; 4.9A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Equipment Supplied

High speed mathematics units
 Standard preprogrammed ROMs (installed)
 Schematics
 Assembly drawing

Reference Manuals

9800410 — ISBC 310 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 310	High Speed Mathematics Unit

ISBC
COMPUTERS



5 iSBC™ Expansion Boards

**Memory Expansion
and Mass Storage**

Digital I/O Expansion

Analog I/O Expansion

iSBC EXPANSION BOARDS

INTRODUCTION

Both the Intel single board computers and Intel packaged systems are supported by a complete line of memory and mass storage expansion boards, digital and analog I/O expansion boards, and peripheral and DMA controllers. These boards are used with Intel's System 80/10 and System 80/20 to extend the iSBC capabilities into low cost, fully packaged, RETMA rack mountable computers. This section provides technical details on the broad lines of MULTIBUS compatible memory, digital parallel and serial I/O, analog I/O, and peripheral controller expansion boards.

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iSBC 032/048/064 RAM MEMORY BOARDS

**iSBC 80 RAM memory expansion through
direct MULTIBUS interface**

**32K, 48K, 64K bytes of read/write memory
(iSBC 032, iSBC 048, iSBC 064,
respectively)**

**On-board hardware for refresh of all
dynamic memory elements**

**Auxiliary power bus and memory protect
control logic provided for battery backup
RAM requirements**

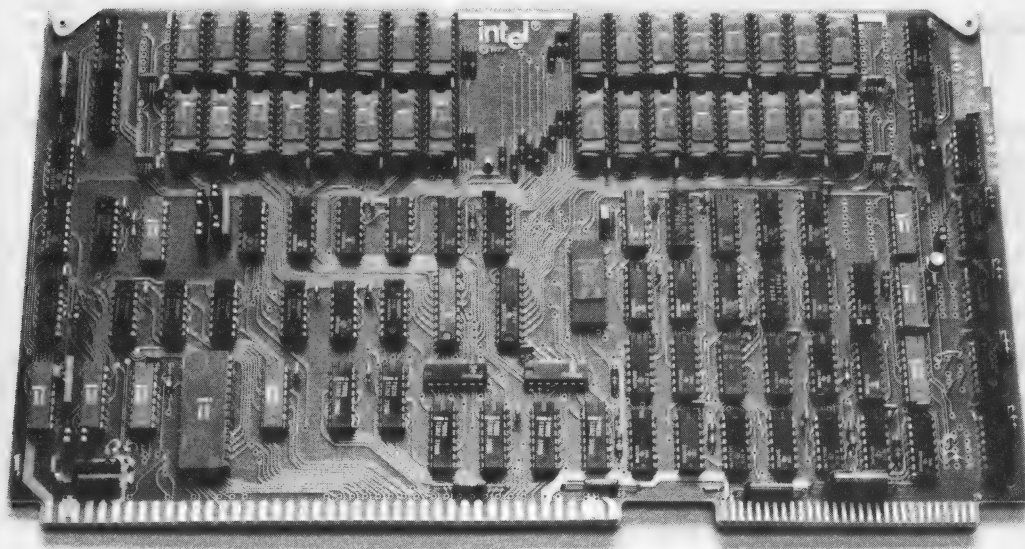
**Jumper selectable starting address for
independent 16K-byte memory segments**

Read/write data buffers

**TTL compatible data, address, and com-
mand signal interface**

The iSBC 032, iSBC 048, and iSBC 064 RAM Memory Boards are members of Intel's complete line of iSBC 80 memory and I/O expansion boards. Each board interfaces directly to any Intel iSBC 80 single board computer via the MULTIBUS interface to expand RAM memory capacity. The iSBC 032 contains 32K, the iSBC 048, 48K, and the iSBC 064, 64K bytes of read/write memory implemented using Intel dynamic RAM memory components. On-board refresh hardware refreshes a portion of RAM memory every 14 microseconds. Each refresh cycle utilizes memory for 585 nanoseconds. If a read or write cycle is in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the cycle. The iSBC 032 contains jumpers used to individually select two independent 16-byte memory segments, and the iSBC 048 contains jumpers used to individually select three independent 16K-byte memory segments starting at locations 0000_H, 4000_H, 8000_H, or C000_H. Read/write buffers reside on each board to buffer all data written into or read from the memory array. All data, address, and command signals on the bus interface are TTL compatible.

EXPANSION
BOARDS



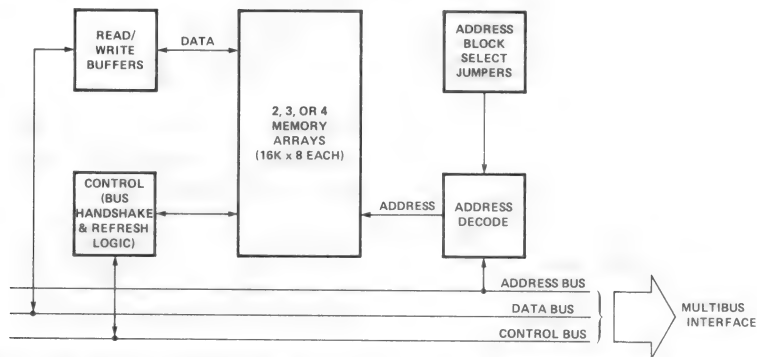


Figure 1. RAM Memory Expansion Boards Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

32,768 bytes (iSBC 032), 49,152 bytes (iSBC 048), 65,536 bytes (iSBC 064)

Access Time

450 ns max

Cycle Times

Read Cycle — 700 ns max

Write Cycle — 600/1240 ns max

Refresh Cycle — 700 ns max

Interface

All address, data, and command signals TTL compatible.

Address Selection

Jumper selection for independent 16K-byte memory blocks starting at locations 0000_H, 4000_H, 8000_H, or C000_H.

Connectors

Edge Connectors — 86-pin double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Control Data VPB01E43A00A1.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery back up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.76 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 14 oz (415.2 gm)

Electrical Characteristics

DC Power Requirements

Voltage	Normal System Operation ¹ (max)	Battery Backup ² (max)
V _{CC} = +5V ± 5%	I _{CC} = 2.0A typ; 3.2A	1.0A typ; 1.7A
V _{DD} = +12V ± 5%	I _{DD} = 400 mA typ; 600 mA	100 mA typ; 200 mA
V _{BB} = -5V ± 5%	I _{BB} = 30 mA typ; 40 mA	30 mA typ; 40 mA

Notes

1. All current values given here apply to iSBC 032, iSBC 048, or iSBC 064, and include battery backup power.
2. RAM chips and RAM control logic (powered via auxiliary power bus).

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manuals

9800488 — iSBC 032/048/064 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 032	32K-Byte RAM Board
SBC 048	48K-Byte RAM Board
SBC 064	64K-Byte RAM Board



iSBC 016 16K-BYTE RAM MEMORY BOARD

iSBC-80 RAM memory expansion through
direct bus interface

16K-byte read/write memory capacity

On-board hardware for refresh of all
dynamic memory elements

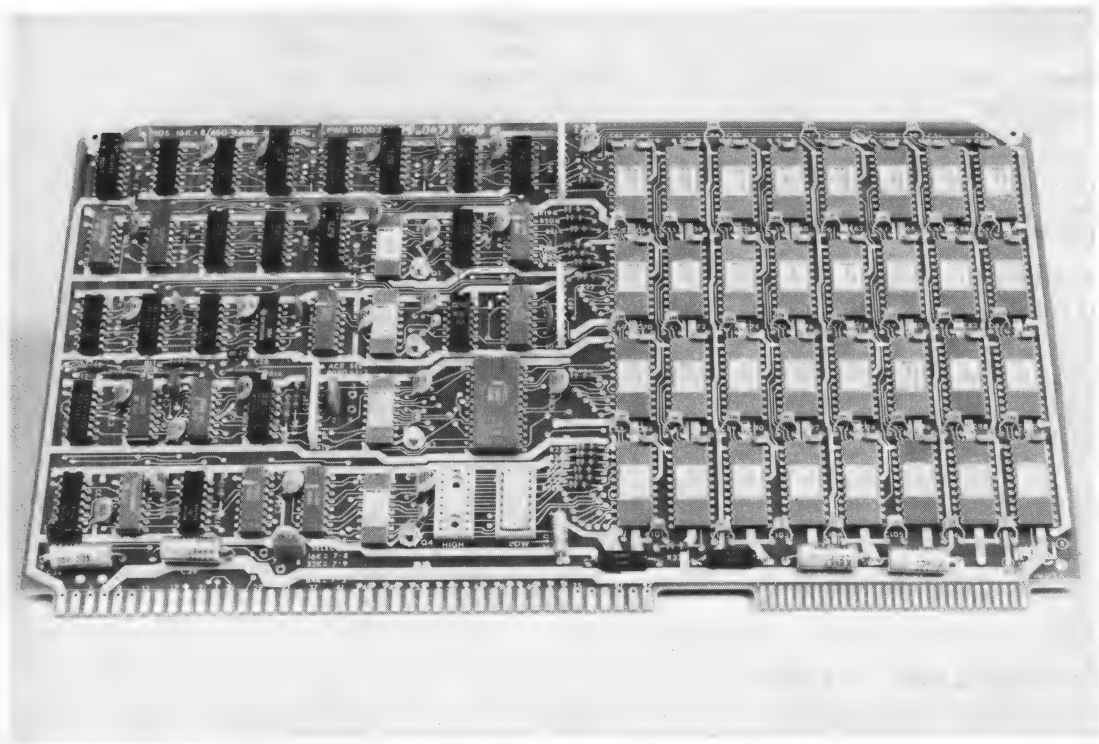
Jumper selectable starting address for
16K contiguous addresses

Read/write data buffers

TTL compatible data, address, and
command signal interface

The iSBC 016 16K-Byte Ram Memory Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 016 interfaces directly to any iSBC 80 single board computer via the system bus to expand RAM memory capacity. The board contains 16K bytes of read/write memory, implemented using 32 Intel 2107 dynamic RAM memory components. On-board refresh hardware refreshes 64 bit positions of all 32 RAM elements every 14 microseconds. Each refresh cycle utilizes memory for 735 nanoseconds. If a read or write cycle is in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the cycle. The iSBC 016 contains a jumper used to select contiguous 16K-byte address segments starting in locations 0000, 4000, 8000, or C000. Read/write buffers reside on the board to buffer all data written into or read from the memory array. All data, address, and command signals on the bus interface are TTL compatible.

EXPANSION
BOARDS



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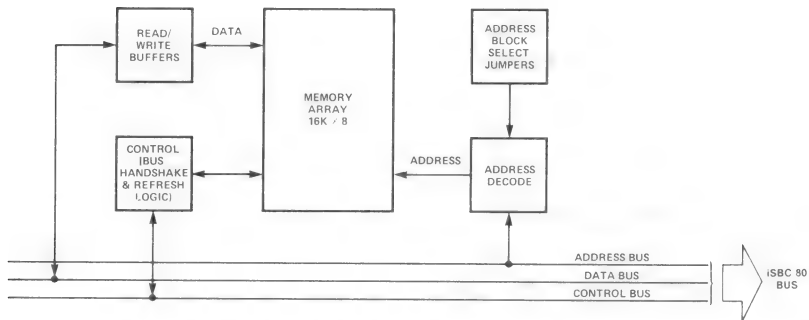


Figure 1. iSBC 016 16K RAM Memory Expansion Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

16,384 bytes

Cycle Times

Read Cycle — 735 ns max

Write Cycle — 1360 ns max

Refresh Cycle — 735 ns max

Interface

All address, data, and command signals are TTL compatible.

Address Selection

Jumper selection of base address of 16K contiguous memory block to reside in locations 0000, 4000, 8000, or C000.

Connectors

Edge Connector — 86-pin double-sided PC edge connector with 0.156-in. contact centers.

Mating Connector — Control Data VPB01E43A00A1

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12 oz (415.2 gm)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V$ DC $\pm 5\%$

$I_{CC} = 1.2A$ typ; 1.5A max

$V_{DD} = +12V$ DC $\pm 5\%$

$I_{DD} = 0.7A$ typ; 1.0A max

$V_{BB} = -5V$ DC $\pm 5\%$

$I_{BB} = 0.2$ mA typ; 3.2 mA max

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800279 — iSBC 016 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 016	16K-Byte RAM Memory Board



iSBC 094 4K-BYTE CMOS RAM MEMORY BATTERY BACKUP BOARD

**iSBC 80 nonvolatile RAM memory
expansion through direct bus interface**

**Base address selectable to start on any
4K memory address boundary**

**4K bytes of low power static CMOS
RAM memory**

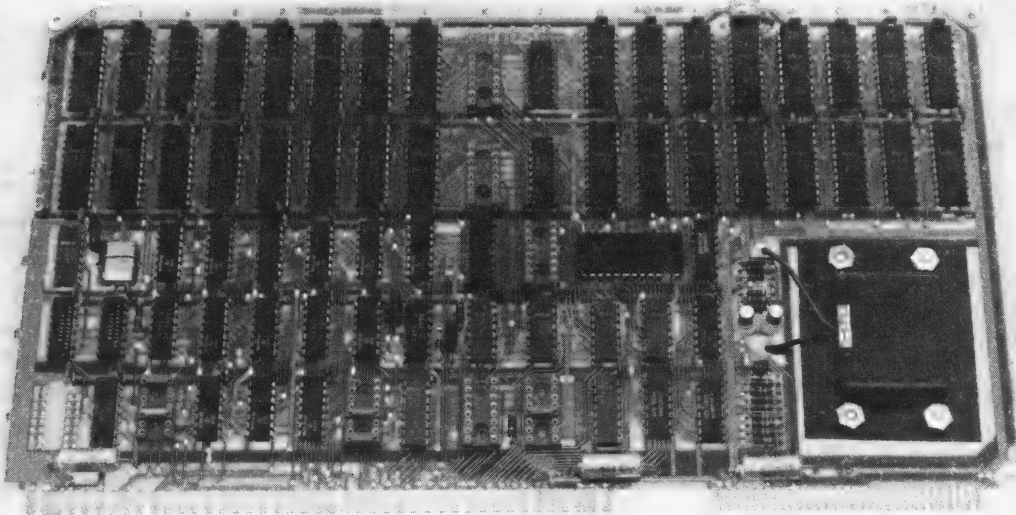
**On-board rechargeable batteries and
charging circuitry for 96-hour data
retention**

On-board power-fail interface logic

Single +5V power requirement

The iSBC 094 4K-Byte CMOS RAM Memory/Battery Backup Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 094 interfaces directly to iSBC 80 single board computer via the system bus to expand RAM memory capacity. The board contains 4K bytes of read/write memory, implemented using 32 Intel 5101 CMOS RAM memory components. On-board rechargeable batteries and charging circuitry insure that data contained in RAM will be retained for at least 96 hours after system bus power (+5V) is removed. Critical system parameters stored in the iSBC 094 RAM will thus be saved during temporary system power failures. Full power-fail interface logic is provided on the board to generate a CPU interrupt when system power fails. Orderly system shut-down procedures may then be executed and critical system parameters may be retrieved and stored. The use of CMOS RAM on the iSBC 094 also reduces power dissipation during normal system operation. The iSBC 094 contains jumpers for use in selecting a contiguous 4K-byte address segment beginning on any 4K memory address boundary (0000H, 1000H, 2000H, etc). Read/write buffers reside on the board to buffer all data written into or read from the memory array. All address, data, and command signals on the bus interface are TTL compatible.

**EXPANSION
BOARDS**



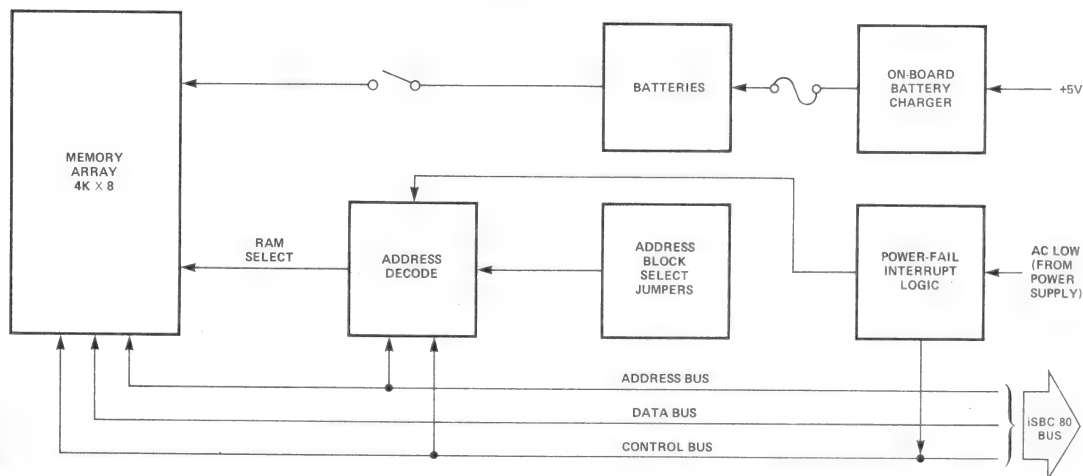


Figure 1. iSBC 094 Memory Backup Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

4096 bytes

Memory Response Time

Operation	Access (ns, max)	Cycle (ns, max)
Read	750	900
Write	—	900

Interface

All address, data, and command signals are TTL compatible.

Power Fail Interrupt

Control logic is also included for generation of a power-fail interrupt to the iSBC 80 bus, which works in conjunction with the AC low signal from the Intel iSBC 635 Power Supply or equivalent.

Memory Protect

An on-board memory protect signal disables read/write access to RAM memory on the board. This input is pro-

vided for the protection of RAM contents during system power-down sequences. This signal is automatically asserted by the power-fail interface logic 3.6 ms after the AC low signal is received from the system power supply to signify that system power is beginning to fail.

Address Selection

4K segments starting at any jumper selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, ... F000_H).

Mating Connectors

Interface	Pins (qty)	Centers(in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1 Viking 2VH43/1AND5
Auxiliary ¹	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector Dimensions vary from vendor to vendor. Review vendor specifications to ensure that connector heights and wire-wrap pin lengths to conform to your system packaging requirements.

Data Retention

96 hours minimum after +5V bus power is removed.

Battery Characteristics

Type — Nickel-Cadmium, rechargeable

Capacity — 150 mA hr

Voltage — 3.6V nominal

Battery Charger Characteristics**Charge Time**

14 hours for full charge (150 mA hr)

Full overcharge protection

Full short-circuit protection

Physical Characteristics**Width** — 12.00 in. (30.48 cm)**Height** — 6.75 in. (17.15 cm)**Depth** — 0.60 in. (1.27 cm)**Weight** — 12 oz (340.5 gm)**Electrical Characteristics****Average DC Current** $V_{CC} = +5V\ DC \pm 5\%$ $I_{CC} = 0.8A\ typ, 1.7A\ max$ **Environmental Characteristics****Operating Temperature** — 0°C to 55°C**Reference Manuals****9800440** — iSBC 094 Hardware Reference Manual
(SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 094	4K-Byte CMOS RAM Memory Battery Backup Board

iSBC 416 16K PROM EXPANSION BOARD

Allows iSBC 80 EPROM/ROM expansion through direct bus interface

Switches to enable or disable each memory block

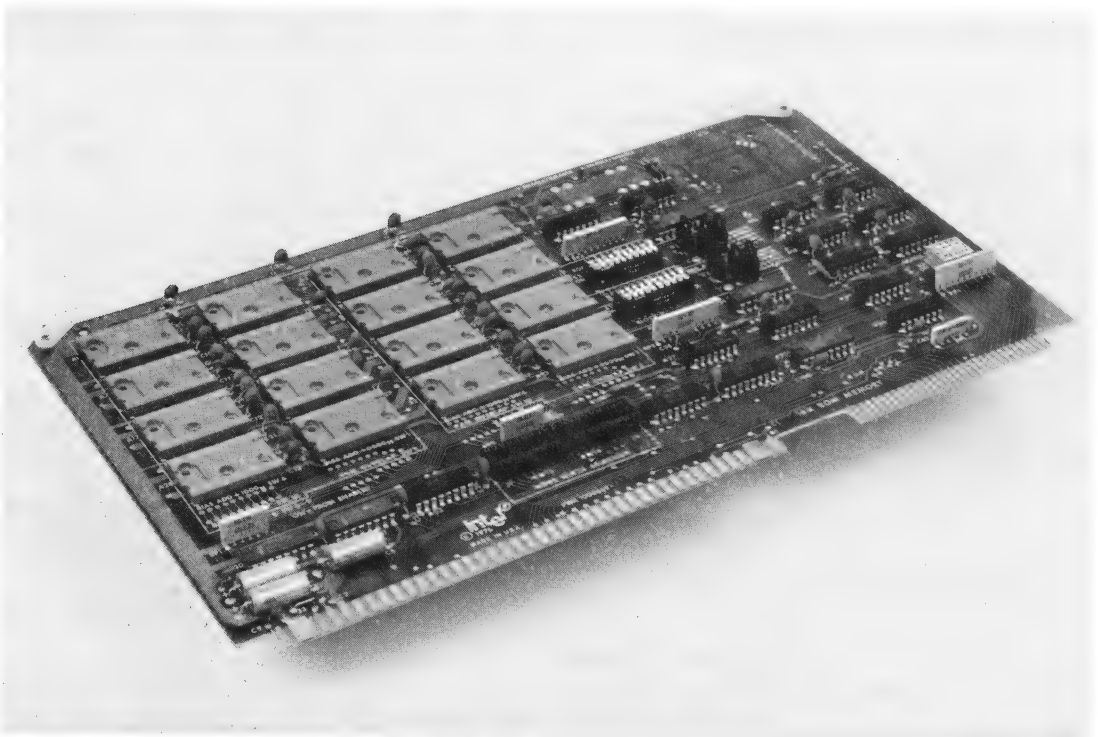
Sockets for up to 16K bytes of interchangeable Intel 8308 masked ROM or 8708 programmable and erasable PROM

Jumper selectable addresses for each 8K block

Buffered address and data lines

EXPANSION
BOARDS

The iSBC 416 16K PROM Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 416 interfaces directly to any iSBC 80 single board computer via the system bus to expand ROM/PROM memory capacity. The board contains 16 sockets that can house either Intel 8308 masked ROMs or Intel 8708 programmable and erasable EPROMs. ROM/PROM memory can be added in 1K-byte increments. The iSBC 416 contains a set of jumpers allowing the selection of the base address of independent 8K memory blocks, to begin on any 8K boundary. Switches are used to enable on-board memory in 1K-block increments.



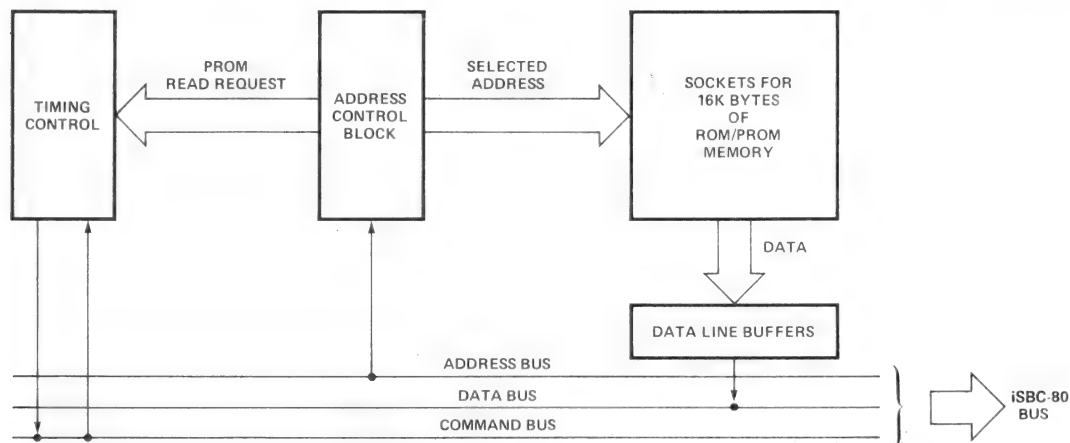


Figure 1. iSBC 416 PROM Expansion Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Memory Size

Sockets for up to 16K bytes. Memory may be added in 1K-byte increments.

Compatible Intel Memory

ROM: 8308

PROM: 8708

Interface

All address, data, and command signals are TTL compatible and iSBC 80 bus compatible.

Address Selection

Switches and jumpers allowing the selection of a base address for each independent 8K block of memory, on any 8K boundaries

Connectors

Edge Connector — 86-pin double-sided PC edge connector with 0.156-in. (0.40 cm) contact centers.

Mating Connector — Control Data VPB01E43A00A1

Physical Characteristics

Width — 12.00 in. (30.40 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

	Without Memory	With 8308		With 8708	
		Typ	Max	Typ	Max
+5V	0.75A	0.77A	0.79A	0.85A	0.91A
-5V	—	0.001A	0.010A	0.48A	0.75A
+12V	—	0.58A	0.96A	0.80A	1.04A

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800265 — iSBC 416 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 416	16K PROM Expansion Board



iSBC 104/108/116 COMBINATION MEMORY AND I/O EXPANSION BOARDS

**4K, 8K, 16K bytes of read/write memory
(iSBC 104, iSBC 108, iSBC 116,
respectively)**

**Sockets for up to 8K bytes of program-
mable or masked read only memory**

**Auxiliary power bus and memory protect
control logic provided for battery backup
RAM requirements**

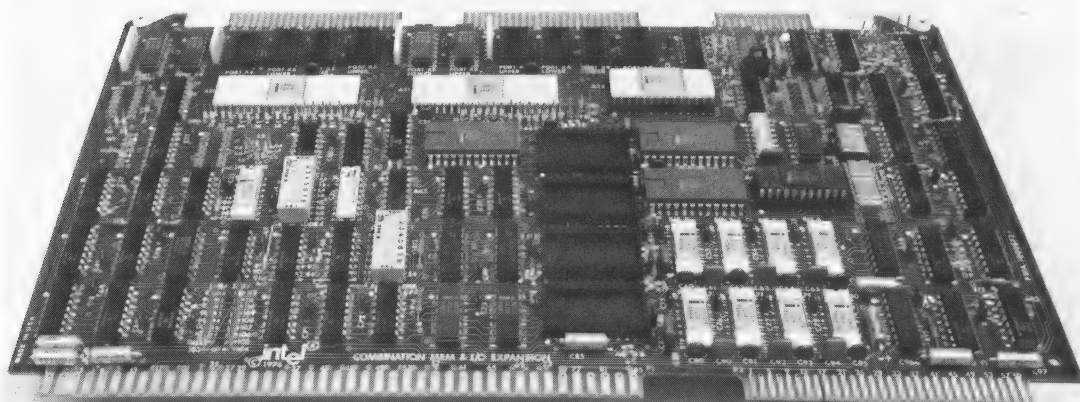
**48 programmable I/O lines with sockets
for interchangeable line drivers and
terminators**

**Synchronous/asynchronous communica-
tions interface with RS232C drivers and
receivers**

**Eight maskable interrupt request lines
with a pending interrupt register**

1 ms interval timer

The iSBC 104, iSBC 108, and iSBC 116 Combination Memory and I/O Expansion Boards are members of Intel's complete line of iSBC 80 memory and I/O expansion boards. Each board interfaces directly with any iSBC 80 single board computer via the system bus to expand RAM and ROM memory capacity and serial and parallel I/O capacity. The iSBC 104 contains 4K, the iSBC 108 8K, and the iSBC 116 16K bytes of RAM memory implemented using Intel dynamic RAM memory components. On-board refresh hardware refreshes a portion of all eight RAM memory elements every 14 microseconds. If a read or write cycle is already in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the read or write cycle. Each refresh cycle utilizes memory for 590 nanoseconds. Typical RAM access time is 485 nanoseconds. Typical read/write cycle time is 560 nanoseconds. Four sockets for up to 8K bytes of nonvolatile read-only-memory reside on the boards. Read-only-memory may be added in 1K-byte increments using Intel 8708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs. Read-only-memory may also be added in 2K-byte increments (up to 8K bytes, total) using Intel 2716 EPROMs or Intel 8316B masked ROMs.



Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X ¹
	4	X		X			X ¹
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X ²
	4	X		X			X ²
Notes							
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output or port 1 is used as a bidirectional port.							
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output or port 4 is used as a bidirectional port.							

Table 1. Input/Output Port Modes of Operation

SPECIFICATIONS

Memory Addressing

ROM/EPROM — 4K or 8K segments starting at any jumper selectable base address on a 4K-byte boundary (e.g., 0000_H, 10000_H, ..., F000_H)

Note

All EPROM/ROM addresses must reside in the range of 0000_H to 7FFF_H or 8000_H to FFFF_H.

RAM — 4K, 8K, 16K segments starting at any jumper selectable base address on a 4K-byte boundary (e.g., 0000_H, 1000_H, ..., F000_H).

Note

Base addresses 7000_H and F000_H not allowed for iSBC 108. Base addresses 5000_H→7000_H and D000_H→F000_H not allowed for iSBC 116.

Memory Response Time

Memory	Access (ns)	Cycle (ns)
RAM	575 max*	675 max*
EPROM/ROM	465 max	685 max

*Without refresh interruption.

I/O Addressing

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note

X is any hex digit assigned by jumper selection.

I/O Transfer Rate

Parallel — Read or write cycle time 760 ns max

Serial — (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous (Program Selectable)
153.6	—	+ 16 + 64
76.8	—	9600 2400
38.4	38400	4800 1200
19.2	19200	2400 600
9.6	9600	1200 300
4.8	4800	600 150
6.98	6980	300 75
		— 110

Serial Communications Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5—8 bit characters; break characters generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines), or interval timer.

Interrupt Register Addresses

X1 Interrupt mask register

X0 Interrupt status register

Note

X is any hex digit assigned by jumper selection.

Timer Interval

1.003 ms ± 0.1% when 110 baud rate is selected

1.042 ms ± 0.1% for all other baud rates

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C

Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary Power	60	0.1	AMP PE5-14559 or TI H311130

Note

Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or MDS packaging.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

I/O Drivers

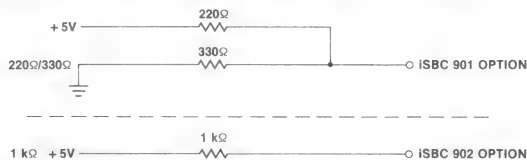
The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 104/108/116. Ports 1 and 4 have 25 mA totem-pole drivers and 1 k Ω terminators.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup.



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 14 oz (397.3 gm)

Electrical Characteristics¹

Average DC Current

Voltage ($\pm 5\%$)	Without EPROM ² (max)	With 8708 EPROM ³ (max)	With 2716 EPROM ⁴ (max)	RAM ⁵ (max)
$V_{CC} = +5V$	$I_{CC} = 2.85A$	3.6A	4.0A	600 mA
$V_{DD} = \pm 12V$	$I_{DD} = 450 mA$	700 mA	450 mA	400 mA
$V_{BB} = -5V$	$I_{BB} = 3 mA$	180 mA	3 mA	3 mA
$V_{AA} = -12V$	$I_{AA} = 60 mA$	60 mA	60 mA	Not Used

Notes

1. All current values given here include RAM power.
2. Does not include power required for optional EPROM, I/O drivers, and I/O terminators.
3. With four 8708 EPROMs and eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.
4. With four Intel 2716 EPROMs and eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.
5. RAM chips and RAM control logic (powered via auxiliary power bus).

Environmental Characteristics

Operating Temperature — 0°C to +55°C.

Reference Manuals

9800277 — iSBC 104/108/116 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number

Description

SBC 104	Combination Memory and I/O Expansion Board with 4K bytes RAM
SBC 108	Combination Memory and I/O Expansion Board with 8K bytes RAM
SBC 116	Combination Memory and I/O Expansion Board with 16K bytes RAM



iSBC 201 DISKETTE CONTROLLER

Provides interface for high speed random access bulk storage capability for Intel OEM computers

Provides microprocessor control of two flexible diskette drives

Microprogrammed for maximum flexibility and easy software development

Compatible with majority of diskette drives, including Shugart and Control Data

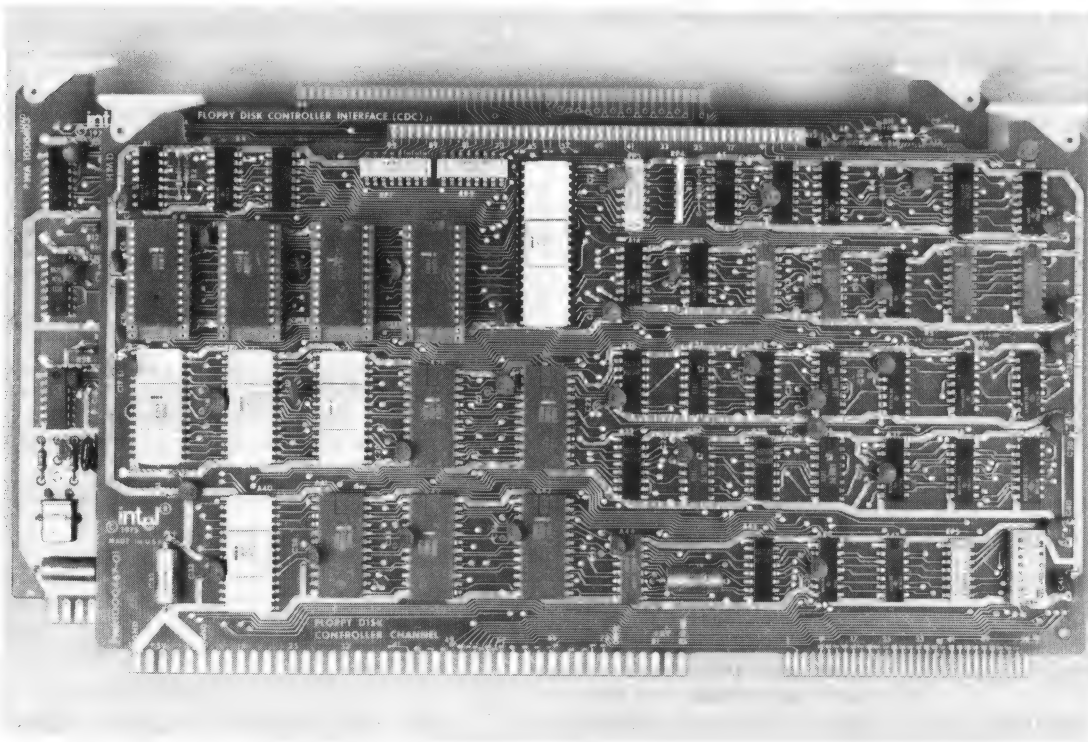
Complete CRC data checking

Data addressed using IBM soft-sectored format allowing 256K bytes of data capacity per diskette

iSBC bus compatible; plugs into standard System 80 backplane or iSBC 604/614 cardcage

Optional go/no go diagnostic

The iSBC 201 Diskette Controller is a high speed, modular set of boards providing the OEM with a powerful and easy to use control technique for the interfacing of Intel MULTIBUS compatible OEM computers with industry standard flexible diskettes. The diskette controller is directly compatible with the entire family of System 80 and iSBC 80 OEM computers, and will interface directly with the majority of flexible diskette drives in use today.



FUNCTIONAL DESCRIPTION

The iSBC 201 Diskette Controller provides an easy to use interface for OEM use of Intel's OEM computers and other manufacturers' flexible diskettes. The controller enables the OEM to develop system software in a simple, straightforward manner. All DMA logic is provided, so no additional boards or circuitry are required, and either one or two flexible diskette drives may be interfaced to the Intel computer with each iSBC 201. The controller is implemented with Intel's powerful Series 3000 Bipolar Microprocessor Set. The controller facilitates recording all data in the IBM-compatible soft-sector format. The controller consists of two boards which may reside in the System 80 chassis, in the iSBC 604 or iSBC 614 Modular Cardcage, or in an OEM custom designed, Intel bus-compatible backplane.

Channel Board

Channel Board Function — The channel board is the primary control module within the diskette controller. The channel board receives, decodes, and responds to channel commands from the central processor unit (CPU) in the Intel OEM computer system. The channel board can access a block of system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

Control Function — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512 × 32 bits of 3604 programmable read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the channel board.

Interface Board

Interface Board Function — The interface board provides the iSBC 201 Diskette Controller with a means of communication with the diskette drives, as well as with the Intel OEM computer system bus. Under control of the microprogram being executed on the channel board, the interface board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The interface board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board. The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Write Operations — During write operations, the interface board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

Memory Operations — When the diskette controller requires access to the system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intel OEM computer bus.

Programming Capability

IOPB Function — Although the controller has been designed primarily to simplify programming, it also has unique capabilities for generating sophisticated software when required. All diskette operations are initiated by Intel OEM computer with standard I/O commands. Once initiated, however, the diskette controller completes the specified operation without further intervention on the part of the CPU. Only three general steps are performed by the CPU to complete any diskette operation:

1. The CPU must prepare and store in system memory an I/O parameter block (IOPB) for each operation to be performed. If multiple operations are desired, the IOPBs can be linked together in the proper order.
2. The CPU then passes the memory address of the first (or only) IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation(s).

IOPB Format — In preparing the IOPBs, the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared, utilizing the following format for the 10-byte parameter block:

Byte	Command
1	Channel word
2	Diskette instruction
3	Number of records
4	Track address
5	Sector address
6	Buffer address (lower)
7	Buffer address (upper)
8	Block number
9	Next IOPB address (lower)
10	Next IOPB address (upper)

Channel Command Function — The channel word or command provides the controller with information to determine the method of assigning logical sector addresses, enable or disable a series of possible diskette interrupts, determine if the parameter block is properly prepared, and determine the length of the data word to be transferred.

Compatible Equipment

Interface Cables — For OEM convenience, Intel provides cables for use with specific manufacturers' drives. The iSBC 951 cable may be used to connect the diskette controller to a Shugart Model 800/800R Flexible Diskette Drive. The iSBC 952 may be used to connect the controller to a Control Data Model 9404 Flexible Diskette Drive. Cabling for these drives or any other flexible diskette drives may also be OEM fabricated as required.

9404 Flexible Diskette Drive. Cabling for these drives or any other flexible diskette drives may also be OEM fabricated as required.

Go/No Go Diagnostic — For OEM convenience, Intel makes available a diskette exerciser and monitor program to facilitate checkout and debugging of OEM-built systems using Intel OEM computers and diskette controllers. The iSBC 915 and iSBC 925 go/no go diagnostic programs are available on four 1K-byte ROMs for instal-

lation in the PROM/ROM memory section of Intel computers. The programs include commands to display and alter main memory and registers, insert instructions, move main memory, substitute main memory, and exercise the flexible diskette drives by reading and/or writing individual sectors, reading sequentially sector-to-sector and track-to-track, and writing/reading random sectors and tracks. The go/no go diagnostic program is designed to provide a convenient means of determining the functionality of any OEM system.

SPECIFICATIONS

Media

Flexible diskette
One recording surface
IBM soft-sector format
77 tracks/diskette
26 sectors/tracks
128 bytes/sector

Physical Characteristics

Mounting — Occupies two slots of System 80 chassis or iSBC 604/614 cardcage

Height — 6.75 in. (17.15 mm)

Width — 12.00 in. (30.48 mm)

Depth — 0.50 in. each board (1.27 mm)

Electrical Characteristics

DC Power Requirements

Channel Board: 5V @ 3.75A typ, 5A max

Interface Board: 5V @ 1.5A typ, 2.5A max

Environmental Characteristics

Temperature

Operating: 0 to 55°C

Non-Operating: -55°C to +85°C

Humidity

Operating: Up to 90% relative humidity without condensation

Non-Operating: All conditions without condensation of water or frost

Equipment Supplied

FDC channel board
FDC interface board
Dual auxiliary board connector

Optional Equipment

iSBC 915 go/no go diagnostic and monitor program for iSBC 80/10 and System 80/10

iSBC 925 go/no go diagnostic and monitor program for iSBC 80/20 and System 80/20

iSBC 951 cables for Shugart Model 800/800R Diskette Drives

iSBC 952 cables for CDC Model 9404 Diskette Drives

Reference Manuals

None

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 201	Diskette Controller



iSBC 202 DOUBLE DENSITY DISKETTE CONTROLLER

iSBC 80 compatible interface, control and DMA logic for high speed, high capacity random access bulk storage

Provides control of up to four flexible diskette drives

Soft-sectored format allowing 500K-byte data storage capacity per double density diskette

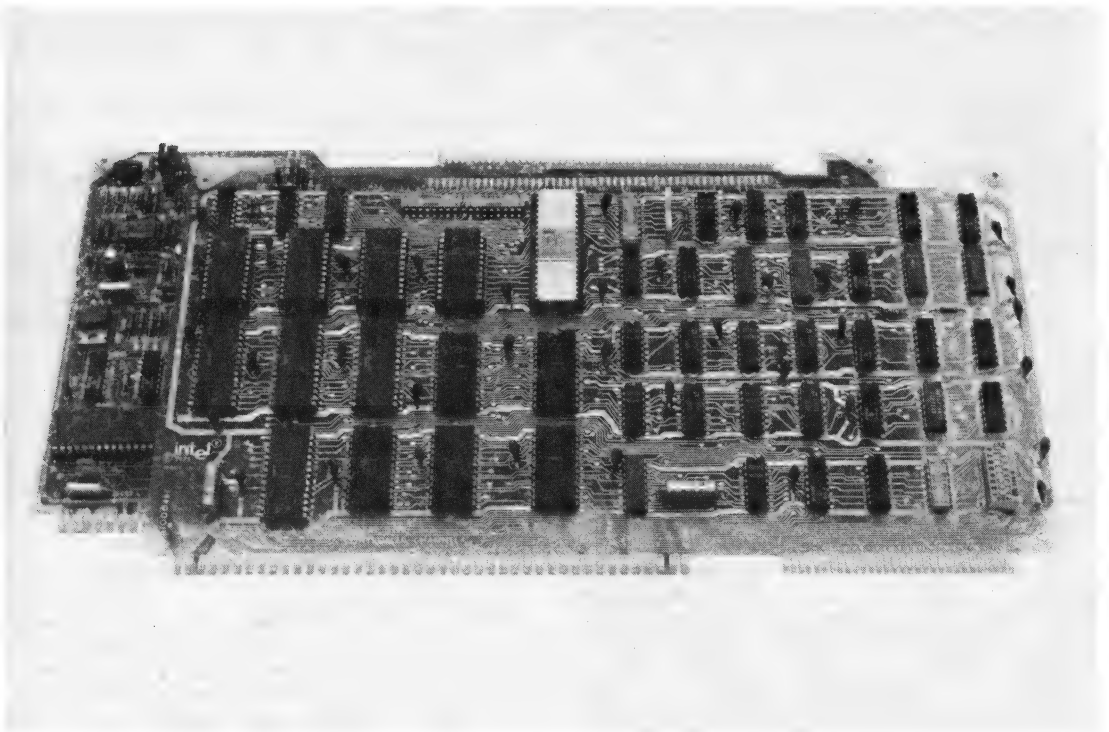
DMA channel allows single board computer to process in parallel with block transfer between diskettes and memory

Complete CRC data checking

Compatible with Shugart SA 800-1 and other double density diskette drives

EXPANSION
BOARDS

The iSBC 202 Double Density Diskette Controller interfaces any Intel MULTIBUS compatible iSBC 80 single board computer to double density flexible diskette drives via a direct bus interface. Designed with Intel's powerful 3000 Series of microprogrammable bit-slice microprocessors, the iSBC 202 provides a high speed, efficient, and easy to use high capacity random access bulk storage interface.



FUNCTIONAL DESCRIPTION

The iSBC 202 Double Density Diskette controller provides an easy to use interface for OEM use of Intel single board computers and other manufacturers' flexible diskette drives. All DMA logic is provided so no additional boards or circuitry are required, and up to four double density flexible diskette drives may be interfaced with each iSBC 202. The controller facilitates recording all data in soft-sector format. The controller consists of two boards which may reside in the System 80 chassis, the iSBC 604 or 614 modular cardcage, or in an OEM custom designed iSBC 80 bus-compatible backplane. The iSBC 202 has been designed to be compatible with a majority of double density specified flexible diskette drives. The microprogrammed track format consists of 52 records with 128 bytes per record. The Shugart SA 800-1 drive is fully compatible with this dense track format due to its "straddle-erase" magnetic head. Use of other manufacturers' flexible disk drives is accommodated also, with the limitation that after any "write data" operation, the CPU must delay 500 μ s before issuing another read or write command (due to the "delayed-erase" magnetic head). Therefore, use of multi-sector "write data" commands is only possible with the SA 800-1 drive.

Channel Board

Channel Board Function — The channel board is the primary control module within the diskette controller. It receives, decodes, and responds to channel commands from the central processor unit (CPU) on the Intel iSBC 80 Single Board Computer. The channel board can access a block of system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

Control Function — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512 \times 32 bit of 3604 programmable read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the channel board.

Interface Board

Interface Board Function — The interface board provides the iSBC 202 Double Density Diskette Controller with a means of communicating with the diskette drives, as well as with the Intel iSBC 80 system bus. Under control of the microprogram being executed on the channel board, the interface board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The interface board accepts the data being read off the diskette, inter-

prets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board. The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Write Operations — During write operations, the interface board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

Memory Operations — When the diskette controller requires access to the system memory, the interface board requests and maintains DMA transfer control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intel iSBC 80 system bus.

Programming Capability

IOPB Function — Although the controller has been designed primarily to simplify programming, it also has unique capabilities for generating sophisticated software when required. All diskette operations are initiated by an Intel iSBC 80 single board computer with standard I/O commands. Once initiated, however, the diskette controller completes the specified operation without further intervention on the part of the CPU. Only three general steps are performed by the CPU to complete any diskette operation:

1. The CPU must prepare and store in system memory an I/O parameter block (IOPB) for each operation to be performed.
2. The CPU then passes the memory address IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation.

IOPB Format — In preparing the IOPB, the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared, utilizing the following format for the 7-byte parameter block:

Byte	Command
1	Channel word
2	Diskette instruction
3	Number of records
4	Track address
5	Sector address
6	Buffer address (lower)
7	Buffer address (upper)

Channel Command Function — The channel word or command provides the controller with information to determine the method of assigning logical sector addresses, enable or disable a series of possible diskette interrupts, and determine the length of the data word to be transferred.

SPECIFICATIONS

Media

Flexible diskette
One recording surface
77 tracks/diskette
52 sectors/track
128 bytes/sector

Physical Characteristics

Mounting — Occupies two slots of System 80 chassis or iSBC 604/614 cardcage

Height — 6.75 in. (17.15 mm)

Width — 12.00 in. (30.48 mm)

Depth — 0.50 in. (1.27 mm)

Electrical Characteristics

DC Power Requirements

Channel Board: 5V @ 3.75A typ, 5A max

Interface Board: 5V @ 1.5A typ, 2.5A max; -5V @ 0.1A typ, 0.2A max

Environmental Characteristics

Temperature

Operating: 0°C to 55°C

Non-Operating: -55°C to +85°C

Humidity

Operating: Up to 90% relative humidity without condensation

Non-Operating: All conditions without condensation of water or frost

Equipment Supplied

DDFDC channel board

DDFDC interface board

Dual auxiliary board connector

Reference Manuals

9800420 — iSBC 202 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
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SBC 202	Double Density Diskette Controller
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iSBC 211/212 DISKETTE HARDWARE SYSTEM

**High speed, random access bulk storage
for Intel's OEM computer family**

Single drive or dual drive packages

**IBM soft-sectored format allowing
256K-byte data storage capacity per
diskette**

High speed I/O capability

- 250 kilobit/sec transfer rate
- 10 ns track-to-track access time

**Compact RETMA compatible chassis
design**

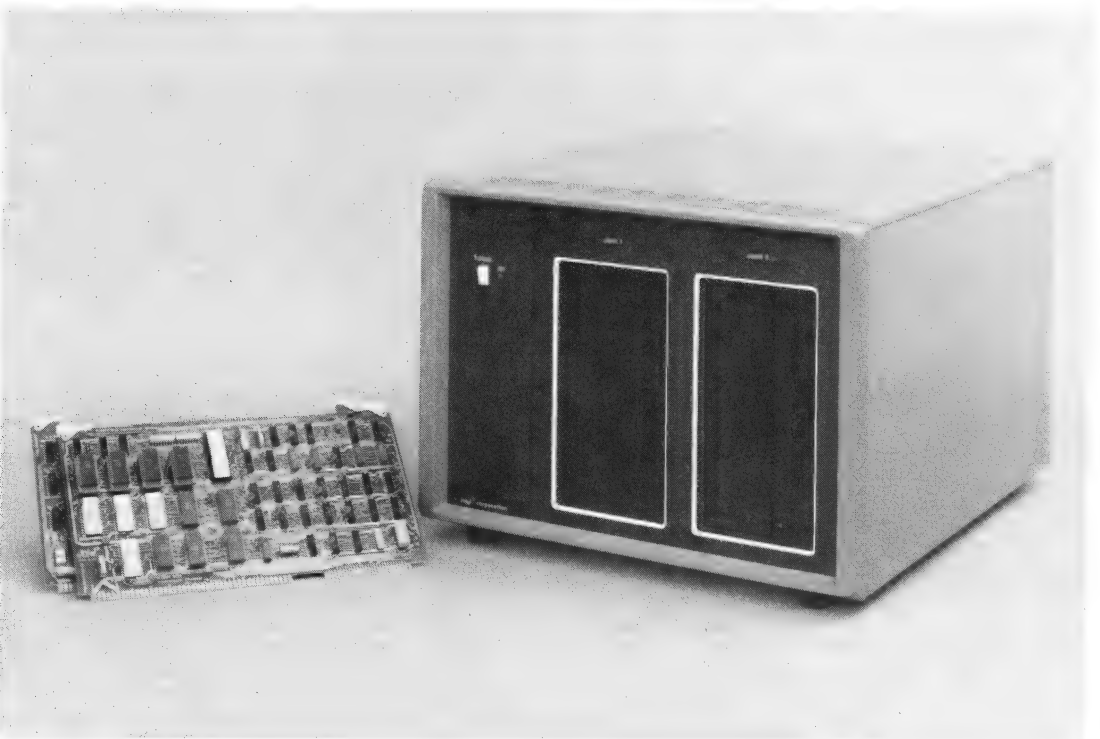
**Microprogrammed diskette controller
allowing easy software development**

Complete CRC data checking

**iSBC bus compatible; diskette controller
plugs into standard System 80 backplane
or iSBC 604/614 cardcage**

Optional go/no go diagnostic

The iSBC 211 Diskette Hardware System and the iSBC 212 Diskette Hardware System are high-speed, random access bulk storage systems for use with Intel's iSBC 80 and System 80 OEM computers. The iSBC 211 is a single drive diskette system and the iSBC 212 is a dual drive system. Both are complete subsystems with the drives fully packaged in a standard RETMA compatible chassis and with Intel's diskette controller. The controller boards simply plug into either the System 80 backplane or the iSBC 604/614 cardcage, and interface with standard cable to diskette drives.



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FUNCTIONAL DESCRIPTION

The iSBC 211 and iSBC 212 hardware diskette systems provide direct access to bulk storage, with an intelligent controller, and up to two diskette drives. Each drive provides 1/4 million bytes of storage with a data transfer rate of 250,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intel OEM computer bus as well as supporting the two diskette drives. The diskette system can record all data in the IBM-compatible soft-factor format. The iSBC diskette controller consist of two boards, the channel board and the interface board. These two printed circuit boards, residing in the iSBC 604/614 cardcage or in the System 80, constitute the diskette controller.

Channel Board

Channel Board Function — The channel board is the primary control module within the diskette system. The channel board receives, decodes, and responds to channel commands from one or more bus masters in this Intel OEM computer system. The channel board can access a block of computer system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

Control Function — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512 x 32 bits of 3604 programmable read only memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the channel board.

Interface Board

Interface Board Function — The interface board provides the iSBC 211 Diskette Controller with a means of communicating with the diskette drives, as well as with the Intel OEM computer system bus. Under control of the microprogram being executed on the channel board, the interface board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track, and verify successful operation. The interface board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board. The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Write Operations — During write operations, the interface board outputs the data clock bits to the selected drive at the proper times and generates the CRC characters which are then appended to the data.

Memory Operations — When the diskette controller requires access to the system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intel OEM computer bus.

Programming Capability

IOPB Function — Although the controller has been designed primarily to simplify programming, it also has unique capabilities for generating sophisticated software as required. All diskette operations are initiated by the Intel OEM computer with standard I/O commands. Once initiated, however, the diskette controller completes the specified operation without further intervention on the part of the CPU. Only three general steps are performed by the CPU to complete any diskette operation:

1. The CPU must prepare and store in system memory an I/O parameter block (IOPB) for each operation to be performed. If multiple operations are desired, the IOPBs can be linked together in the proper order.
2. The CPU then passes the memory address of the first (or only) IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation.

IOPB Format — In preparing the IOPB, the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared, utilizing the following format for the 10-byte parameter block:

Byte	Command
1	Channel word
2	Diskette instruction
3	Number of records
4	Track address
5	Sector address
6	Buffer address (lower)
7	Buffer address (upper)
8	Block number
9	Next IOPB address (lower)
10	Next IOPB address (upper)

Channel Command Function — The channel word provides the controller with information to determine the method of assigning logical sector addresses, enable or disable a series of possible diskette interrupts, determine if the parameter block is properly prepared, and determine the length of the data word to be transferred.

Go/No Go Diagnostic — For OEM convenience, Intel makes available a diskette exerciser and monitor program to facilitate checkout and debugging of OEM-built systems using Intel OEM computers and diskette con-

trollers. The iSBC 915 and iSBC 925 go/no go diagnostic programs are available on four 1K-byte ROMs for installation in the PROM/ROM memory section of Intel computers. The programs include commands to display and alter main memory and registers, insert instructions, move main memory, substitute main memory, and exer-

cise the flexible diskette drives by reading and/or writing individual sectors, reading sequentially sector-to-sector and track-to-track, and writing/reading random sectors and tracks. The go/no go diagnostic program is designed to provide a convenient means of determining the functionality of any OEM system.

SPECIFICATIONS

Access Time

Track-to-Track — 10 ms

Head Settling Time — 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm

Average Latency — 83 ms

Recording Mode — Frequency modulation

Physical Characteristics

CONTROLLER

Mounting — Occupies two slots of System 80 chassis or iSBC 604/614 cardcage

Height — 6.75 in. (17.15 mm)

Width — 12.00 in. (30.48 mm)

Depth — 0.50 in. each board (1.27 mm)

CHASSIS AND DRIVES

Mounting — Table-top or standard 19 in. RETMA cabinet

Height — 12.08 in. (30.68 cm)

Width — 16.88 in. (42.88 cm)

Depth — 19.0 in. (48.26 cm)

Weight — 1 drive — 51 lb (23 kg); 2 drives — 64 lb (29 kg)

Electrical Characteristics

CONTROLLER

DC Power Requirements

Channel Board: 5V @ 3.75A typ, 5A max

Interface Board: 5V @ 1.5A typ, 2.5A max

CHASSIS

DC Power Requirements

Voltage	Current
5V	3A \pm 5%
-5V	600 mA \pm 5%
24V	4A \pm 5%

AC Power Requirements

3-wire input with center conductor (earth ground) tied to chassis.

Single-phase: 115/230V AC; 50-60Hz; 160W

Environmental Characteristics

MEDIA

Temperature — 15.6°C to 51.7°C operating; 5°C to 55°C non-operating

Humidity — 8% to 80% (wet bulb 29.4°C) operating; 8% to 90% non-operating

CONTROLLER BOARDS

Temperature — 0°C to 55°C operating; -55°C to 85°C non-operating

Humidity — Up to 90% relative humidity without condensation, operating; all conditions without condensation of water or frost, non-operating

CHASSIS AND DRIVES

Temperature — 10°C to 38°C operating; -35°C to 65°C non-operating

Humidity — 20% to 90% (wet bulb 26.7°C) operating; 5% to 95% non-operating

Equipment Supplied

Cabinet, power supplies, line cord
Diskette drive(s)
FDC channel board
FDC interface board
Dual auxiliary connector
Flexible diskette controller cable
Peripheral cable

Optional Equipment

iSBC 915 go/no go diagnostic and monitor program for iSBC 80/10 and System 80/10

iSBC 925 go/no go diagnostic and monitor program for iSBC 80/20 and System 80/20

Reference Manuals

9800349 — iSBC 211/212 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 211/110V/220V	Single Drive Single Density Diskette Hardware System
SBC 212/110V/220V	Dual Drive Single Density Diskette Hardware System



iSBC 508 I/O EXPANSION BOARD

iSBC-80 I/O expansion via direct bus interface

Four 8-bit terminated input ports

Four 8-bit output ports with buffered TTL drivers

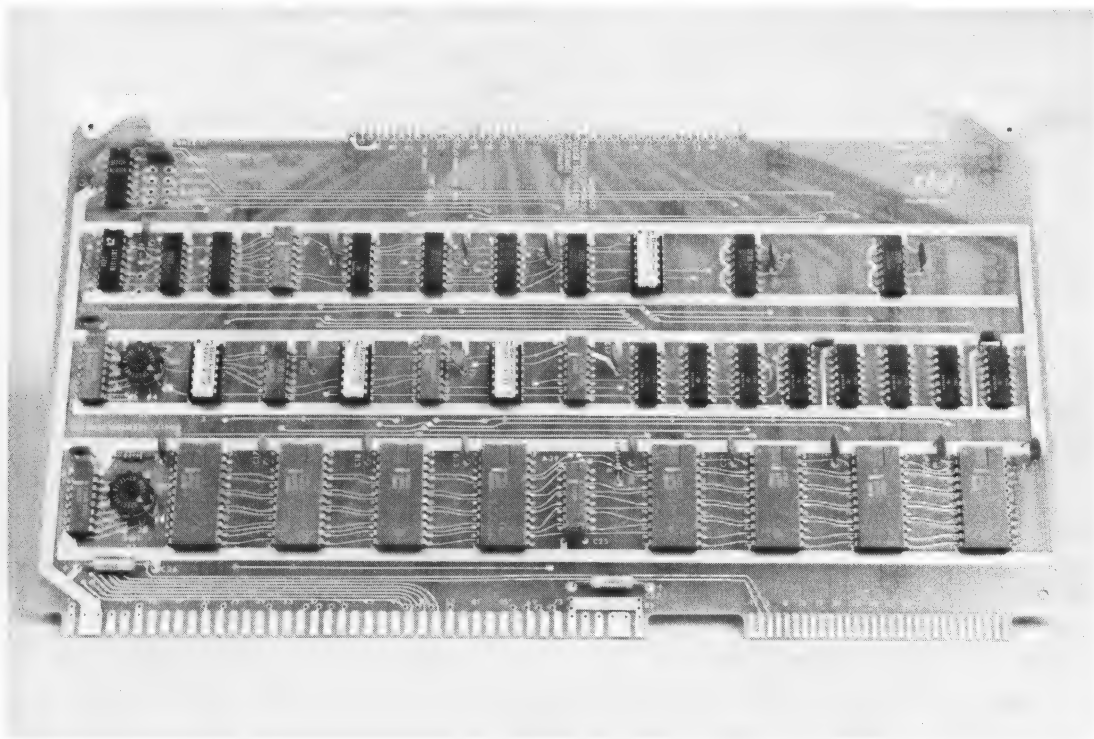
Selectable latched or unlatched input ports

Latched outputs with selectable width strobes

Switch selectable I/O port addresses

The iSBC-508 I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 508 interfaces directly to any iSBC 80 single board computer via the system bus to expand input and output port capacity. Four 8-bit terminated input ports are contained on the board. Data is gated into the port while the strobe is present and latched if the strobe is removed. The iSBC 508 contains four 8-bit output ports. All output lines are driven by TTL level buffer drivers residing on the board. Output data is latched. A strobe signal of jumper selectable width is sent to the peripheral device during an output operation. Address selection is accomplished using two resident rotary switches to select one of 64 unique base addresses for all input and output ports. The board operates with a single +5V power supply.

EXPANSION
BOARDS



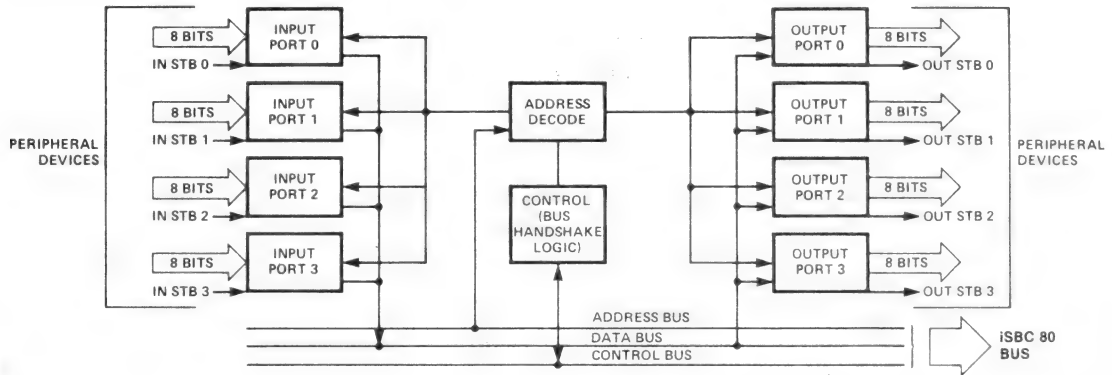


Figure 1. iSBC 508 I/O Expansion Board Block Diagram

SPECIFICATIONS

Word Size

8 bits

Capacity

Four 8-bit input ports; four 8-bit output ports.

Address Selection

Input and output ports are accessed as four sequential addresses starting in one of 64 switch selectable locations between 00 and FC₁₆.

I/O Interface Characteristics

All I/O interface data and control signals are TTL levels.

I/O Line Driver Sink Current — 48 mA

I/O Line Terminator Load — 1 k Ω pullup

Inputs — Data positive relative to data bus

Outputs — Data positive relative to data bus

Output Strobe — Jumper selectable to 100, 200, 400, 800, or 1600-ns pulse widths

Bus Interface Characteristics

All address, data, and control signals are TTL compatible.

Connectors

Bus Edge Connector — 86-pin double-sized PC edge connector with 0.156-in. contact centers

Mating Connector — Control Data VPB01E43A00A1

I/O Edge Connector — 100-pin double-sided PC edge connector with 0.1 in. contact centers

Mating Connector — Viking 3VH50/1JN5

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12 oz (415.2 gm)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$

$I_{CC} = 2.6A$ max, 1.9A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800278 — iSBC 508 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 508	I/O Expansion Board



iSBC 519 PROGRAMMABLE I/O EXPANSION BOARD

iSBC 80 I/O expansion via direct bus interface

72 programmable I/O lines with sockets for interchangeable line drivers and terminators

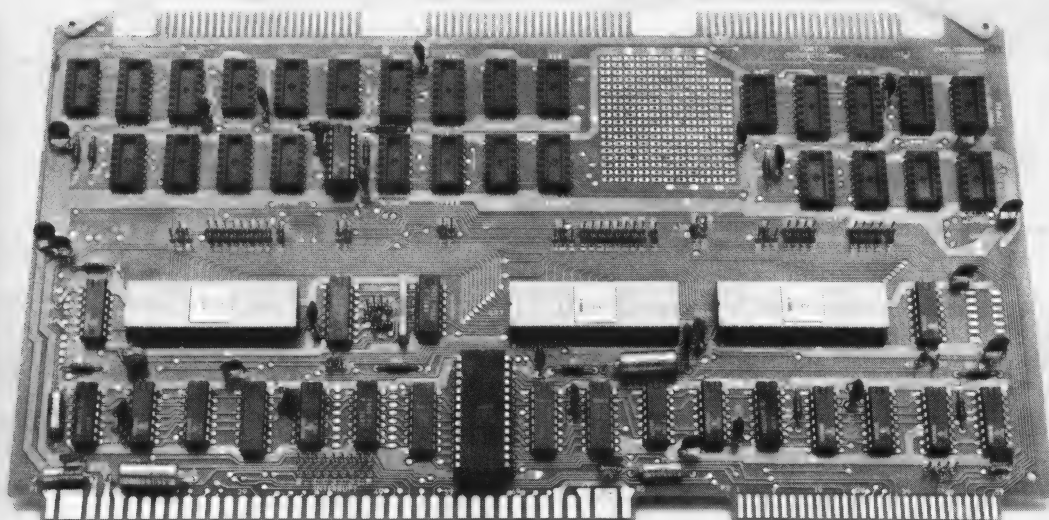
Jumper selectable I/O port addresses

Jumper selectable 0.5, 1.0, 2.0, or 4.0 ms interval timer

Eight maskable interrupt request lines with priority encoded and programmable interrupt algorithms

The iSBC 519 Programmable I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 519 interfaces directly to any iSBC 80 single board computer via the system bus to expand input and output port capacity. The iSBC 519 provides 72 programmable I/O lines. The system software is used to configure the I/O lines to meet a wide variety of peripheral requirements. The flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. Address selection is accomplished by using wire-wrap jumpers to select one of 16 unique base addresses for the input and output ports. The board operates with a single +5V power supply.

EXPANSION
BOARDS



FUNCTIONAL DESCRIPTION

The 72 programmable I/O lines on the ISBC 519 are implemented utilizing three Intel 8255 programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. The 72 programmable I/O lines and signal ground lines are brought out to three 50-pin edge connectors that mate with flat, round, or woven cable.

Interval Timer

Typical I/O read access cycle time is 350 nanoseconds.
Typical I/O read/write cycle time is 450 nanoseconds.

The interval timer provided on the ISBC 519 may be used to generate real time clocking in systems requiring the periodic monitoring of I/O functions. The time interval is derived from the ISBC 80 constant clock (BUS CCLK) and the timing interval is jumper selectable. Intervals of 0.5, 1.0, 2.0, and 4.0 milliseconds may be selected when an ISBC 80 single board computer is used to generate the clock. Other timing intervals may be generated if the user provides a separate constant clock reference in the system.

Eight-Level Vectored Interrupt

An Intel 8259 programmable interrupt controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 2, a selection of three priority processing algorithms is available to the system designer so that the

Ports	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1,4,7	8	X	X	X	X		
2,5,8	8	X	X	X	X		
3,6,9	4	X		X		X ^{1,2,3}	
	4	X		X		X ^{1,2,3}	

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.
3. Part of port 9 must be used as a control port when either port 7 or port 8 are used as a latched and strobed input or a latched and strobed output port or port 7 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

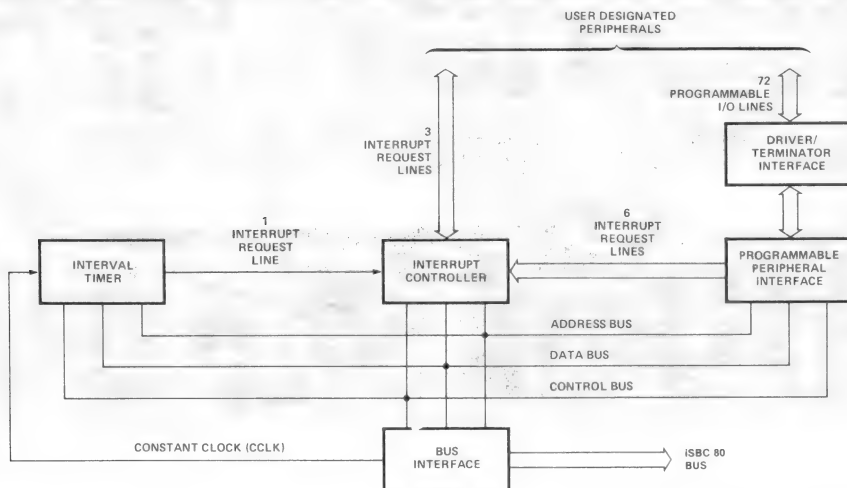


Figure 1. ISBC 519 Programmable I/O Expansion Board Block Diagram

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels are based in sequence numerically on this assignment.

Table 2. Interrupt Priority Options

manner in which requests are serviced may be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel I/O interfaces, the interval timer, or direct from peripheral equipment. The PIC then determines which of the

incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the system master. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the interrupt mask register of the PIC.

Interrupt Request Generation — Interrupt requests may originate from 10 sources. Six jumper selectable interrupt requests can be automatically generated by the programmable peripheral interfaces when a byte of information is ready to be transferred to the system master (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Three interrupt request lines may be interfaced to the PIC directly from user designated peripheral devices via the I/O edge connectors. One interrupt request may be generated by the interval timer.

Bus Line Drivers — The PIC interrupt request output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus. Any of the on-board request lines may also drive any iSBC 80 bus interrupt line directly via jumpers and buffers on the board.

SPECIFICATIONS

Addressing

Port	1	2	3	8255 No. 1 Control	4	5	6	8255 No. 2 Control	7	8	9	8255 No. 3 Control
Address	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	XA	XB

Interrupts

Register Addresses (hex notation, I/O address space)

- XD Interrupt request register
- XC In-service register
- XD Mask register
- XC Command register
- XD Block address register
- XC Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Ten interrupt request lines may originate from the programmable peripheral interface (6 lines), or user specified devices via the I/O edge connector (3 lines), or interval timer (1 line).

Interval Timer

Output Register — Timer interrupt register output is cleared by an output instruction to I/O address XE or XF¹.

Timing Intervals — 500, 1,000, 2,000, and 4,000 ms $\pm 1\%$; jumper selectable².

Notes

1. X is any hex digit assigned by jumper selection.

2. Assumes iSBC 80 constant clock (CCLK) frequency of 9.216 MHz $\pm 1\%$.

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary ¹	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector heights and wirewrap pin lengths are not guaranteed to conform to Intel OEM or System packaging.

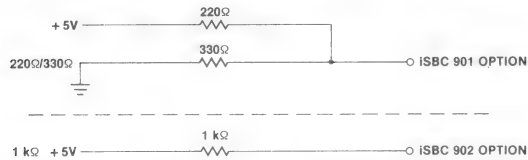
Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 519:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open-collector.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pullup

Ports 1, 4, and 7 may use any of the drivers or terminators shown above for unidirectional (input or output) port configurations. Either terminator and the following bidirectional drivers and terminators may be used for ports 1, 4, and 7 when these ports are used as bidirectional ports.

Bidirectional Drivers

Driver	Characteristic	Sink Current (mA)
Intel 8216	NI, TS	25
Intel 8226	I, TS	50

Note

I = inverting; NI = non-inverting; TS = three-state.

Terminators (for ports 1, 4, and 7 when used as bidirectional ports)

Supplier	Product Series
CTS	760-
Dale	LDP14k-02
Beckman	899-1

Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Commands	Tri-state	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (397.3 gm)

Electrical Characteristics**Average DC Current**

Voltage	Without Termination ¹	With Termination ²
$V_{CC} = +5V \pm 5\%$	$I_{CC} = 1.5A \text{ max}$	3.5A max

Note

- Does not include power required for optional I/O drivers and I/O terminators.
- With 18 220Ω/330Ω Input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manuals

9800385 — iSBC 519 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 519	Programmable I/O Expansion Board



iSBC 556 OPTICALLY ISOLATED I/O BOARD

iSBC 80 and MULTIBUS compatible

Up to 48 digital optically isolated input/output data lines

Choice of

- 24 fixed input lines
- 16 fixed output lines
- 8 programmable lines

Provisions for plug-in, optically isolated receivers, drivers, and terminators

Voltage/current levels

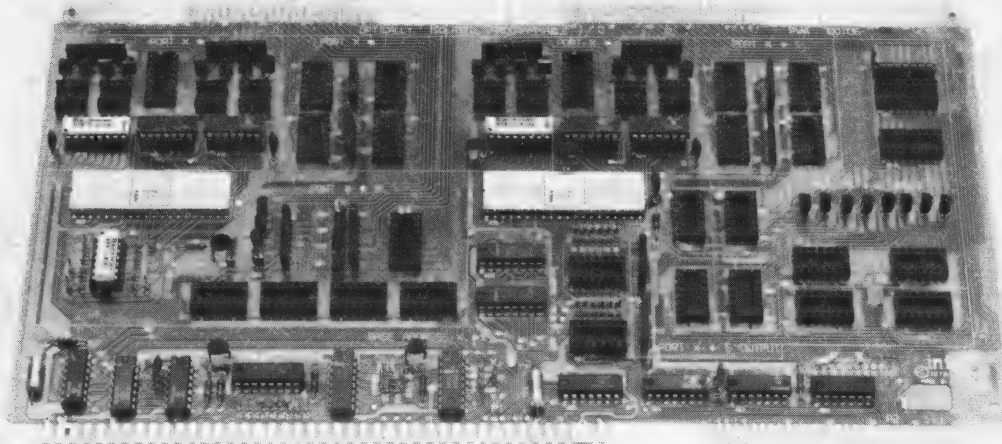
- Input up to 48V
- Output up to 30V, 60 mA

Common interrupt for up to 8 sources

+ 5V supply only

EXPANSION
BOARDS

The iSBC 556 Optically Isolated I/O Board provides 48 digital input/output lines with isolation between process application or peripheral device and the iSBC 80 series single board computers. The iSBC 556 contains two 8255A programmable interface devices, and sockets for user supplied optically isolated drivers, receivers, and input resistor terminators, together with common interrupt logic and iSBC 80 bus interface logic. Input signals can be single-ended or differential types with user defined input range (resistor terminator and opto-isolated receiver selection), allowing flexibility in design of voltage and threshold levels. The output allows user selection of Opto-Isolated Darlington Pair which can be used as an output driver either as an open collector or current switch.



FUNCTIONAL DESCRIPTION

The iSBC 556 contains 48 input/output lines configured in the following manner to allow complete optical isolation:

- 24 fixed input lines
- 16 fixed output lines
- 8 programmable input/output lines (in 4-bit increments)

The sockets provided for optically isolated receivers and drivers are in increments of 2 lines, allowing a high

degree of flexibility not usually associated on optically isolated digital input/output capability with microcomputers. (See Table 1 for selection of optically isolated receivers, drivers, and terminators.) Up to 8 lines of interrupt sources can be common to the iSBC bus interrupt line when strapped to the isolated input and programmable I/O lines, allowing level change optically isolated interrupts. (See Figure 1 for the iSBC 556 block diagram.) Addressing the iSBC 556 is base I/O address jumper selectable and must be on 8-byte boundary (evenly divisible by 8).

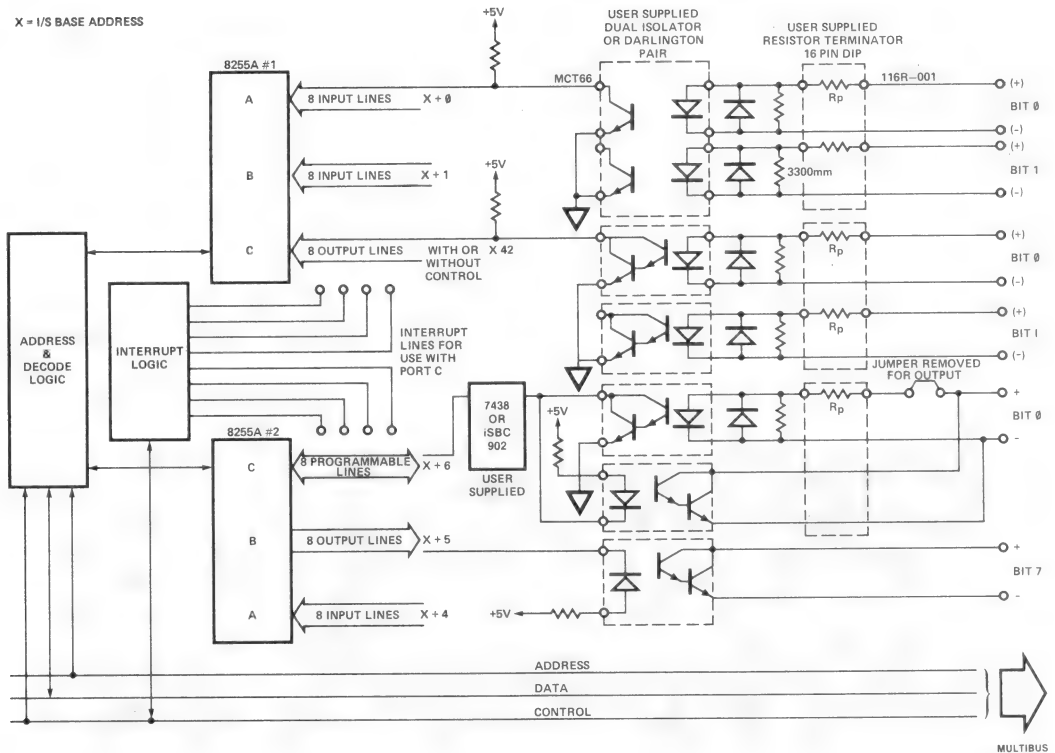


Figure 1. iSBC 556 I/O Board Block Diagram

Port No. X = I/O Base Address	Type of I/O	Lines (qty)	Resistor Terminator Pac Rp 16-Pin DIP Bourns 4116R-00 or Equivalent	Dual Opto-Isolator 8-Pin Dip Monsanto MC T66 or Equivalent	Dual Opto-Isolator Darlington Pair 6-Pin DIP Monsanto 4N29, 30 31, 32 or Equivalent	Driver 7438 or Equivalent	Pull-Up iSBC 902
X + 0	Input	8	1	4	—	—	
X + 1	Output	8	—		8	—	
X + 2	Input/ Control	8	1		8	—	
X + 4	Input	8	1	4	—	—	
X + 5	Output	8			8	—	
X + 6	Input/ Output	8	1 if input		8	2 if output	2 if input
X + 7	Control						

Table 1. I/O Ports Opto-Isolator Receivers, Drivers, And Terminators

EXPANSION
BOARDS

SPECIFICATIONS

Number of Lines

24 input lines

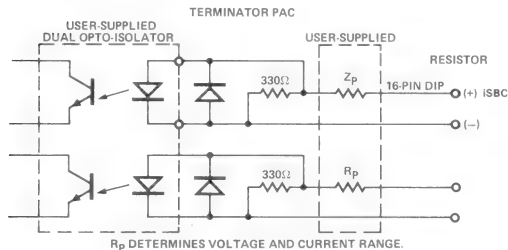
16 output lines

8 programmable lines: 4 input — 4 output

I/O Interface Characteristics

Line-to-Line Isolation — 235V DC or peak AC

Input/Output Isolation — 500V DC or peak AC



Bus Interface Characteristics

All data address and control commands are iSBC 80 bus compatible.

I/O Addressing

Port	8255 #1			Control	8255 #2			Control
	A	B	C		A	B	C	
Address	X + 0	X + 1	X + 2	X + 3	X + 4	X + 5	X + 6	X + 7

Where:

base address is from 00H to 1FH (jumper selectable)

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		In.	cm	
P1 iSBC bus	86	0.156		CDCVPB01E43A00A1
J1 16 fixed input and 8 fixed output lines	50	0.1		3M 3415-000 or TI M312125
J2 8 fixed output, 8 fixed output, and 8 programmable input/output lines	50	0.1		3M 3415-000 or TI M312125

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 12 oz (397.3 gm)

Electrical Characteristics

Average DC Current

 $V_{CC} = +5V \pm 5\%$, 1.0A without user supplied isolated receiver/driver $I_{CC} = 1.6A$ max with user supplied isolator receiver/driver

Environmental Characteristics

Temperature — 0°C to 55°C

Relative Humidity — 0 to 90%, non-condensing

Reference Manuals

9800489 — iSBC 556 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 556	Optically Isolated I/O Board

EXPANSION
BOARDS



iSBC 534

FOUR CHANNEL COMMUNICATION EXPANSION BOARD

iSBC 80 serial I/O expansion through four programmable synchronous and asynchronous communications channels

Individual software programmable baud rate generation for each serial I/O channel

Two independent programmable 16-bit interval timers

Sixteen maskable interrupt request lines with priority encoded and programmable interrupt algorithms

Jumper selectable interface register addresses

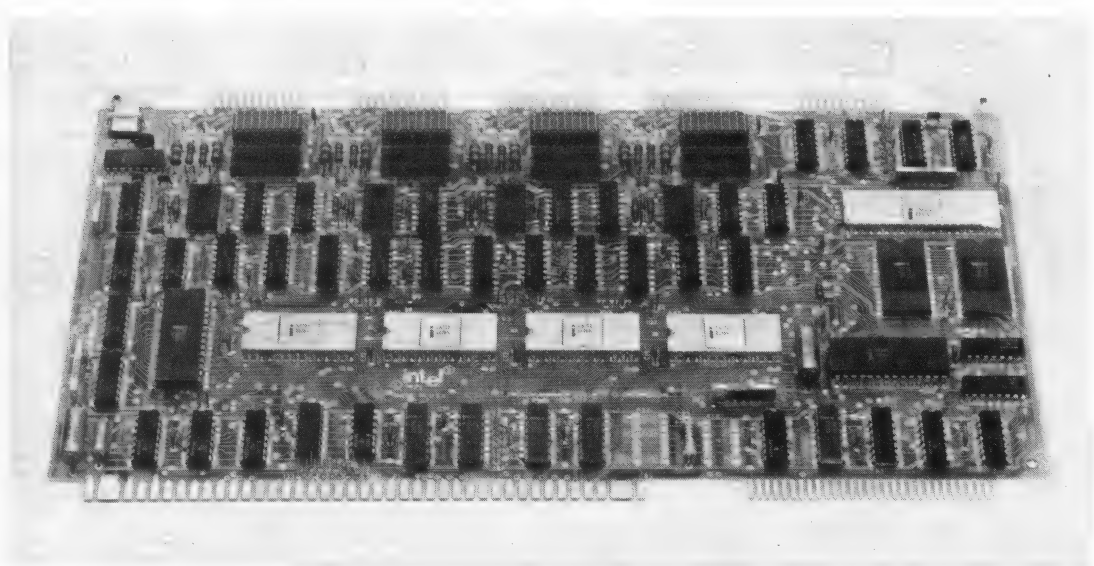
16-Bit parallel I/O interface compatible with Bell 801 automatic calling unit

RS232C/CCITT V.24 interfaces plus 20 mA optically isolated current loop interfaces (sockets)

Programmable digital loopback for diagnostics

Interface control for auto answer and auto originate modems

The iSBC 534 Four Channel Communication Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 534 interfaces directly to any iSBC 80 single board computer via the system bus to provide expansion of system serial communications capability. Four fully programmable synchronous and asynchronous serial channels with RS232C buffering and provision for 20 mA optically isolated current loop buffering are provided. Baud rates, data formats, and interrupt priorities for each channel are individually software selectable. In addition to the extensive complement of EIA Standard RS232C signals provided, the iSBC 534 provides 16 lines of RS232C buffered programmable parallel I/O. This interface is configured to be directly compatible with the Bell Model 801 automatic calling unit. These capabilities provide a flexible and easy means for interfacing iSBC 80 and System 80 based systems to RS232C and optically isolated current loop compatible terminals, cassettes, asynchronous and synchronous modems, and distributed processing networks.



EXPANSION
BOARDS

FUNCTIONAL DESCRIPTION

Communications Interface

Four programmable communications interfaces using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) are contained on the board.* Each USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e. synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. Each 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in each USART. Each set of RS232C command lines, serial data lines, and signal ground lines are brought out to 26-pin edge connectors that mate with RS232C flat or round cables.

16-Bit Interval Timers

The iSBC 534 provides six fully programmable and independent BCD and binary 16-bit interval timers utilizing two Intel 8253 programmable interval timers.* Four timers are available to the systems designer to generate baud rates for the USARTs under software control. Routing for the outputs from the other two counters is jumper selectable. Each may be independently routed to the programmable interrupt controller to provide real time clocking or to the USARTs (for applications requiring different transmit and receive baud rates). In utilizing the iSBC 534, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given baud rate or

time delay is needed, software commands to the programmable timers select the desired function. Three functions of these timers are supported on the iSBC 534, as shown in Table 1. The contents of each counter may be read at any time during system operation.

Function	Operation
Interrupt on terminal count	When terminal count is reached an interrupt request is generated. This function is used for the generation of real-time clocks.
Rate generator	Divide by N counter. The output will go low for one input clock cycle and high for N - 1 input clock periods.
Square wave rate generator	Output will remain high for one-half the count and low for the other half of the count.

Table 1. Programmable Timer Functions

Interrupt Request Lines

Two independent Intel 8259 programmable interrupt controllers (PIC's) provide vectoring for 16 interrupt levels.* As shown in Table 2, a selection of three priority processing algorithms is available to the system designer. The manner in which requests are serviced may thus be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the interrupt mask register of each PIC. Each PIC's interrupt request

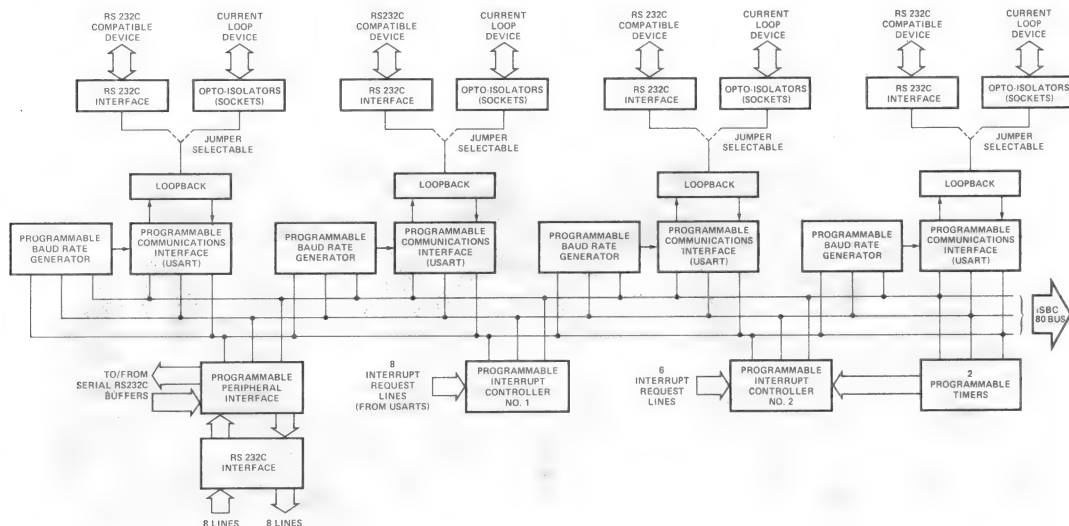


Figure 1. iSBC 534 Four Channel Communications Expansion Board Block Diagram

output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus.

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.

Table 2. Interrupt Priority Options

Interrupt Request Generation — As shown in Table 3, interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests (8 total) can be automatically generated by each USART when a character is ready to be transferred to the iSBC 80 system bus (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). Jumper selectable requests can be generated by two of the programmable timers (PITs), and six lines are routed directly from peripherals to accept carrier detect (4 lines), ring indicator, and the Bell 801 present next digit request lines.

Systems Compatibility

The iSBC 534 provides 16 RS232C buffered parallel I/O lines implemented utilizing an Intel 8255 programmable

Interrupt Request Line	PIC 0	PIC 1
0	PORT 0 R _X RDY	PIT 1 counter 1
1	PORT 0 T _X RDY	PIT 2 counter 2
2	PORT 1 R _X RDY	Ring indicator (all ports)
3	PORT 1 T _X RDY	Present next digit
4	PORT 2 R _X RDY	Carrier detect port 0
5	PORT 2 T _X RDY	Carrier detect port 1
6	PORT 3 R _X RDY	Carrier detect port 2
7	PORT 3 T _X RDY	Carrier detect port 3

Table 3. Interrupt Assignments

peripheral interface (PPI) configured to operate in mode 0.* These lines are configured to be directly compatible with the Bell 801 automatic calling unit (ACU). This capability allows the iSBC 534 to interface iSBC 80 and System 80-based systems to Bell 801 type ACUs and up to four modems or other serial communications devices. For systems not requiring interface to an ACU, the parallel I/O lines may also be used as general purpose RS232C compatible control lines in system implementation.

*Complete operational details on the Intel 8251 USART, the Intel 8253 Programmable Interval Timer, the Intel 8255 Programmable Peripheral Interface, and the Intel 8259 Programmable Interrupt controller are contained in the Intel 8080 Microcomputer System User's Manual and 8085 Microcomputer System User's Manual.

SPECIFICATIONS

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Sample Baud Rates¹

Frequency ² (kHz, Software Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous
		÷ 16 ÷ 64
153.6	—	9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
6.98	6980	— 110

Notes:

1. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit programmable interval timer (used here as frequency divider).

2. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

Interval Timer and Baud Rate Generator Frequencies

Input Frequency (On-Board Crystal Oscillator) — 1.2288 MHz ± 10% (0.813 µs period, nominal)

Function	Single Timer		Dual/Timer Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt Interval	1.63 µs	53.3 ms	3.26 µs	58.25 minutes
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.0029 Hz	307.2 kHz

Interfaces — RS232C Interfaces

EIA Standard RS232C Signals provided and supported:

Carrier detect	Receive data
Clear to send	Ring indicator
Data set ready	Secondary receive data
Data terminal ready	Secondary transmit data
Request to send	Transmit clock
Receive clock	Transmit data

Parallel I/O — 8 input lines, 8 output lines, all signals RS232C compatible

Bus — All signals iSBC 80 bus compatible

I/O Addressing

The USART, interval timer, interrupt controller, and parallel interface registers of the iSBC 534 are configured as a block of 16 I/O address locations. The location of this block is jumper selectable to begin at any 16-byte I/O address boundary (i.e., 00H, 10H, 20H, etc.).

I/O Access Time

400 ns USART registers
 400 ns Parallel I/O registers
 400 ns Interval timer registers
 400 ns Interrupt controller registers

Compatible Connectors/Cable

Interface	Pins (qty)	Centers (in.)	Mating Connectors	Cable
Bus	86	0.156	CDC VPB01E43A00A1	N/A
Serial and parallel I/O	26	0.1	3M 3462-000 or TI H312113	Intel iSBC 955

Compatible Opto-Isolators

Function	Supplier	Part Number
Driver	Fairchild General Electric Monsanto	4N33
Receiver	Fairchild General Electric Monsanto	4N37

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (398 gm)

Electrical Characteristics**Average DC Current**

Voltage	Without Opto-Isolators	With Opto-Isolators ¹
V _{CC} = +5V	1.9 A, max	1.9 A, max
V _{DD} = +12V	275 mA, max	420 mA, max
V _{AA} = -12V	250 mA, max	400 mA, max

Note

1. With four 4N33 and four 4N37 opto-isolator packages installed in sockets provided to implement four 20 mA current loop interfaces.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manuals

9800450 — iSBC 534 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 534	Four Channel Communication Expansion Board



iSBC 517 COMBINATION I/O EXPANSION BOARD

I/O addressing and connectors directly compatible with iSBC 104, iSBC 108, and iSBC 116 combination boards

48 programmable I/O lines with sockets for interchangeable line drivers and terminators

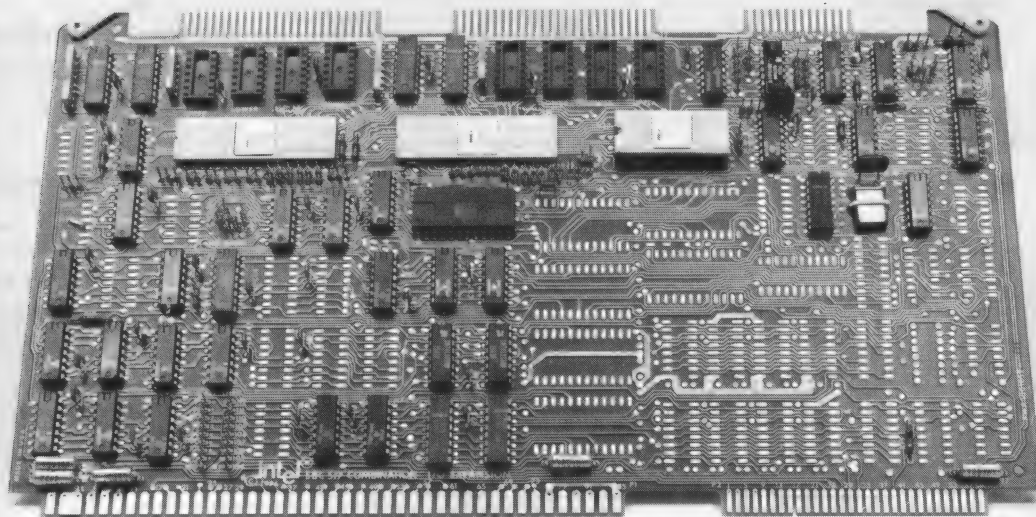
Synchronous/asynchronous communications interface with RS232C drivers and receivers

Eight maskable interrupt request lines with a pending interrupt register

1 ms interval timer

The iSBC 517 Combination I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The board interfaces directly with any iSBC 80 single board computer via the system bus to expand serial and parallel I/O capacity. The combination I/O board contains 48 programmable parallel I/O lines. The system software is used to configure the I/O lines to meet a wide variety of system peripheral requirements. The flexibility of the I/O interface is significantly enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. A programmable RS232C communications interface is provided on the iSBC 517. This interface may be programmed by the system software to provide virtually any asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). A comprehensive RS232C interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems is thus on the board. An on-board register contains the status of eight interrupt request lines which may be interrogated from the system bus, and each interrupt request line is maskable under program control. The iSBC 517 also contains a jumper selectable 1 ms interval timer and interface logic for eight interrupt request lines.

EXPANSION
BOARDS



FUNCTIONAL DESCRIPTION

Programming Flexibility

The 48 programmable I/O lines on the iSBC 517 are implemented utilizing two Intel 8255 programmable peripheral interfaces. The system software is used to configure these programmable I/O lines in any of the combinations of unidirectional input/output, and bi-directional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable. Typical I/O read access time is 280 nanoseconds. Typical I/O read cycle time is 600 nanoseconds.

Communications Interface

The programmable communications interface on the iSBC 517 is provided by an Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-

buffered transmit and receive capability, and parity, overrun, and framing error detection are all incorporated in the USART. The comprehensive RS232C interface on the board provides a direct interface to RS232C compatible equipment. The RS232C serial data lines and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables. The iSBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The iSBC 530 may be used to interface the iSBC 517 Combination I/O Expansion Board to teletypewriters and other 20 mA current loop equipment.

Interrupt Request Lines

Interrupt requests may originate from eight sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is

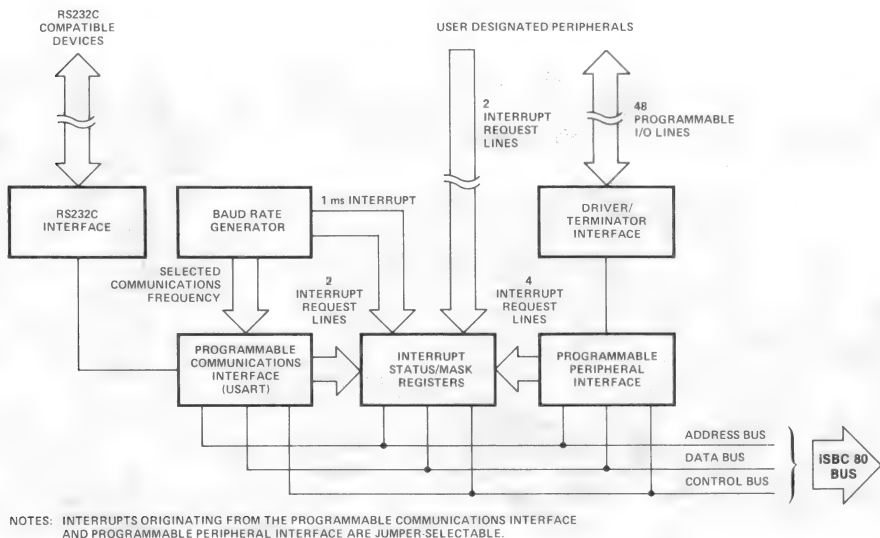


Figure 1. iSBC 517 Combination I/O Expansion Board Block Diagram

Ports	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X ¹
	4	X		X			X ¹
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X ²
	4	X		X			X ²

Notes

1. Part of port 3 must be used as control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

maskable under program control. Routing for the eight interrupt request lines is jumper selectable. They may be ORed to provide a single interrupt request line for the iSBC 80/10, or they may be individually provided to the system bus for use by the iSBC 80/20 priority interrupt controller.

Interval Timer

Each board contains a jumper selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

SPECIFICATIONS**I/O Addressing**

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note

X is any hex digit assigned by jumper selection.

I/O Transfer Rate

Parallel — Read or write cycle time 760 ns max

Serial — (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; peak characters generation; 1, 1½, or 2 stop bits; false start bit detectors.

Interrupts

Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines), or user specified devices via the I/O edge connector (2 lines) or interval timer.

Interrupt Register Address

- X1 Interrupt mask register
- X0 Interrupt status register

Note

X is any hex digit assigned by jumper selection.

Timer Interval

- 1.003 ms ± 0.1% when 110 baud rate is selected
- 1.042 ms ± 0.1% for all other baud rates

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C

Interrupt Requests — All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary ¹	60	0.1	AMP PE5-14559 or TI H311130

Note

1. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or system packaging. Auxiliary connector is used for test purposes only.

Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 517:

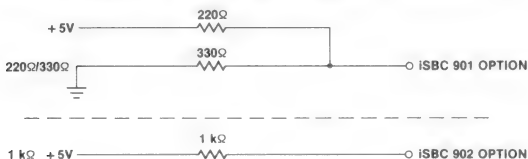
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open-collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Commands	Tri-state	25

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 14 oz (397.3 gm)

Electrical Characteristics

Average DC Current

$$V_{CC} = +5V \pm 5\%$$

$$V_{DD} = +12V \pm 5\%$$

$$V_{AA} = -12V \pm 5\%$$

$$I_{CC} = 2.4 \text{ mA max}$$

$$I_{DD} = 40 \text{ mA max}$$

$$I_{AA} = 60 \text{ mA max}$$

Note

Does not include power required for optional I/O drivers and I/O terminators. With eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manuals

9800388 — iSBC 517 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 517	Combination I/O Expansion Board



iSBC 501 DIRECT MEMORY ACCESS CONTROLLER

**Directly compatible with Intel iSBC 80
single board computers**

Block length up to 65,536 words

**Directly addresses up to 65,536 memory
locations**

**Transfer rate up to 1 million words per
second for block transfers**

Transfers initialized via software

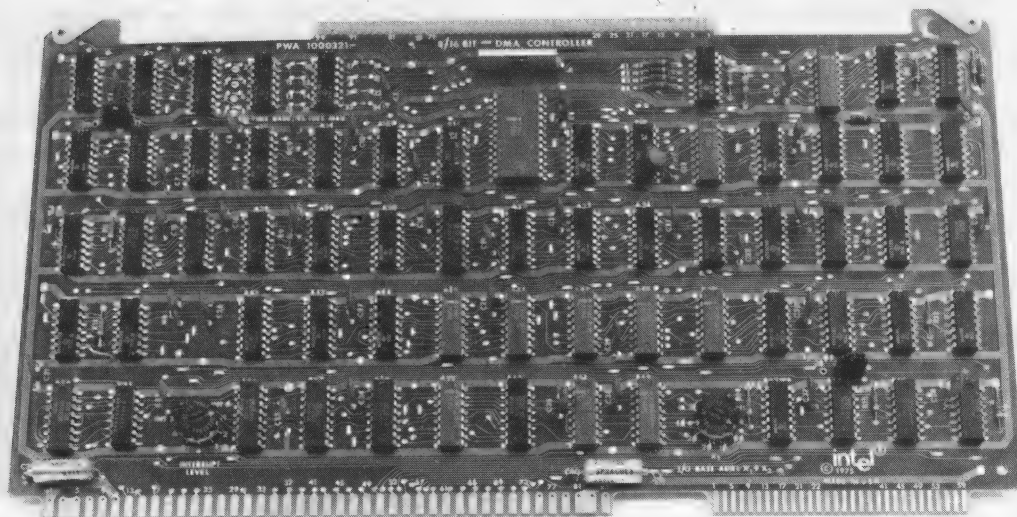
**Transfers data up to 330K words per
second for interleaved transfers**

**Software selectable/maskable interrupt
operations**

Interrupt priority switch selectable

EXPANSION
BOARDS

The iSBC 501 Direct Memory Access Controller is a member of Intel's complete line of iSBC 80 OEM computer systems. The iSBC 501 interfaces directly with any iSBC 80 single board computer based system via the system bus. High speed, direct memory access control and interfacing for transfers between iSBC 80 expansion board memory and up to 16 peripheral devices is provided.



FUNCTIONAL DESCRIPTION

Transfer Capability

Block lengths up to 65,536 bytes long may be transferred directly to or from RAM memory in iSBC 80 systems at rates up to 1 million words per second. The iSBC 501 16-bit addressing capability allows transfers to take place at any location within memory. It is designed to control the direct transfer of data to or from Intel iSBC 80 memory expansion or combination memory and I/O boards. Two transfer modes of operation are included. System software is used to select the desired mode. Transfer rates up to 330K words per second may be achieved in the shared bus mode, wherein the iSBC 501 requests access to the system bus for 600 ns to perform a transfer of one word to or from memory. The second mode, the override mode, establishes the DMA controller as the only master which may access the system bus during the transfer period, thereby providing rapid block transfer capability. This mode provides transfer rates up to 1 million words per second. Either mode may be used with the iSBC 80/20 single board computer. The iSBC 80/10

single board computer may only interact with the iSBC 501 in the shared bus mode. Four timing strobes are provided for the control of data input transfers and four timing strobes are provided for output transfer operations. Strokes are initiated and selected via system software, and strobe pulses are jumper selectable to 100, 200, 400, 800, or 1600 ns widths.

Interrupt Requests

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selected DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Peripheral Interface

A 4-bit tag register is provided which may be used as a device select port to provide selection for four (up to 16 with external decoding) high speed peripheral devices interfacing through the iSBC 501.

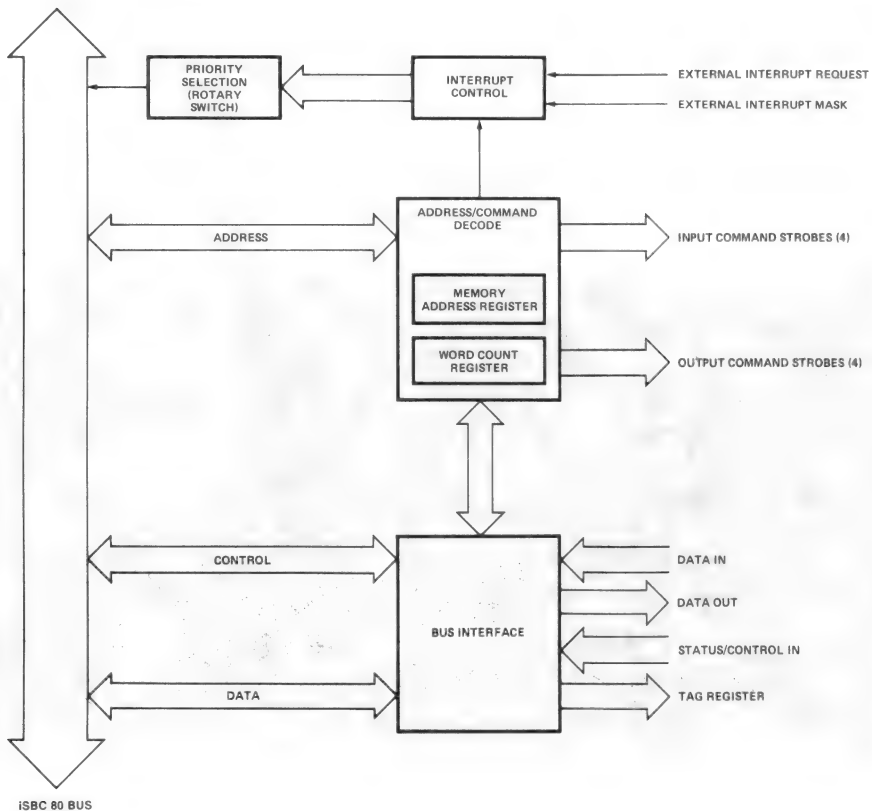


Figure 1. iSBC 501 DMA Controller Block Diagram

SPECIFICATIONS

Word Size

8 bits

Block Size

65,536 words, max

Address Capability

65,536 words

Transfer Rates

Mode	Transfer Rates (K bytes/sec) ¹			
	Memory Read Operations		Memory Write Operations	
	Typical	Worst Case ³	Typical	Worst Case ³
Shared bus, CPU halted ²	330	270	330	270
Shared bus, CPU executing code ²	180	160	180	160
Override	1000	660	1000	660

Notes

1. Transfer rates given are to and from RAM memory on iSBC 104 or iSBC 108 combination memory and I/O boards.

2. Shared bus mode may be used with Intel iSBC 80/10 or Intel iSBC 80/20. iSBC 80/20 may also operate in override mode.

3. Assumes every DMA transfer must wait for RAM refresh cycle to be completed, worst case memory cycle times.

Interrupts

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selectable DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Key Registers

Control Register (6 bits) — The contents of the control register specify the busy status of the DMA board, the type of operation to be performed (transfer or non-transfer), the transfer direction (to or from memory), the interrupt condition (enabled or disabled), and the means by which the DMA board is using the system bus (shared mode or override mode).

Memory Address Register (16 bits) — Contains the address of the next memory location to be accessed by the iSBC 501. Loaded from the CPU, prior to a transfer operation, with the address of the first memory location to be accessed. The address is gated onto the system address bus during each transfer, and incremented by one for each word transferred.

Length Register (16 bits) — Contents of this register specify the total number of words to be transferred. This word count is decremented by one after each word is transferred. The transfer stops when the word count equals zero.

Tag Register (4 bits) — The contents of the tag register are used as control/select lines to the external peripheral devices being interfaced by the iSBC 501 (e.g., as the "go" command line to each of four devices), or the tag register outputs may be used with external decoding to expand the maximum number of DMA peripherals to 16.

Status Register (8-bits) — Provides 4 bits of DMA controller status: software interrupt, memory read/write operation requested, external/end-of-transfer interrupt, and DMA controller busy. The status register also provides four status/control bits directly from user peripheral devices.

Address Selection

iSBC 501 registers are located in a jumper selectable block starting at any 16-word boundary in the I/O address space.

Register Locations

Address ¹	I/O Operation	Function
X0	Output	Output strobe 0
X1	Output	Output strobe 1
X2	Output	Output strobe 2
X3	Output	Output strobe 3
X4	Output	Output tag strobe
X8	Output	Set interrupt
X9	Output	Reset interrupt
XA	Output	Load control register
XB	Output	Load tag register
XC	Output	Load LSB length register
XD	Output	Load MSB length register
XE	Output	Load LSB memory address register
XF	Output	Load MSB memory address register
X0	Input	Input command strobe 0
X1	Input	Input command strobe 1
X2	Input	Input command strobe 2
X3	Input	Input command strobe 3
X4	Input	Read LSB length register
X5	Input	Read MSB length register
X6	Input	Read DMA status
X7	Input	Invalid command

Note

1. X is any hex digit, assigned by jumpers.

Connectors

Interface	Double-sided Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43D00A1 Viking 2VH43/1AV5
I/O	100	0.100	Intel MDS 990 Viking 3VH50/1JN5

Interface Characteristics

I/O Line Driver Sink Current — 48 mA

I/O Line Terminator Load — 150Ω pullup

Input — Data positive relative to data bus

Output — Data positive relative to data bus

Output Strokes — Jumper selectable to 100, 200, 400, 800, or 1600 ns pulse widths.

All I/O interface data and control signals are TTL compatible and iSBC 80 bus compatible.

Physical Characteristics**Width** — 12.00 in. (30.48 cm)**Height** — 6.75 in. (17.15 cm)**Depth** — 0.50 in. (1.27 cm)**Weight** — 12 oz (340.5 gm)**Electrical Characteristics****DC Power Requirements** $V_{CC} = 5V \pm 5\%$ $I_{CC} = 3.35A \text{ max}; 2.70A \text{ typ}$ **Environmental Characteristics****Operating Temperature** — 0°C to 55°C**Equipment Supplied**

iSBC 501 DMA Controller Board

Reference Manuals**9800294** — iSBC 501 Hardware Reference Manual (SUPPLIED)

iSBC 501 Schematic (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 501	Direct Memory Access Controller

iSBC 711 ANALOG INPUT BOARD

iSBC 80 and MULTIBUS compatible

Up to 16 differential/32 single-ended non-isolated inputs

Fault protection on all inputs

Voltage or current loop input

Programmable gain amplifier

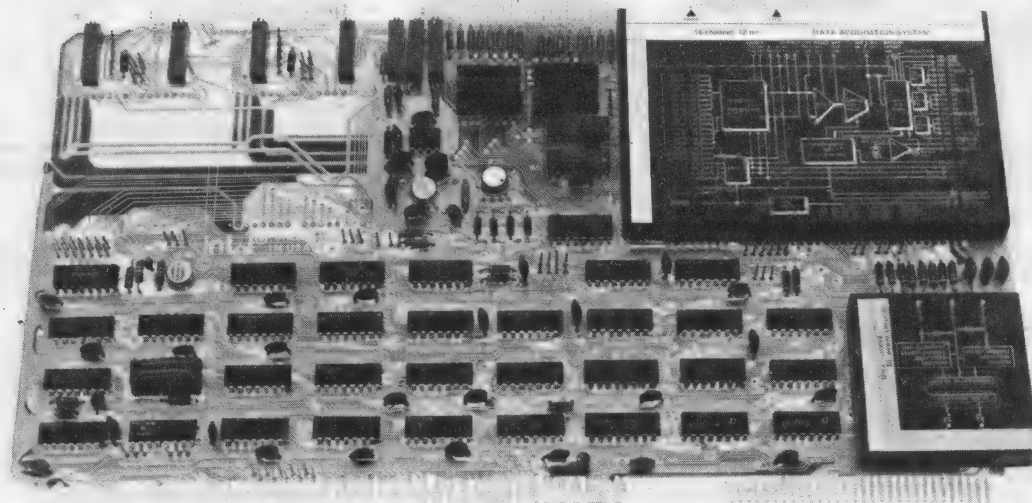
12-Bit A/D converter

Memory mapped I/O

Single +5V supply

The iSBC 711 Analog Input Board is a complete single board input subsystem which allows easy interfacing of high level analog input signals to Intel's complete line of iSBC 80 single board computers. The iSBC 711 performs the basic functions of data acquisition of analog input signals under microprocessor control. The iSBC 711 consists of 8 differential/16 single ended channel multiplexer, input protection circuits, programmable gain amplifier, sample and hold amplifier, 12-bit A/D converter, DC to DC converter, memory mapped interface, and control logic.

EXPANSION
BOARDS



FUNCTIONAL DESCRIPTION

The iSBC 711 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the iSBC 732 Analog Combination I/O Board. A block diagram of the iSBC 711 Analog Input Board is shown in Figure 1.

Input Capacity

The iSBC 711 contains an 8 differential or 16 single ended analog input multiplexer. Optionally, the iSBC 711 can be expanded up to 16 differential or 32 single ended, non-isolated input channels via two plug-in multiplexers (Part No. Harris H1818A).

Fault Protection

All input channels are protected up to $\pm 28V$ via diode clamping, together with fusible current limit resistors, limiting potentially destructive overloads under fault conditions.

Current Loop Input

The differential input channels have provisions for up to 16 user supplied 250-ohm resistors to accept 4 to 20 mA current loop inputs.

Programmable Gain Amplifier

The programmable gain amplifier allows gains of 1, 2, 4, and 8 to be specified under program control.

12-Bit A/D Converter

The A/D converter is a 12-bit 35 μs successive approximation device with sample and hold amplifier which can be jumper selected for 0 to +5V, 0 to +10V, $\pm 5V$, and $\pm 10V$ input ranges. A/D conversion can be initiated by external trigger, pacer clock, or programmed I/O. Interrupt on conversion or end of scan is a standard feature. The external trigger is useful when the A/D conversion is to be synchronized to some external event. The internal pacer clock (10 ranges jumper selectable from 976 μs to 1 sec) allows precise, evenly spaced A/D conversions where signal reconstruction is required.

OPERATIONAL DESCRIPTION

Analog Input

The iSBC 711 has three modes of operation for acquisition of analog inputs. These are:

1. Repetitive single channel input
2. Sequential input scan
3. Random channel input

Repetitive Single Channel Input — The channel is selected by a write to the multiplexer address register (MAR). The initiation of the first conversion is stated by a write to the command register (CR). Setting the appropriate bits in the command register allows stop/start, pacing, external trigger. Subsequent conversions are initiated by read of the A/D register (ADCR), or by another write to the command register.

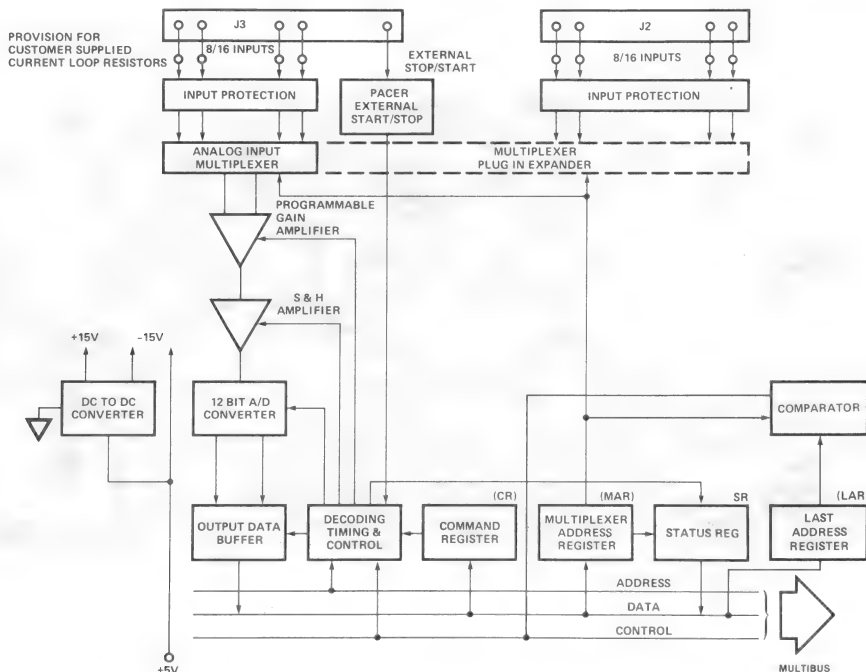


Figure 1. iSBC 711 Analog Input Board Block Diagram

Sequential Input Scan — This mode is initiated in the same manner as the repetitive single channel, except bit 1 of the command register (CR) is set to a "1" on the write command.

Random Input Scan — This mode is initiated in the same manner as repetitive single channel input; subsequent channels are selected by a write to the multiplexer address register (MAR) before a read of the current converted value from the ADCR register.

Addressing

The iSBC 711 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the iSBC 711 interfaces as memory, any of

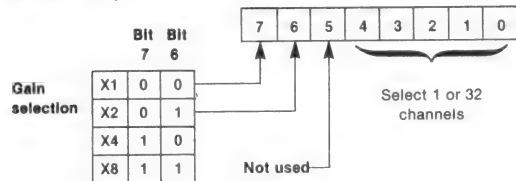
the 8080's 16-bit memory reference instructions can be used. The A/D converter is addressed as memory: base plus specific address. The base address is factory set at F700H and is jumper selectable. Table 1 shows address:

Address	Command	Function
Base + 0	Write	Write to command register
Base + 0	Read	Read status register
Base + 1	Write	Write to multiplexer address register
Base + 1	Read	Read multiplexer address register
Base + 2	Write	Write to last channel register
Base + 3	Write	Clear interrupts
Base + 4	Read	Read LS byte of A/D data
Base + 5	Read	Read MS byte of A/D data

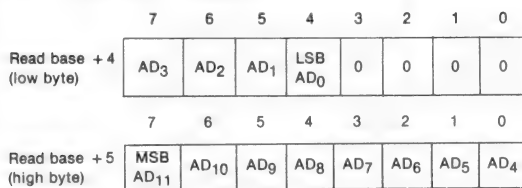
Table 1. Address Commands and Functions

SPECIFICATIONS

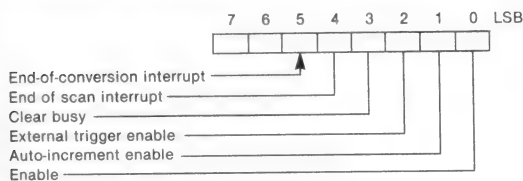
Multiplexer Address Register (MAR) (Write Base + 1)



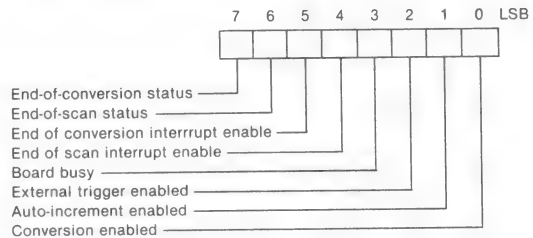
A/D Converter Register (ADCR)



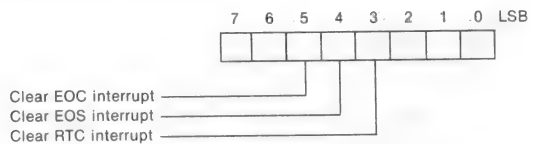
Command Register (CR) (Write Base + 0)



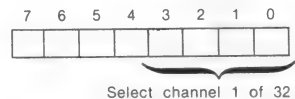
Status Register (Read Base + 0)



Clear Interrupt (Write Base + 3)



Last Address Register (LAR) (Write Base + 2)



Analog Input

Number of Input Channels — 8 differential or 16 single-ended (jumper selectable); expandable from 8/16 to 16/32 using two plug-in multiplexers (Part No. Harris H1818A).

Resolution — 12 bit bipolar or unipolar

Sample and Hold Aperture Time — <20 ns

Sample and Hold Uncertainty — 5 ns

Multiplexer Input Voltage Ranges

Gain X	A/D Input Range			
	+5V	+10V	±5V	±10V
1	+5V	+10V	±5V	±10V
2	+2.5V	+5V	±2.5V	±5V
4	1.25V	+2.5V	±1.25V	±2.5V
8	0.625V	+1.25V	±0.625V	±1.25V

Jumper
selectable

Programmable

Input Impedance

Power Off: 680 ohms

Power On: >100M ohms

Input Current Range — 0-20 mA using 250-ohm user installed resistors

Source Impedance

Balanced: <5000 ohms

Unbalanced: <1000 ohms

Overall Accuracy @ 25°C

0.05% FSR ± ½ LSB (gain × 1)

0.07% FSR ± ½ LSB (gain × 2, × 4, × 8)

(Includes 3 sigma noise, linearity, offset gain, and dynamic response errors.)

Temperature Coefficient

0.0025% FSR/°C (gain × 1)

0.0030% FSR/°C (gain × 2, × 4, × 8)

A/D Conversion Speed — 28 kHz**Throughput****Sample Rate** (Single Channel) — 17 kHz**Channel to Channel Rate** — 16kHz**Common Mode Rejection (CMR)** — 60 dB differential input**Common Mode Voltage (CMV)** — ±10.24V (signal and common mode)**Input Over-Voltage Protection** — ±28V DC, peak AC continuous**External Trigger** — TTL compatible, 1.5 μs (min) better than 50 ns risetime**Pacer Clock**

Crystal controlled accuracy 0.05%

Divider gives range of $\frac{1000}{2^n}$ ms

n=0 through 10

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		in.	cm	
P1 iSBC Bus	86	0.156		CDCVPB01E43A00A1
P2 ±15V Auxiliary power	60	0.1		
J1 Not used	50	0.1		3M3415-000 or TIH312125
J2 1st 8/16 input channels	50	0.1		3M3415-000 or TIH312125
J3 Expander 8/16 input channels	50	0.1		3M3415-000 or TIH312125

Compatible Boards and Systems

iSBC 80/05

iSBC 80/10

iSBC 80/20

System 80/10, and

System 80/20-4

Physical Characteristics**Width** — 12.00 in. (30.48 cm)**Height** — 6.75 in. (17.15 cm)**Depth** — 0.5 in. (1.27 cm)**Weight** — 1 lb (454 gm)**Electrical Characteristics****Power supply** — +5V ± 5%, 1.7A max**Environmental Characteristics**

	Reference Operating Conditions	Operative Limits	Transportation and Storage Limits
Temperature	25 ± 0.2°C	0 to 55°C	-25 to 85°C
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	+5V ± 5%	+5V ± 5%	N/A

Reference Manuals**9800486** — iSBC 711 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 711	Analog Input Board



iSBC 724 ANALOG OUTPUT BOARD

iSBC 80 and MULTIBUS compatible

Accuracy: 0.05% FSR

Four independent 12-bit D/A converters

Unipolar or bipolar with 0 to +10V, 0 to +5V, $\pm 10V$ ranges

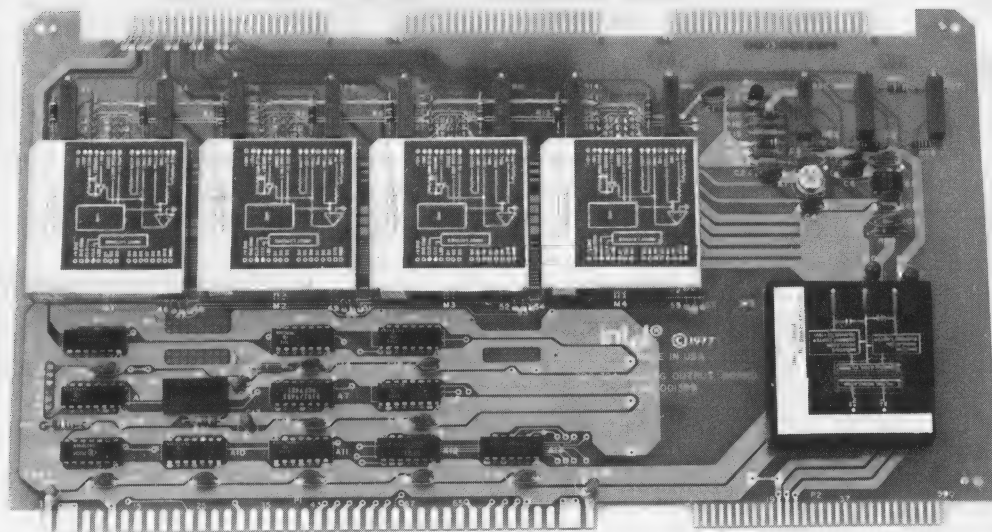
Short circuit protection on voltage output

Memory mapped I/O

Single +5V supply

The iSBC 724 is a complete single board analog output subsystem which allows easy interfacing of analog outputs from Intel's complete line of iSBC 80 series single board computers to voltage actuated devices or control elements. The iSBC 724 contains four independent 12-bit D/A converters and associated voltage output amplifiers, 8-bit holder register, DC to DC converter, memory mapped interface, and control logic.

EXPANSION
BOARDS



FUNCTIONAL DESCRIPTION

The iSBC 724 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the analog output provided on the iSBC 732 analog I/O board. Each individual D/A converter can be jumper selected for 0 to +5V, 0 to +10V, $\pm 5V$, $\pm 10V$. Short circuit protection for voltage outputs is a standard feature suitable for many display and control applications. A block diagram of the iSBC 724 analog output board is shown in Figure 1.

OPERATIONAL DESCRIPTION

Data Transfer

Data transfer to a 12-bit D/A converter is accomplished by a write of the least significant 4 bits to the holding register. When the 8 remaining bits of the upper byte are transferred, the 12 bits of data are immediately loaded into the specific D/A converter channel.

Addressing

The iSBC 724 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the iSBC 724 interfaces as memory, any of the 8080's memory reference instructions can be used. Each independent D/A converter is addressed as memory; base plus specific address. The base address is factory set at F708H which is jumper selectable. Table 1 shows addressing:

Address	Command	Function
Base + 0	Write	Write to DAC holding register
Base + 1	Write	Write to DAC 0
Base + 2	Write	Write to DAC holding register
Base + 3	Write	Write to DAC 1
Base + 4	Write	Write to DAC holding register
Base + 5	Write	Write to DAC 2
Base + 6	Write	Write to DAC holding register
Base + 7	Write	Write to DAC 3

Table 1. Address Commands and Functions

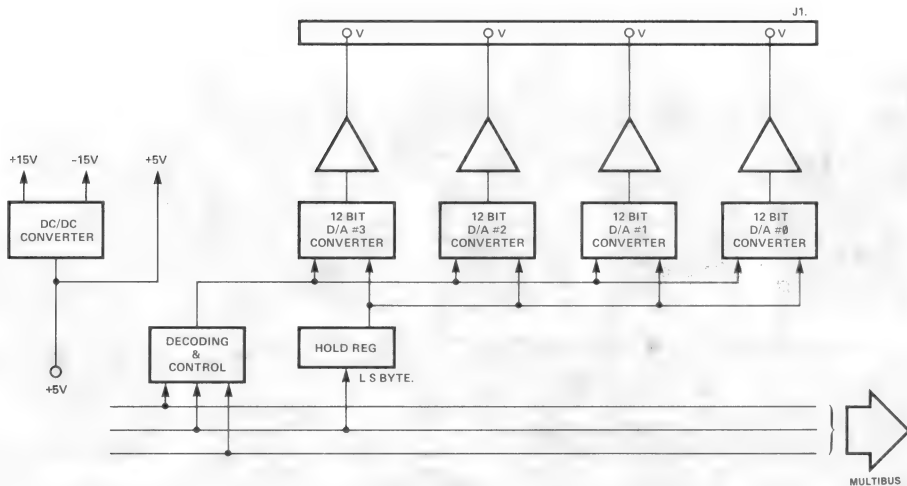
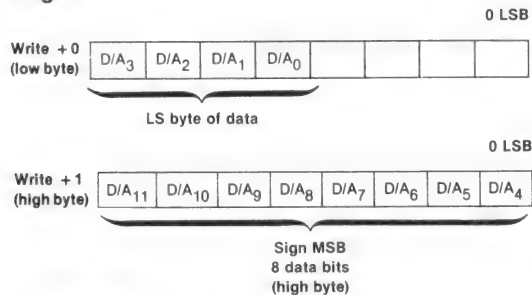


Figure 1. iSBC 724 Analog Output Board Block Diagram

SPECIFICATIONS

Registers



Analog Output

Number of Channels — 4 non-isolated

Resolution — 12 bits bipolar or unipolar (switch selectable)

Voltage Output Characteristics

Voltage Output Ranges — 0 to +5V, 0 to +10V, $\pm 5V$, $\pm 10V$ (jumper selectable)

Output Current — $\pm 5\text{ mA}$ @ $\pm 10V$

Output Impedance — 0.2 ohm

Slew Rate — $10V/\mu s$

Accuracy @ 25°C — 0.05% FSR (includes linearity and noise)

Temperature Coefficient — $0.005/^\circ C$

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		in.	cm	
P1 iSBC bus	86	0.156	.396	CDC VPB01E4300A1 3M 3415-000 or TI H312125
P2 $\pm 15V$ auxiliary power	60	0.1	.254	
J1 4 channels of analog output	50	0.1	.254	

Compatible Boards and Systems

iSBC 80/05

iSBC 80/10

iSBC 80/20

System 80/10

System 80/20-4

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 1 lb 2 oz (511 gm)

Electrical Characteristics

Power Supply — $+5V \pm 5\%$, 2.0A max

Environmental Characteristics

	Reference Operating Conditions	Operative Limits	Transportation and Storage
Temperature	$25 \pm 2.0^\circ C$	0 to $55^\circ C$	-25 to $85^\circ C$
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	$+5 \pm 5\%$	$+5V \pm 5\%$	N/A

Reference Manuals

9800486 — iSBC 724 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SBC 724 Analog Output Board

iSBC 732 ANALOG COMBINATION I/O BOARD

iSBC 80 and MULTIBUS compatible

Up to 16 differential/32 single ended non-isolated inputs

Fault protection on all inputs

Voltage or current loop input/output

Programmable gain amplifier

12-Bit, 28 kHz A/D converter

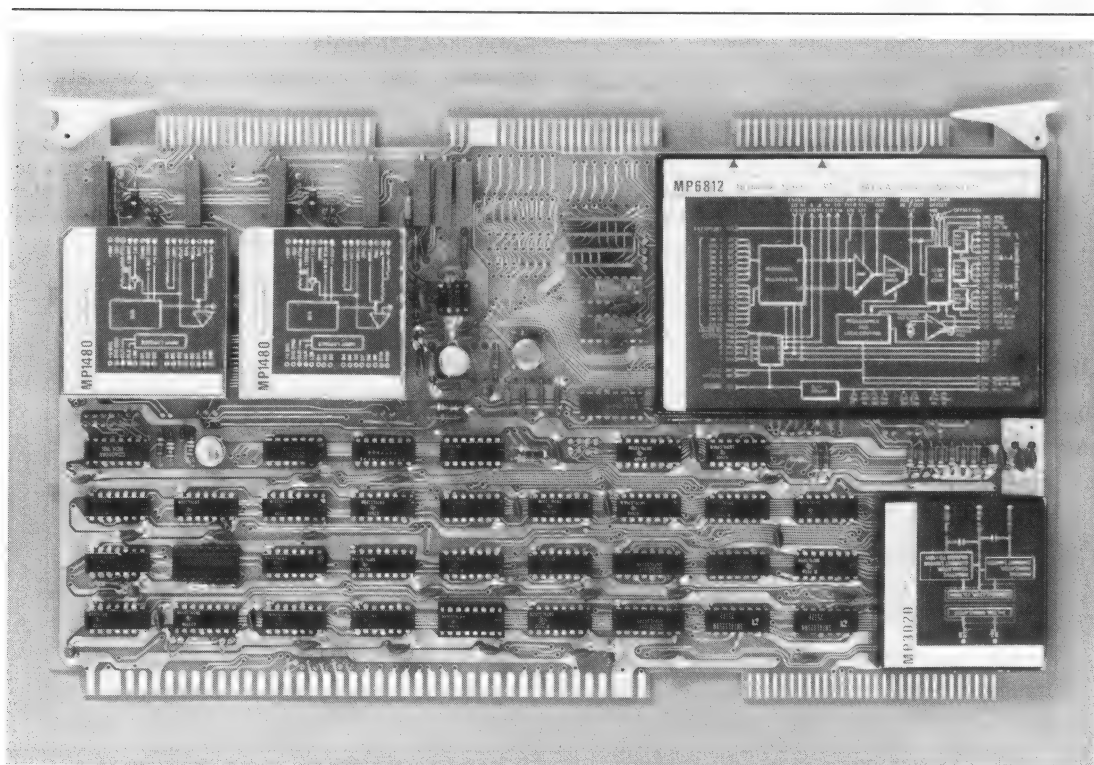
Two 12-bit D/A converter output channels

Memory mapped I/O

Single +5V supply

EXPANSION
BOARDS

The iSBC 732 is a complete single board analog input/output subsystem which allows easy interfacing of high level analog input and output signals to Intel's complete line of iSBC 80 series single board computers. The iSBC 732 performs the basic functions of data acquisition of analog inputs and controlled analog output signals under microprocessor control.



FUNCTIONAL DESCRIPTION

The iSBC 732 is electrically and mechanically compatible with the iSBC 80 series single board computers. Programming compatibility is also maintained with the iSBC 711 Analog Input Board and the iSBC 724 Analog Output Card. A block diagram of the iSBC 732 Combination Analog I/O Board is shown in Figure 1.

Input Capacity

iSBC 732 contains an 8 differential or 16 single ended analog input multiplexer. Optionally, the iSBC 732 can be expanded up to 16 differential or 32 single ended, non-isolated input channels via two plug-in multiplexers (Part No. Harris H1818A).

Fault Protection

All input channels are protected up to $\pm 28V$ via diode clamping, together with fusible current limit resistors, limiting potentially destructive overloads under fault conditions.

Current Loop Input

The differential input channels have provisions for up to 16 user supplied 250-ohm resistors to accept 4 to 20 mA current loop inputs.

Programmable Gain Amplifier

The programmable gain amplifier allows gains of 1, 2, 4, and 8, to be specified under program control.

12-Bit A/D Converter

The A/D converter is a 12-bit, 34 μs successive approximation device with sample and hold amplifier which can be jumper selected for 0 to +5V, 0 to +10V, $\pm 5V$ and $\pm 10V$ input ranges. A/D conversion can be initiated by external trigger, pacer clock, or programmed I/O. Interrupt on conversion or end of scan is a standard feature. The external trigger is useful when the A/D conversion is to be synchronized to some external event. The internal pacer clock (10 ranges jumper selectable from 976 μs to 1 sec) allows precise, evenly spaced A/D conversions where signal reconstruction is required.

D/A Converter

The dual 12-bit non-isolated D/A converter can be configured for voltage or current loop output. Each D/A converter voltage output can be jumper selected for 0 to +5V, 0 to +10V, $\pm 5V$, $\pm 10V$, or optionally 0 to 20 mA current loop output. Short circuit protection for voltage outputs is a standard feature and user supplied compliance voltage of up to 30V make the current loop output suitable for many control applications.

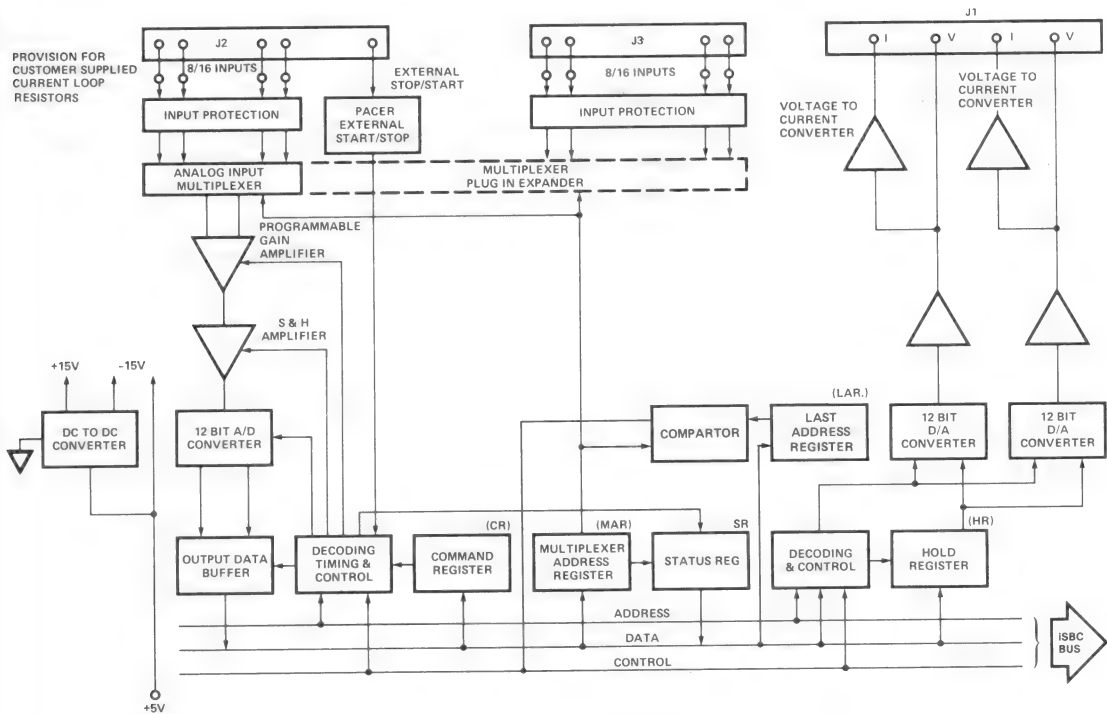


Figure 1. iSBC 732 Analog Combination I/O Board Block Diagram

OPERATIONAL DESCRIPTION

Analog Input

The ISBC 732 has three modes of operation for acquisition of analog inputs. These are:

1. Repetitive single channel input
2. Sequential input scan
3. Random channel input

Repetitive Single Channel Input — The channel is selected by a write to the multiplexer address register (MAR). The initiation of the first conversion is started by a write command to the command register (CR). Setting the appropriate bits in the command register allow stop/start, pacing, external trigger. Subsequent conversions are initiated by a read command of the A/D register (ADCR).

Sequential Input Scan — This mode is initiated in the same manner as the repetitive single channel, except bit 1 of the command register (CR) is set to a "1" on the write command.

Random Input Scan — This mode is initiated in the same manner as repetitive single channel input. Subsequent channels are selected by a write command to the multiplexer address register (MAR) before a read command of the current converted value from the ADCR register.

Analog Output

Data transfer to a D/A converter is accomplished by a write command of the least significant 4 bits to the holding register. When the upper byte is transferred, the 12 bits of data are immediately loaded to the specific D/A channel.

Addressing

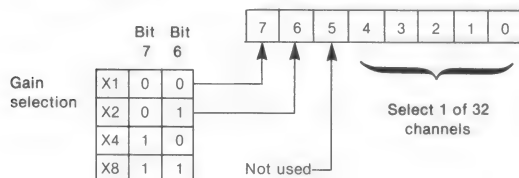
The ISBC 732 utilizes a memory mapping technique which simplifies programming in transferring 12-bit data. Since the ISBC 732 interfaces as memory, any of the 8080's memory reference instructions can be used. The A/D and independent D/A converters are addressed as memory: base plus specific address. The base address is set at F700H which is jumper selectable. Table 1 shows addressing.

Address	Command	Function
Base + 0	Write	Write to command register
Base + 0	Read	Read status register
Base + 1	Write	Write to multiplexer address register
Base + 1	Read	Read multiplexer address register
Base + 2	Write	Write to last channel register
Base + 3	Write	Clear interrupts
Base + 4	Read	Read LS byte of A/D data
Base + 5	Read	Read MS byte of A/D data
Base + 8	Write	Write to DAC holding register (low byte)
Base + 9	Write	Write to DAC 0 (high byte)
Base + A	Write	Write to DAC holding register (low byte)
Base + B	Write	Write to DAC 1 (high byte)

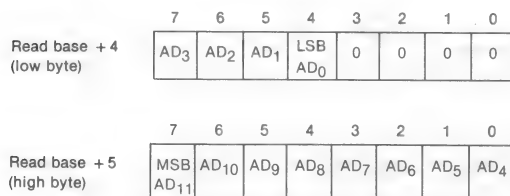
Table 1. Address Commands and Functions

SPECIFICATIONS

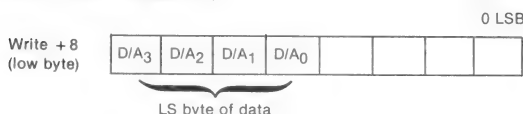
Multiplexer Address Register (MAR) Write



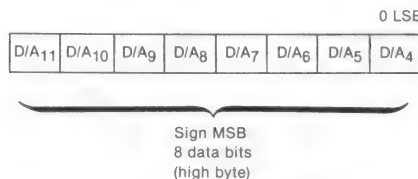
A/D Converter Register (ADCR)



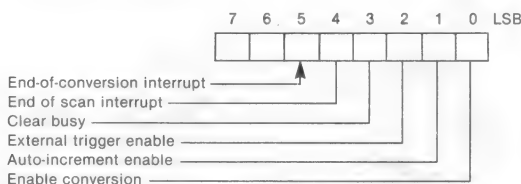
D/A Hold Register



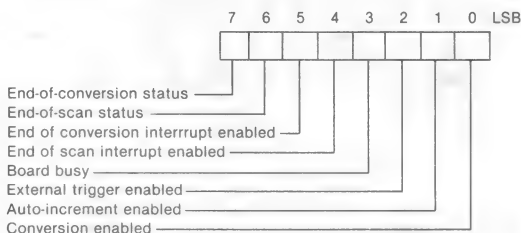
Write + 9 (high byte)

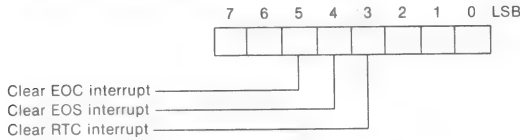
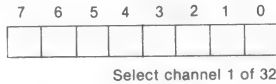


Command Register (CR) (Write Base + 0)



Status Register (Read Base + 0)



Clear Interrupt (Write Base + 3)**Last Address Register (LAR) (Write Base + 2)****Analog Input**

Number of Input Channels — 8 differential or 16 single ended (jumper selectable); expandable from 8/16 to 16/32 using two plug-in multiplexers (Part No. Harris H1818A).

Resolution — 12-bit bipolar or unipolar
Sample and Hold Aperture Time — <20 ns
Sample and Hold Uncertainty — 5 ns
Multiplexer Input Voltage Ranges

Gain X	A/D Input Range			
	+5V	+10V	±5V	±10V
1	+5V	+10V	±5V	±10V
2	+2.5V	+5V	±2.5V	±5V
4	1.25V	+2.5V	±1.25V	±2.5V
8	0.625V	+1.25V	±0.625V	±1.25V

Jumper
selectable

Software
programmable

Input Impedance

Power Off: 680 ohms
 Power On: >100M ohms

Input Current Range — 0 to 20 mA using 250-ohm user installed resistors

Source Impedance

Balanced: <5000 ohms
 Unbalanced: <1000 ohms

Overall Accuracy @ 25°C

0.05% FSR ± ½ LSB (gain × 1)
 0.07% FSR ± ½ LSB (gain × 2, × 4, × 8)
 (Includes 3 sigma noise, linearity, offset gain, and dynamic response errors)

Temperature Coefficient

0.0025% FSR/°C (gain × 1)
 0.0030% FSR/°C (gain × 2, × 4, × 8)

A/D Conversion Speed — 28 kHz

Throughput

Sample Rate (Single Channel) — 17 kHz
Channel to Channel Rate — 16 kHz
Common Mode Rejection (CMR) — 60 dB differential input

Common Mode Voltage (CMV) — ± 10.24V (signal and common mode)

Input Over-Voltage Protection — ± 28V DC, peak AC continuous

External Trigger — TTL compatible, 1.5 μs (min) better than 50 ns risetime

Pacer Clock

Crystal controlled accuracy 0.05%

Divider gives range of $\frac{1000}{2^n}$ ms

n = 0 through 10

Analog Output

Number of Channels — 2 Non-isolated
Resolution — 12 bits bipolar or unipolar (switch selectable)

Voltage Output Characteristics

Voltage Output Ranges — 0 to +5V, 0 to +10V, ±5V, ±10V (jumper selectable)

Output Current — ± 5 mA @ ± 10V

Output Impedance — 0.2 ohm

Slew Rate — 10V/μs with no external capacitance

Accuracy @ 25°C — 0.05% FSR (includes linearity and noise)

Temperature Coefficient — 0.005/°C

Current Loop Characteristics

Current Output — 0 to 20 mA

Load Resistance — 0 to 500 ohms

Compliance Voltage — Up to 30V DC (provided by user)

Accuracy @ 25°C — 0.075% FSR (includes linearity and noise)

Temperature Coefficient — 0.005/°C

Connectors

Interface	Pins (qty)	Centers		Mating Connectors
		in.	cm	
P1 iSBC Bus	86	0.156	.396	CDCVPB01E43A00A1
P2 ± 15V Auxiliary power	60	0.1	.254	
J1 2 Channels of analog output	50	0.1	.254	
J2 1st 8/16 input channels	50	0.1	.254	
J3 Expander 8/16 input channels	50	0.1	.254	3M3415-000 or TIH312125

Compatible Boards and Systems

iSBC 80/05
 iSBC 80/10
 iSBC 80/20
 System 80/10
 System 80/20-4

Physical Characteristics

Width — 12.00 in. (30.48 cm)
 Height — 6.75 in. (17.15 cm)
 Depth — 0.5 in. (1.27 cm)
 Weight — 1 lb 4 oz (568 gm)

Electrical Characteristics

Power Supply — +5V \pm 5%, 2.3A max

Environmental Characteristics

	Reference Operating Conditions	Operative Limits	Transportation and Storage Limits
Temperature	25 \pm 0.2°C	0 to 55°C	- 25 to 85°C
Relative humidity		0 to 95% not to exceed upper limit 40°C dewpoint	0 to 95%
DC supply	+ 5V \pm 5%	+ 5V \pm 5%	N/A

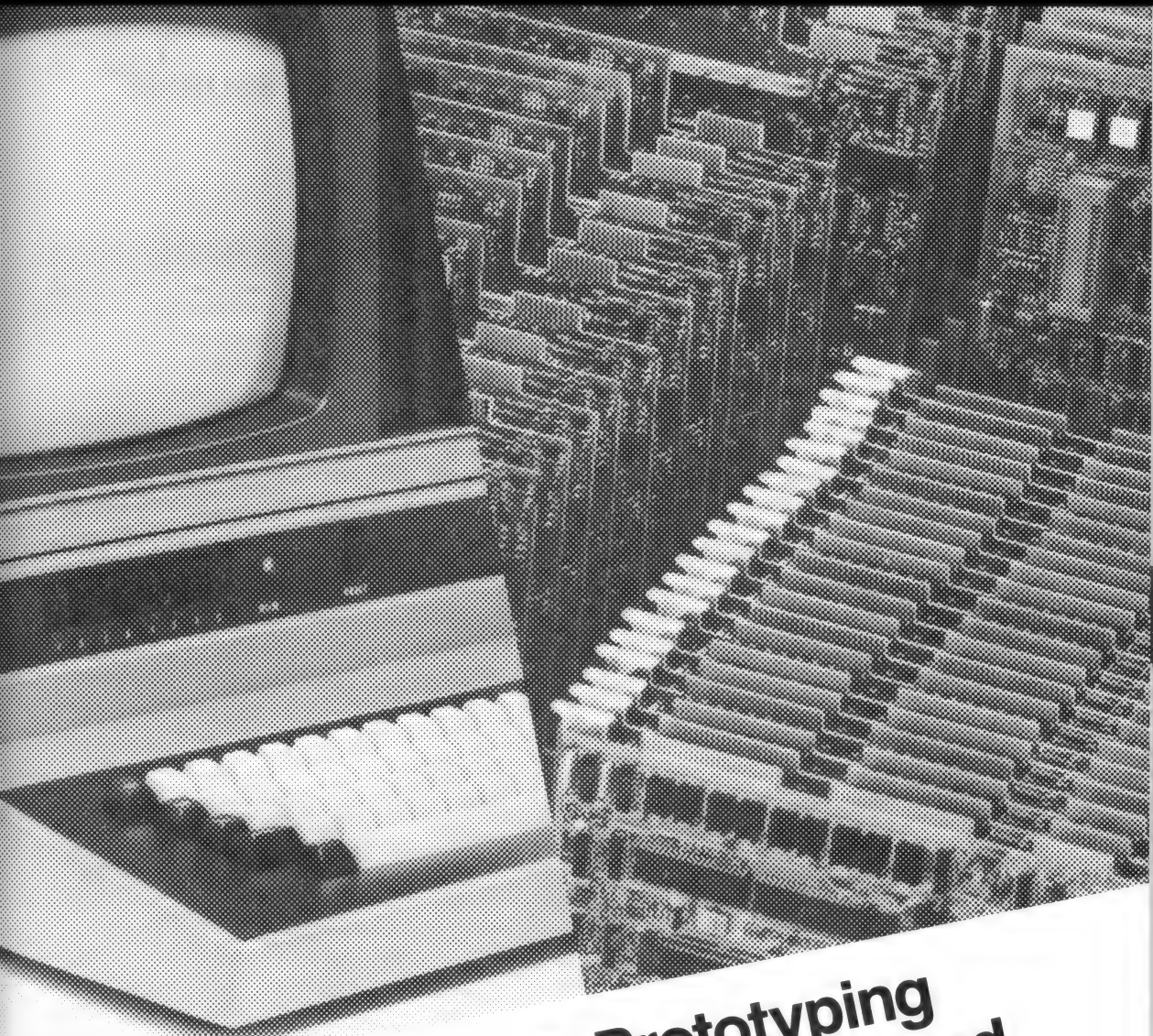
Reference Manuals

9800487 — iSBC 732 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

EXPANSION
BOARDS**ORDERING INFORMATION****Part Number Description**

SBC 732 Analog Combination I/O Board



6 Prototyping Packages and Accessories

PROTOTYPING PACKAGES AND ACCESSORIES

INTRODUCTION

The complete line of iSBC 80 prototyping packages and accessories described in this section provide support for Intel's single board computers and packaged systems. These prototyping packages contain all the hardware, software, and documentation necessary to evaluate the iSBC 80 single board computers, principally the iSBC 80/20, iSBC 80/10A, and iSBC 80/05 models. This section also contains complete details on the iSBC 80 modular backplane/cardcages and power supplies, and the iSBC 530 teletypewriter adapter.

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iSBC 80P20 Prototype Package	6-3
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iSBC 80P20 PROTOTYPE PACKAGE

iSBC 80/20 Single Board Computer

iSBC 604 cardcage/backplane with compatible power supply cables

Comprehensive system monitor residing on two Intel 8708 EPROMs

RS232C cable to interface the iSBC 80/20 to RS232C compatible devices

iSBC 530 teletypewriter adapter and TTY cable to interface the iSBC 80/20 to teletypewriters

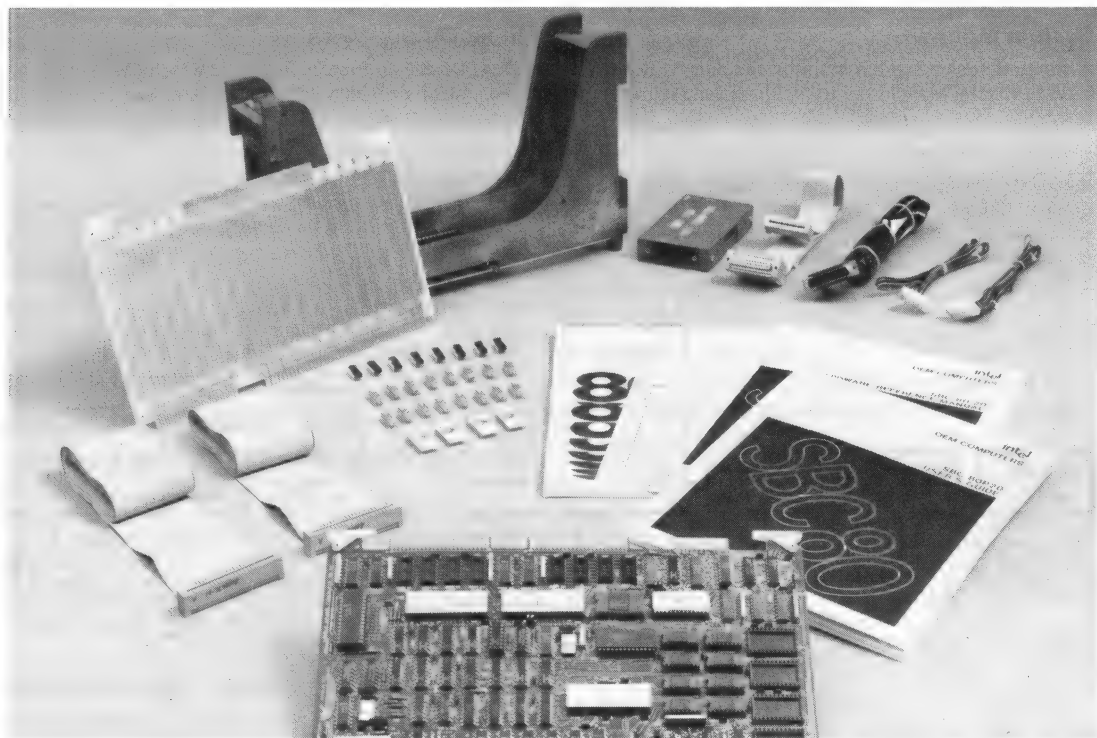
Two 50-pin unterminated flat cables with connectors to mate with iSBC 80/20 parallel I/O PC edge connectors

Full complement of EPROMs, I/O line drivers, and I/O line terminators

iSBC 905 universal prototype board for interfacing custom hardware to the iSBC 80/20

The iSBC 80P20 Prototype Package contains all the hardware, software, and documentation necessary to evaluate Intel's iSBC 80/20 single board computers for OEM applications.

PROTOTYPING
PACKAGES



FUNCTIONAL DESCRIPTION

80/20 Single Board Computer

The heart of the iSBC 80P20 Prototype Package is the iSBC 80/20 Single Board Computer, a complete computer on a single 6.75 by 12-inch printed circuit board. The iSBC 80/20 includes an 8080A CPU, 2K bytes of RAM memory, sockets for 4K bytes of EPROM memory, full multi-master bus arbitration logic allowing up to 16 CPU or controller masters to share the iSBC 80 system bus, full programmable multi-mode eight-level vectored interrupt, two programmable interval timers used either as real-time clocks or for controlled I/O timing, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, and a programmable synchronous/asynchronous communications interface with RS232C compatibility. Baud rates for the communications interface are software programmable. Systems software is used to select the appropriate communications frequency. Bus drivers are also included for memory and I/O expansion. The iSBC 80/20 block diagram is shown in Figure 1.

Cardcage/Backplane Housing

An iSBC 604 Modular Cardcage/Backplane is included to house the iSBC 80/20 and provide an easily accessible bus interface. The iSBC 604 houses the iSBC 80/20 and up to three expansion boards. All iSBC 80 bus signals are present on all four mating connectors. Also included are two power supply cables, which mate with the power supply connectors on the backplane, to carry $\pm 5V$ DC and $\pm 12V$ DC output.

System Monitor

A comprehensive system monitor, residing in two Intel 8708 EPROMs, is included to facilitate loading, execut-

ing, and debugging iSBC 80/20-based programs. Monitor commands include the ability to read and write hexadecimal paper tapes; execute pre-defined program segments; execute single program instructions; break program execution or any of seven system conditions; display, move, and alter memory contents; display and alter CPU register contents; and read and write memory contents from or to paper tape. Monitor commands and resulting information may be initiated and displayed using a teletypewriter or CRT terminal. Two cables and an iSBC 530 Teletypewriter Adapter are provided for this purpose. The first interconnects the serial PC edge connector on the iSBC 80/20 to any RS232C compatible device. For teletypewriter interfaces, the iSBC 530 Teletypewriter Adapter converts RS232C signals from the RS232C cable to a 20 mA current loop interface. The TTY cable then mates these signals directly to a teletypewriter. Any of eight standard baud rates may be used with the monitor to automatically determine the baud rate of terminal used.

Cable Interface

Two 50-pin unterminated flat cables are included to facilitate interfacing the 48 parallel I/O lines on the iSBC 80/20 to user designated I/O devices. The 48 programmable I/O signal lines and corresponding 48 ground lines on the iSBC 80/20 are brought out to two 50-pin PC edge connectors where they mate with the two flat cables. The cables are left unterminated at the user end to allow the user to provide the appropriate mating connector for any application.

Input/Output Lines

The iSBC 80P20 Prototype Package includes a full complement of EPROMs, I/O line drivers, and I/O line ter-

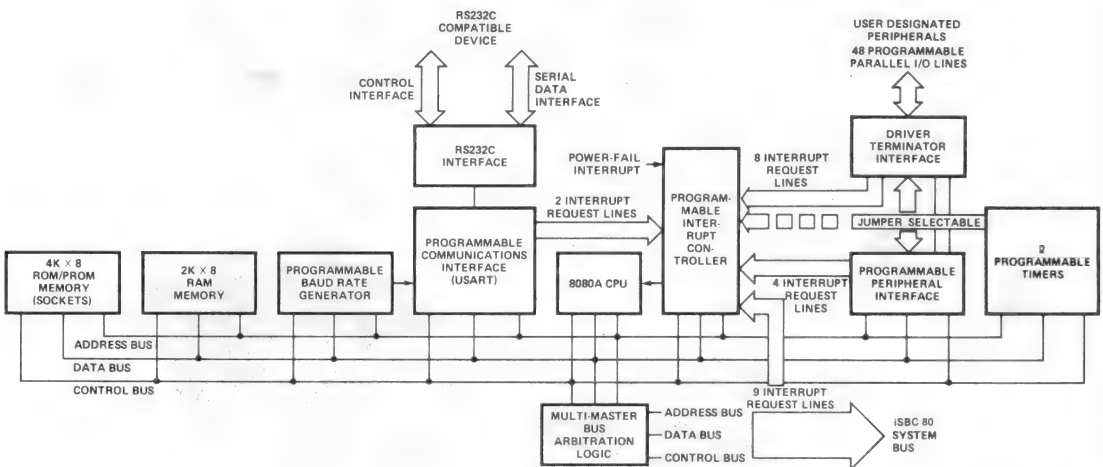


Figure 1. iSBC 80/20 Single Board Computer Block Diagram

minators. Four Intel 8708 EPROMs (1K bytes each) are included. Two EPROMs contain the system monitor and two are unprogrammed. Eight 7437 48 mA TTL quad I/O line drivers, eight Intel iSBC 901 220 Ω /330 Ω line terminators, and eight iSBC 902 1k Ω line terminators are included.

Prototype Board

An iSBC 905 Universal Prototype Board is provided to facilitate the construction of iSBC 80/20 customized I/O and/or memory hardware. The iSBC 905 plugs directly into the iSBC 604 cardcage/backplane and can house up

to 95 16-pin wire-wrap sockets or an equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets.

Support Documentation

The iSBC 80P20 Prototype Package contains all the in-depth documentation needed to program and interface iSBC 80/20 single board computers. An 8080 assembly language manual, PL/M programming manual, iSBC 80/20 hardware reference manual, and iSBC 80P20 user's guide are all included to provide clear and concise information relevant to the use of the iSBC 80/20 in OEM equipment.

SPECIFICATIONS

System Monitor

Addresses —

0000-069C_H (ROM)

3F80-3FFF_H (RAM)

Commands

- D Display memory
- G Execute program
- I Insert instruction or data into memory
- M Move memory
- N Execute next instruction (i.e., single step)
- R Read hexadecimal file
- S Substitute memory
- W Write hexadecimal file
- X Examine and modify CPU registers

Drivers

- Console input
- Console output
- Reader input
- Punch output

Breakpoint — Program breaking (BREAK) may occur upon any of up to seven system conditions. Breaks are implemented via the iSBC 80/20 programmable interrupt controller. Upon a break command, the break level, all CPU registers, and the next instruction (OP CODE) are displayed at the console.

Baud Rates — Baud rate search capability automatically sets serial baud rate to that of system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, 4800, and 9600.

Equipment Supplied

Single Board Computer — One iSBC 80/20 Single Board Computer

Read Only Memory — Two Intel 8708 EPROMs containing the system monitor; two unprogrammed Intel 8708 EPROMs

Cardcage/Backplane — One iSBC 604 Modular Cardcage/Backplane with capacity for four iSBC 80 boards

Interface Adapter — One iSBC 530 Teletypewriter Adapter for converting RS232C levels to 20 mA current loop interface

Cables

Two Power Supply Cables (2 ft long): both required for $\pm 5V$ DC and $\pm 12V$ DC; both to mate with iSBC 604

Two 50-wire parallel I/O Flat Cables (5 ft long): both to mate with iSBC 80/20 50-pin parallel I/O PC edge connectors, unterminated at user end

One RS232C Cable (2 ft long): flat cable with 26-pin iSBC 80/20 connector on one end and standard 25-pin RS232C connector on other end

One TTY Cable (5 ft long): interconnects iSBC 530 Teletypewriter Adapter with teletypewriter; 25-pin RS232C mating connector on one end; seven spade lugs on the other end

I/O Line Drivers and Terminators

- Eight 7437 48 mA totem-pole line drivers
- Eight iSBC 901 220 Ω /330 Ω terminators
- Eight iSBC 902 1 k Ω terminators

Universal Prototype Board — One iSBC 905 Universal Prototype Board with capacity for 95 16-pin wire wrap sockets or equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets; compatible with iSBC 604 cardcage/backplane

Reference Manuals

9800338 — iSBC 80P20 User's Guide (SUPPLIED)

9800301 — 8080/8085 Assembly Reference Programming Manual (SUPPLIED)

9800317 — iSBC 80/20 and iSBC 80/20-4 Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

PROTOTYPING
PACKAGES

ORDERING INFORMATION

Part Number Description

SBC 80P20 Prototype package

iSBC 80P10 PROTOTYPE PACKAGE

iSBC 80/10A Single Board Computer

iSBC 604 cardcage/backplane with compatible power supply cables

Comprehensive system monitor residing on two Intel 8708 EPROMs

RS232C and TTY cables to interface the iSBC 80/10A to any RS232C compatible device or teletype

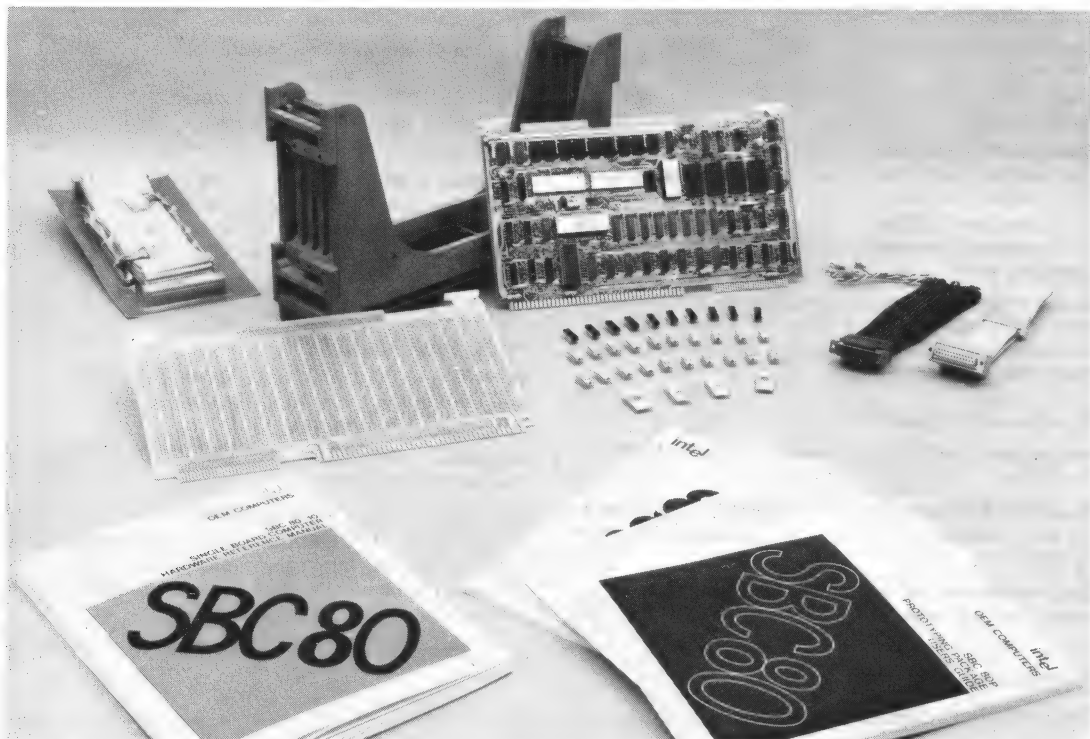
Two 50-pin unterminated flat cables with connectors to mate with iSBC 80/10A parallel I/O PC edge connectors

Full complement of EPROMs, I/O line drivers, and I/O terminators

iSBC 905 universal prototype board for interfacing custom hardware to the iSBC 80/10A

PROTOTYPING
PACKAGES

The iSBC 80P10 Prototype Package contains all the hardware, software, and documentation necessary to evaluate Intel's iSBC 80/10A single board computers for OEM applications.



FUNCTIONAL DESCRIPTION

80/10A Single Board Computer

The heart of the iSBC 80P10 Prototype Package is the iSBC 80/10A Single Board Computer, a complete computer on a single 6.75 by 12-inch printed circuit board. The iSBC 80/10A includes an 8080A CPU, 1K bytes of RAM memory, sockets for 8K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous communications interface with RS232C and teletype compatibility, a multi-source single level interrupt network, and bus drivers for memory and I/O expansion. The iSBC 80/10A block diagram is shown in Figure 1.

Cardcage/Backplane Housing

An iSBC 604 Modular Cardcage/Backplane is included to house the iSBC 80/10A and provide an easily accessible bus interface. The iSBC 604 houses the iSBC 80/10A and up to three expansion boards. All iSBC 80 bus signals are present on all four mating connectors. Also included are two power supply cables, which mate with the power supply connectors on the backplane, to carry $\pm 5V$ DC and $\pm 12V$ DC output.

System Monitor

A comprehensive system monitor, residing in two Intel 8708 EPROMs, is included to facilitate loading, executing, and debugging of iSBC 80/10A-based programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, and display and alter CPU register contents. Monitor commands and resulting information may be initiated and displayed using a teletype or CRT terminal. Two cables

are provided for this purpose. The first interconnects the serial PC edge connector on the iSBC 80/10A to any RS232C compatible device. The second connects the RS232C cable to a teletype. Wire-wrap jumpers on the iSBC 80/10A select either teletypewriter or RS232C operation and a jumper selectable baud rate generator on the iSBC 80/10A is used to select the appropriate communications frequency.

Cable Interface

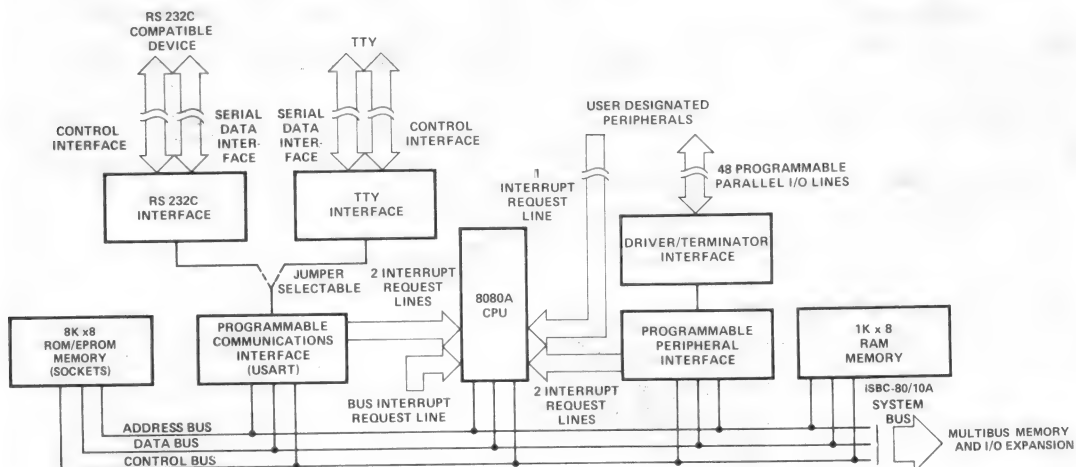
Two 50-pin unterminated flat cables are included to facilitate interfacing the 48 parallel I/O lines on the iSBC 80/10A to user designated I/O devices. The 48 programmable I/O signal lines and corresponding 48 ground lines on the iSBC 80/10A are brought out to two 50-pin PC edge connectors where they mate with the two flat cables. The cables are left unterminated to allow the user to provide the appropriate mating connector for any application.

Input/Output Lines

The iSBC 80P10 prototype package includes a full complement of EPROMs, I/O line drivers, and I/O line terminators. Four Intel 8708 EPROMs (1K bytes each) are included. Two EPROMs contain the system monitor and two are unprogrammed. Ten 7437 48-mA TTL quad I/O line drivers, ten Intel iSBC 901 220 Ω /330 Ω line terminators, and ten iSBC 902 1k Ω line terminators are included.

Prototype Board

An iSBC 905 Universal Prototype Board is provided to facilitate the construction of iSBC 80/10A customized I/O and/or memory hardware. The iSBC 905 plugs directly into the iSBC 604 Cardcage/Backplane and can house up to 95 16-pin wire wrap sockets or an equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets.



Note

1. Interrupts originating from the programmable communications interface and programmable peripheral interface are jumper selectable.

Figure 1. iSBC 80/10A Single Board Computer Block Diagram

Support Documentation

The iSBC 80P10 Prototype Package contains all the in-depth documentation needed to program and interface iSBC 80/10A single board computers. An 8080 assembly

language manual, a PL/M Programming Manual, an iSBC 80/10A hardware reference manual, and an iSBC 80P10 user's guide are all included to provide clear and concise information relevant to the use of the iSBC 80/10A in OEM equipment.

SPECIFICATIONS

System Monitor

Addresses

0000-0561_H (ROM)

3C00_H-3C3F_H (RAM)

Commands

- D Display memory
- G Program execute
- I Insert instructions into memory
- M Move memory
- R Read hexadecimal file
- S Substitute memory
- W Write hexadecimal file
- X Examine and modify CPU registers

Drivers

- Console input
- Console output
- Reader input
- Punch output

Breakpoints — A hardware breakpoint capability may be implemented by an interrupt service routine beginning at RAM location 3C3D_H. Typically, a 2-byte call is used. Interrupt generation at the breakpoint may be accomplished by user hardware or by insertion of single byte calls at instruction boundaries.

Equipment Supplied

Single Board Computer — One iSBC 80/10A Single Board Computer

Read Only Memory — Two Intel 8708 EPROMs containing the system monitor; two unprogrammed Intel 8708 EPROMs

Cardcage/Backplane — One iSBC 604 Modular Cardcage/Backplane with capacity for four iSBC boards

Cables

Two Power Supply Cables (2 ft long): both required for $\pm 5V$ DC and $\pm 12V$ DC; both to mate with iSBC 604

Two 50-wire parallel I/O Flat Cables (5 ft long): both to mate with iSBC 80/10A 50-pin parallel I/O PC edge connectors

One RS232C Cable (2 ft long): flat cable with 26-pin iSBC 80/10A connector on one end and standard 25-pin RS232C connector on other end

One TTY Cable (5 ft long): interconnects RS232C cable with teletype; 25-pin RS232C mating connector on one side; seven spade lugs on other end

I/O Line Drivers and Terminators

Ten 7437 48 mA open collector line drivers

Ten iSBC 901 220 Ω /330 Ω terminators

Ten iSBC 902 1 k Ω terminators

Universal Prototype Board — One iSBC 905 Universal Prototype Board with capacity for 95 16-pin wire-wrap sockets or equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets; compatible with iSBC 604 cardcage/backplane

Reference Manuals

9800301 — 8080/8085 Assembly Language Manual (SUPPLIED)

9800268 — PL/M Programming Manual (SUPPLIED)

9800230 — iSBC 80/10A Hardware Reference Manual (SUPPLIED)

9800223 — iSBC 80P10 User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SBC 80P10 Prototype package



iSBC 80P05 PROTOTYPE PACKAGE

iSBC 80/05 Single Board Computer

iSBC 530 teletypewriter adapter and TTY cable to interface the iSBC 80/05 to teletypewriters

iSBC 604 cardcage/backplane with compatible power supply cables

50-pin unterminated flat cable with connector to mate with iSBC 80/05 parallel I/O PC edge connector

Comprehensive system monitor residing on an Intel 2716 EPROM

Full complement of EPROMs, I/O line drivers, I/O line terminators, RS232C drivers, and RS232C receivers

RS232C cable to interface the iSBC 80/05 to RS232C compatible devices

iSBC 905 universal prototype board for interfacing custom hardware to the iSBC 80/05

The iSBC 80P05 Prototype Package contains all the necessary tools to evaluate Intel's iSBC 80/05 and iSBC 80/04 single board computers for OEM applications.

PROTOTYPING
PACKAGES



FUNCTIONAL DESCRIPTION

80/05 Single Board Computer

The heart of the ISBC 80P05 Prototype Package is the ISBC 80/05 Single Board Computer, a complete computer on a single 6.75 by 12-inch printed circuit board. The ISBC 80/05 includes an Intel 8085 CPU, 512 bytes of RAM memory, sockets for 4K bytes of EPROM memory, full multi-master MULTIBUS arbitration logic allowing up to 16 CPU or controller masters to share the MULTIBUS, four-level vectored interrupts, one programmable interval timer used as either a real-time clock or for controlled I/O timing, 22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, and serial I/O interface with TTL buffers and sockets for RS232C line drivers and receivers. The ISBC 80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085 CPU. Baud rates are controlled by software through execution of 8085 RIM and SIM instructions. Bus drivers are also included for memory and I/O expansion. The ISBC 80/05 block diagram is shown in Figure 1.

Cardcage/Backplane Housing

An ISBC 604 Modular Cardcage/Backplane is included to house the ISBC 80/05 and provide an easily accessible MULTIBUS interface. The ISBC 604 houses the ISBC 80/05 and up to three expansion boards. All MULTIBUS signals are present on all four mating connectors. Also included are two power supply cables, which mate with the power supply connectors on the backplane, to carry +5V DC and $\pm 12V$ DC output.

System Monitor

A comprehensive system monitor, residing in one Intel 2716 EPROM, is included to facilitate loading, executing, and debugging ISBC 80/05-based programs. Monitor commands include the ability to read and write hexadecimal paper tapes; execute predefined program segments; execute single program instructions; break program execution on any of four system conditions; display, move, and alter memory contents; display and alter CPU register contents; and read and write memory contents from or to paper tape. Monitor commands and resulting information may be initiated and displayed using a teletypewriter or CRT terminal. Two cables and an ISBC 530 Teletypewriter Adapter are provided for this purpose. The first interconnects the serial PC edge connector on the ISBC 80/05 to an RS232C compatible device. For teletypewriter interfaces, the ISBC 530 Teletypewriter Adapter converts RS232C signals from the RS232C cable to a 20 mA current loop interface. The TTY cable then mates these signals directly to a teletypewriter. Any of seven standard baud rates may be used with the monitor. A special "baud rate search" capability is built into the monitor to automatically determine the baud rate of the terminal used.

Cable Interface

One 50-pin unterminated flat cable is included to facilitate interfacing the 22 parallel I/O lines on the ISBC 80/05 to user designated I/O devices. The 22 programmable I/O signal lines and corresponding 22 ground lines on the ISBC 80/05 are brought out to one 50-pin PC edge connector where they mate with the flat cable. The

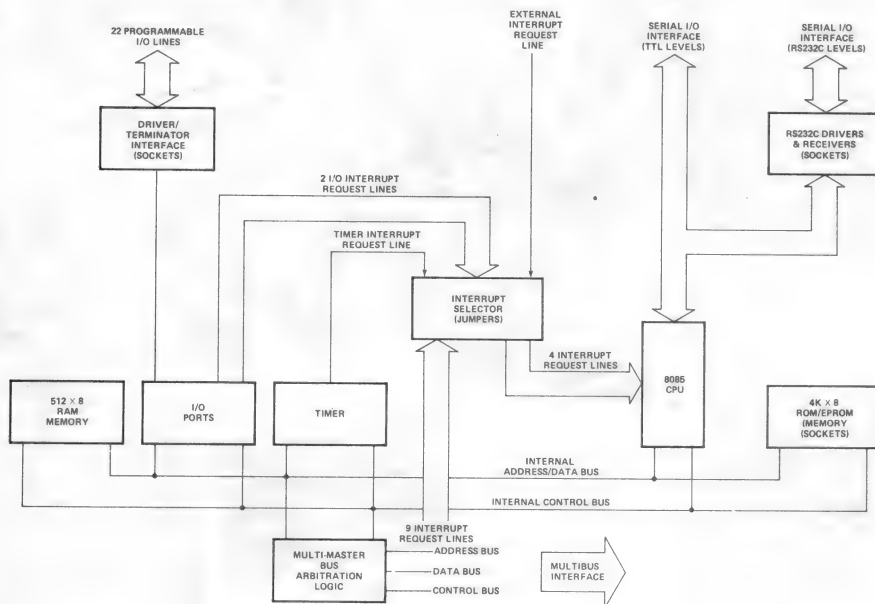


Figure 1. ISBC 80/05 Single Board Computer Block Diagram

cable is left unterminated at the user end to allow the user to provide the appropriate mating connector for any application.

Input/Output Lines

The iSBC 80P05 Prototype Package includes a full complement of EPROMs, I/O line drivers, I/O line terminators, RS232C drivers, and RS232C receivers. Two Intel 2716 EPROMs (2K bytes each) are included. One EPROM contains the system monitor and one is unprogrammed. Six 7437 48-mA TTL quad I/O line drivers, six Intel iSBC 901 220 Ω /330 Ω line terminators, and six iSBC 902 1 k Ω line terminators are included. One 1488 quad RS232C driver and one 1489 quad RS232C receiver are also included.

Prototype Board

An iSBC 905 Universal Prototype Board is provided to facilitate the construction of iSBC 80/05 customized I/O

and/or memory hardware. The iSBC 905 plugs directly into the iSBC 604 cardcage/backplane and can house up to 95 16-pin wire-wrap sockets or an equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets.

Support Documentation

The iSBC 80P05 Prototype Package contains all the in-depth documentation needed to program iSBC 80/04 and iSBC 80/05 single board computers. An 8080/85 assembly language manual, an 80/05 hardware reference manual, an iSBC 80/04 hardware reference manual, an 80P05 user's guide, iSBC 80/05 schematics, iSBC 80/04 schematics, and iSBC 530 schematics are all included to provide clear and concise information relevant to the use of the iSBC 80/05 and iSBC 80/04 in OEM equipment.

SPECIFICATIONS

System Monitor

Addresses

0000-0690_H (ROM)
3FD0-3FFF_H (RAM)

Commands

D Display memory
G Execute program
I Insert instruction or data in memory
M Move memory
N Execute next instruction (i.e., single step)
R Read hexadecimal file
S Substitute memory
W Write hexadecimal file
X Examine and modify CPU registers

Drivers

Console input
Console output
TTY reader input
TTY punch output

Breakpoints — Program breaking (BREAK) may occur upon any of up to four system conditions. Breaks are implemented via the iSBC 80/05 interrupt structure. Upon a break, the break level, all CPU registers, and the next instruction (OP CODE) are displayed at the console.

Baud Rates — Baud rate search capability automatically sets serial baud rate to that of system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, and 4800.

Equipment Supplied

Single Board Computer — One iSBC 80/05 Single Board Computer

Read Only Memory — One Intel 2716 EPROM containing the system monitor; one unprogrammed Intel 2716 EPROM

Cardcage/Backplane — One iSBC 604 Modular Cardcage/Backplane with capacity for four iSBC 80 boards

Interface Adapter — One iSBC 530 Teletypewriter Adapter for converting RS232C levels to 20 mA current loop interface

Cables

Two Power Supply Cables (2 ft long): both required for $\pm 5V$ DC and $\pm 12V$ DC; both to mate with iSBC 604

One 50-wire parallel I/O Flat Cable (5 ft long): to mate with iSBC 80/05 50-pin parallel I/O PC edge connector, unterminated at user end

One RS232C Cable (1.5 ft long): round cable with 7-pin iSBC 80/05 connector on one end and standard 25-pin RS232C connector on other end

One TTY Cable (5 ft long): interconnects iSBC 530 Teletypewriter Adapter with teletypewriter; 25-pin RS232C mating connector on one end; and seven spade lugs on the other end

I/O Line Drivers and Terminators

Six 7437 40 mA totem-pole line drivers
Six iSBC 901 220 Ω /330 Ω terminators
Six iSBC 902 1 k Ω terminators

RS232C Drivers and Terminators

One 1488 RS232C driver
One 1489 RS232C receiver

Universal Prototype Board — One iSBC 905 Universal Prototype Board with capacity for 95 16-pin wire wrap sockets or equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets; compatible with iSBC 604 cardcage/backplane

Reference Manuals

9800508 — 8080/85 Assembly Language Manual (SUPPLIED)

9800482 — iSBC 80/04 Hardware Reference Manual (SUPPLIED)

9800483 — iSBC 80/05 Hardware Reference Manual (SUPPLIED)

9800508 — iSBC 80P05 User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
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SBC 80P05	Prototype package
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PROTOTYPING
PACKAGES



iSBC 604/614 MODULAR CARDCAGE/BACKPLANE

Interconnection and housing for up to four Intel iSBC boards

Cardcage mounting holes, facilitating interconnection of two or more units

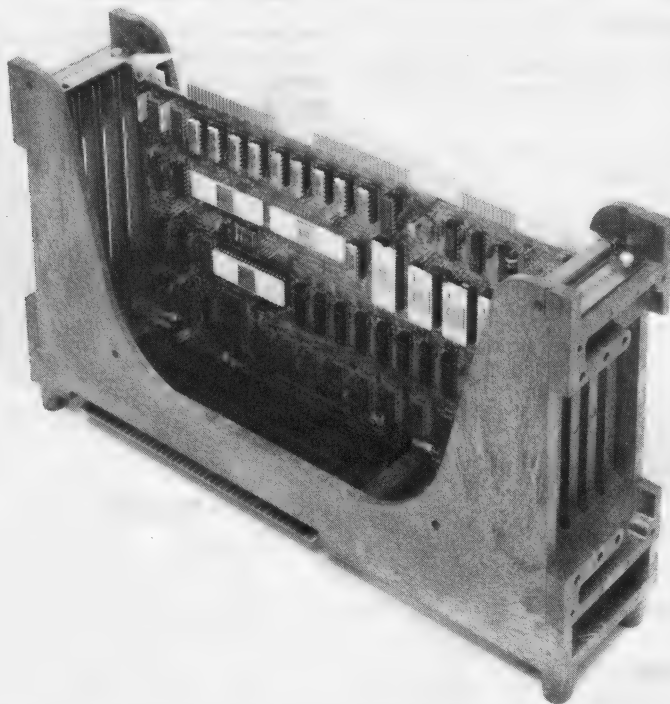
Connectors allowing interconnection of two or more backplanes

Compatibility with 3.5 inch RETMA rack mount increments

Dual backplane power supply connectors

The iSBC 604 and iSBC 614 Modular Cardcage/Backplane units provide low-cost, off-the-shelf housing for OEM products using two or more Intel single board computers. Each unit interconnects and houses up to four boards. The iSBC 604 contains a male backplane PC edge connector and bus signal termination circuits. It is suitable for applications requiring a single unit, or may be interconnected with the iSBC 614 when more than one backplane/cardcage unit is needed. The iSBC 614 contains both male and female backplane connectors, and may be interconnected with the iSBC 604 and the other iSBC 614 units. Both units are identical, with the exception of the backplane connectors and bus signal terminator features. A single unit may be packaged in a 3.5-inch RETMA rack enclosure, and two interconnected units may be packaged in a 7-inch enclosure. The units are mountable in any of three planes. The iSBC 604 contains power supply connectors.

PROTOTYPING
PACKAGES



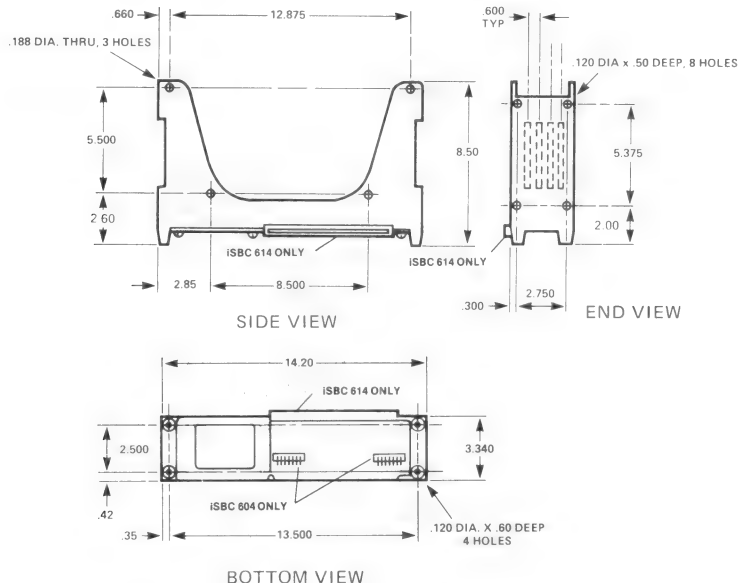


Figure 1. iSBC 604/614 Modular Backplane and Cardcage Dimensions

SPECIFICATIONS

Backplane Characteristics

Bus Lines — All iSBC 80 address, data, and command bus lines are bussed to all four connectors on the printed circuit backplane

Power Connectors — for ground, +5V, -5V, +12V, -12V, -10V power supply lines

iSBC 604 — Bus signal terminators, backplane male PC edge connector only, and power supply headers

iSBC 614 — Backplane male and female connectors

Mating Power Connectors

AMP	Connector	87159-7
	Pin	87023-1
	Polarizing key	87116-2
Molex	Connector	09-50-7071
	Pin	08-50-0106
	Polarizing key	15-04-0219

Note

1. Pins from a given vendor may only be used with connectors from the same vendor.

Physical Dimensions

Height — 8.5 in. (21.59 cm)

Width — 14.2 in. (36.07 cm)

Depth — 3.34 in. (8.48 cm)

Weight — 35 oz (992.23 gm)

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

None supplied.

ORDERING INFORMATION

Part Number Description

SBC 604/614 Modular backplane and cardcage



iSBC 630 POWER SUPPLY

Compact single chassis

Additional +26.5V supply

$\pm 5V$ and $\pm 12V$ iSBC 80 system power

Keyed to standard AC and DC connectors

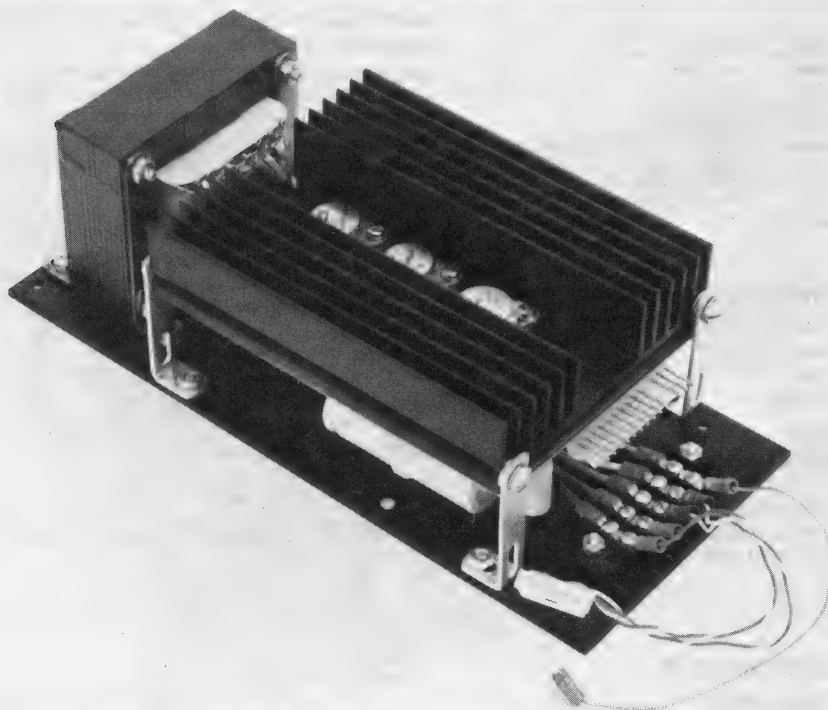
Sufficient power for one fully loaded Intel single board computer, plus residual power for user functions

115V AC and 230V AC operation

50 Hz or 60 Hz input

The iSBC 630 Power Supply provides low cost, off-the-shelf, single chassis power generation for OEM products using Intel single board computers. The iSBC 630 provides regulated DC output power at +12V, +5V, -5V, and -12V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to +55°C temperature range for one Intel single board computer fully loaded with I/O line terminators and drivers and four 8708 EPROMs, plus residual capability for additional OEM system logic functions. A +26.5V power level has also been provided for use in OEM products for relay interfaces and displays, and for those OEM products requiring in-system 8708 EPROM programming capability. Current limiting protection is provided on the +12V and +5V outputs, and over-voltage protection is incorporated on the +5V output. Access to AC input and DC output levels is provided via standard 4-pin and 14-pin keyed connectors, respectively.

PROTOTYPING
PACKAGES



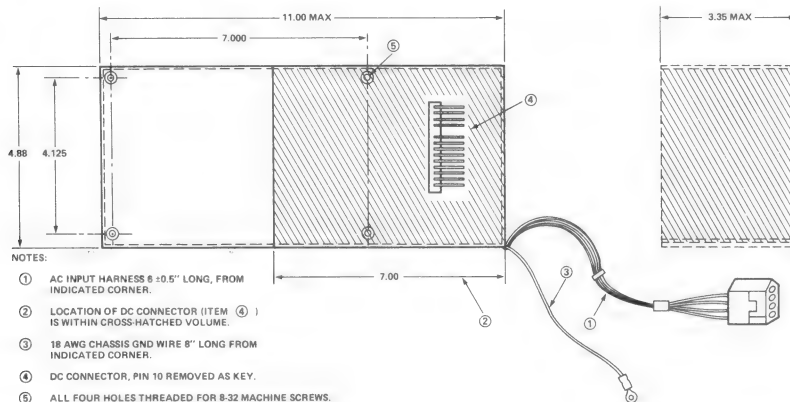


Figure 1. ISBC 630 Mounting Information

SPECIFICATIONS

Mating Connectors¹

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output

Connector	Molex	09-05-7141
	AMP	1-87159-3
Polarizing key	Molex	15-04-0219
	AMP	87116-2
Pin	Molex	08-50-0106 (18 to 22 gauge wire)
	AMP	87023-1 (18 to 22 gauge wire)

Note

1. Pins from a given vendor may only be used with connectors from the same vendor.

Physical Characteristics

Height — 3.35 in. max (8.51 cm)
Width — 4.91 in. max (12.40 cm)
Depth — 11.00 in. max (27.95 cm)
Weight — 8.0 lb (3.63 kgm)

Electrical Characteristics

Input Power

Frequency: 47 Hz to 63 Hz
 Voltage: 115V AC ± 10% and 230V AC ± 10%
 Current: 1.8A max (at 125 V AC)

Output Power

Power	Output Current (Max)	Accuracy
+ 26.5V	100 mA	± 0.5V
+ 12V	1.2A	± 5%
+ 5V	6A	± 5%
- 5V	300 mA	± 5%
- 12V	300 mA	± 5%

Over-Voltage Protection — 5V output; fixed within the range 6.08V to 6.72V

Line Regulation — (10% line voltage change) + 5V and + 12V outputs: 0.1%; - 5V, - 12V and + 26.5V outputs: 1%

Load Regulation — (half load to full load) + 5V and + 12V outputs: 0.1%; - 5V, - 12V and + 26.5V outputs: 1%

Output Ripple and Noise — 50 mV peak-to-peak on all outputs, max

Short Circuit Current — + 5V output: 7.5A max; + 12V output: 1.5A max

Environmental Characteristics

Operating Temperature — 0°C to + 55°C

Equipment Supplied

iSBC 630 Power Supply

Reference Manuals

9800297 — iSBC 630 User's Manual (includes schematic) (SUPPLIED)

ORDERING INFORMATION

Part Number Description

SBC 630 Power supply



iSBC 635 POWER SUPPLY

Compact single chassis

$\pm 5V$ and $\pm 12V$ iSBC 80 system power

Sufficient power for one fully loaded Intel single board computer plus residual power for up to three Intel iSBC expansion boards

Current limiting and overvoltage protection on all outputs

DC power cables and connectors mate directly to iSBC 604 Modular Cardcage/Backplane assembly

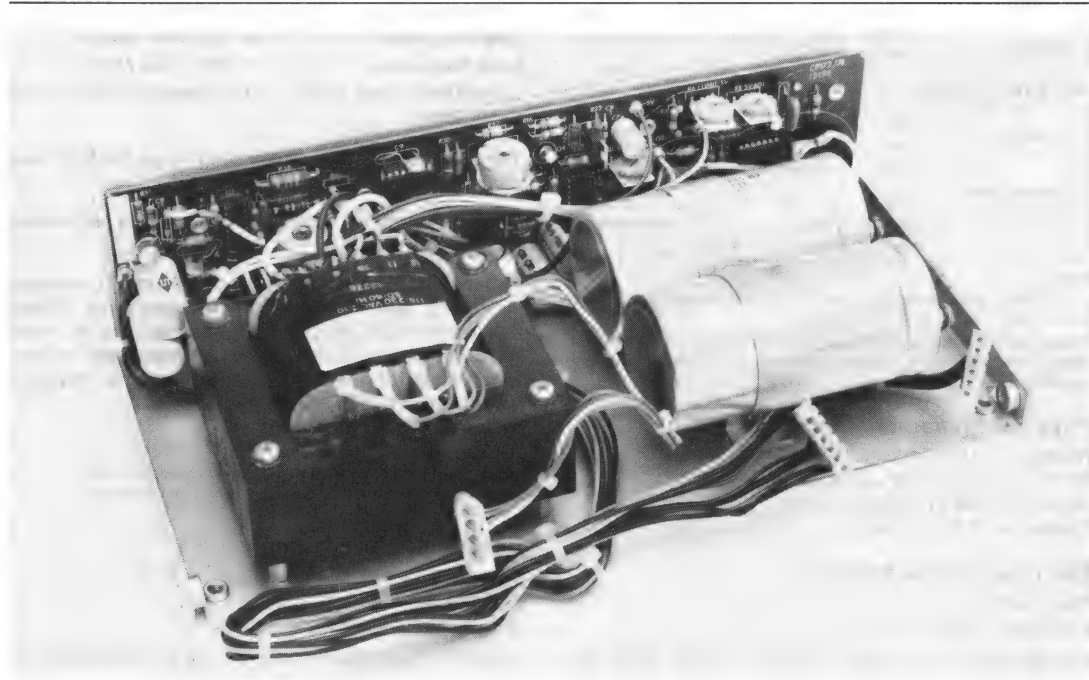
"AC low" power failure TTL logic level output provided for system power-down control

100, 115, 215, and 230V AC operation

50 Hz or 60 Hz input

The iSBC 635 Power Supply provides low cost, off-the-shelf, single chassis power generation for OEM products using Intel single board computers. The iSBC 635 provides regulated DC output power at +12V, +5V, -5V, and -12V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to +55°C temperature range for one Intel single board computer fully loaded with I/O line terminators and drivers and four 8708 EPROMs, plus residual capability for most combinations of up to three iSBC memory, I/O, or combination expansion boards. Current limiting and overvoltage protection is provided on all outputs. Access for AC input is provided via a standard 4-pin keyed connector. DC output power levels are provided on cables with keyed connectors directly compatible with the iSBC 604 Modular Backplane/Cardcage assembly. The iSBC 635 includes logic whose purpose is to sense system AC power failure and generate a TTL signal for clean system power-down control.

PROTOTYPING
PACKAGES



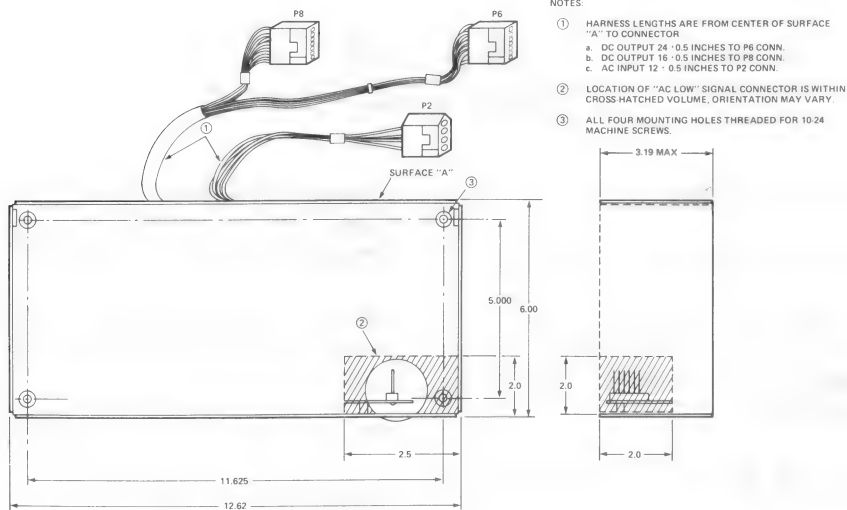


Figure 1. iSBC 635 Mounting Information

SPECIFICATIONS

Mating Connectors¹

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output²

Header	Molex	09-66-1071
	AMP	87194-6

"AC Low" Control

Connector	Molex	09-50-7071
	AMP	87159-7
Polarizing key	Molex	15-04-0219
	AMP	87116-2
Pin	Molex	08-50-0106 (18 to 22 gauge wire)
	AMP	87023-1 (18 to 22 gauge wire)

Notes

- Pins from a given vendor may only be used with connectors from the same vendor.
- iSBC 635 DC output connectors are directly compatible with power input power connectors on iSBC 604 Modular Cardcage/Backplane assembly.

Physical Characteristics

Height — 3.19 in. max (8.11 cm)
Width — 6.03 in. max (15.32 cm)
Depth — 12.65 in. max (32.12 cm)
Weight — 13 lb (5.90 kgm)

Electrical Characteristics

Input Power

Frequency: 47 Hz to 63 Hz

Voltage: 100V AC $\pm 10\%$, 115V AC $\pm 10\%$, 215V AC $\pm 10\%$, 230V AC $\pm 10\%$ via user provided wiring options

Output Power

Power	Output Current (max)	Current Limit (max)	Over-Voltage Protection
+ 12V	2.0A	2.4A	+ 14.0V to + 16.0V
+ 5V	14.0A	16.8A	+ 5.8V to + 6.6V
- 5V	0.9A	1.1A	- 5.8V to - 6.6V
- 12V	0.8A	1.0A	- 14.0V to - 16.0V

Remote Sensing — Sensing provided for +5V output

Line Regulation — $\pm 0.1\%$ for 10% line change¹

Load Regulation — $\pm 0.1\%$ for 50% load change¹

Output Ripple and Noise — 10 mV peak-to-peak max (DC to 500 kHz)¹

Transient Response — Less than 50 μ s for 50% load change¹

Output Voltage Accuracy — All outputs adjustable $\pm 5\%$ from nominal²

Power Failure Indication — An active high, TTL compatible output logic level is provided when input voltage falls below 103V AC (RMS)³ to indicate low AC input voltage conditions. All output voltages will remain within spec for one-half cycle (≈ 8.3 ms @ 60 Hz) minimum after "AC low" is asserted.

Notes

- All outputs.
- All outputs set to nominal voltage (no load) before delivery.
- 206V AC (RMS) for 230V AC (RMS) nominal input operation.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Equipment Supplied

iSBC 635 Power Supply with AC and DC cables and connectors attached as shown in Figure 1.

Reference Manuals

9800298 — iSBC 635 User's Manual (includes schematics) (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 635	Power supply

PROTOTYPING
PACKAGES



iSBC 530 TELETYPEWRITER ADAPTER

Compact, easily mounted package with standard connectors

General purpose RS232C to 20 mA current loop interface

Compatibility with iSBC 80/20 Single Board Computer

Jumper selectable RS232C data set or data terminal configuration

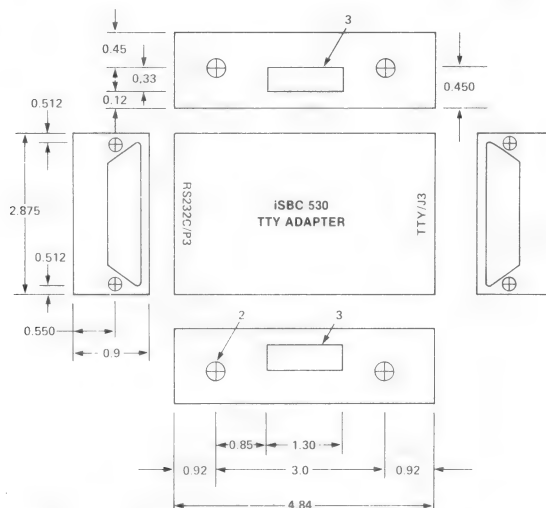
Compatibility with iSBC 80 combination boards

Interface opto-isolated for high noise immunity

The iSBC 530 Teletypewriter Adapter provides a compact and flexible means for interfacing the Intel iSBC 80/20 Single Board Computer, iSBC 80 combination memory and I/O expansion boards, and most RS232C compatible equipment to teletypewriters and other 20 mA current loop equipment. The iSBC 530 converts RS232C signal levels to an optically isolated 20 mA current loop interface. The iSBC 530 provides signal translation for transmitted data (Txd), received data (Rcd), and a teletypewriter paper tape reader relay. The RS232C interfaces are jumper selectable, and may be configured to accept signals from an RS232C data terminal or data set. Threaded holes have been incorporated in the iSBC 530 for ease in system chassis design, and multiple units may be mounted together to support multiple serial channels. The units are mountable in any of three planes. When used with the iSBC 80/20 Single Board Computer, power is provided to the iSBC 530 directly through its RS232C connector. Power may also be provided through either of two auxiliary power connectors for standard current loop interfacing. The noise immunity benefits of total intersystem power isolation may be achieved through the use of both auxiliary power connectors on the iSBC 530.

PROTOTYPING
PACKAGES





NOTES: 1. ALL DIMENSIONS IN INCHES.
2. ALL FOUR MOUNTING HOLES THREADED FOR 6-32 MACHINE SCREWS
3. CUTOUTS FOR AUXILIARY POWER CONNECTORS.

Figure 1. ISBC 530 Dimensions

SPECIFICATIONS

Interface Characteristics

RS232C Side

RS232C signal levels in/out¹

TTY Side

20 mA optically isolated current loop

Note

1. RS232C data set ready line controls 20 mA paper tape reader relay driver line.

Mating Connectors

RS232C	Cinch	DB-25S
	ITT Cannon	DB-25S
20 mA (TTY)	Cinch	DB-25P
	ITT Cannon	DB-25P
Auxiliary power	AMP	Connector 87159-7
		Pin 87023-1
		Polarizing key 87116-2
	Molex	Connector 09-50-7071
		Pin 08-50-0106
		Polarizing key 15-04-0219

Note

1. Pins from a given vendor may only be used with connectors from the same vendor.

Physical Characteristics

Width — 2.876 in. max (7.31 cm)

Height — 4.850 in. max (12.32 cm)

Depth — 0.920 in. max (2.34 cm)

Weight — 9 oz (255.4 gm)

Electrical Characteristics

Power connectors for ground, +12V and -12V, are jumper selectable. Power may be provided via 25-pin RS232C connector or via two separate auxiliary power connectors. Auxiliary connectors allow total power system isolation at ISBC 530 opto-coupler interface.

Power Requirements

$V_{DD} = +12V \pm 5\%$

$V_{AA} = -12V \pm 5\%$

$I_{DD} = 98 \text{ mA max}$

$I_{AA} = 98 \text{ mA max}$

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

None supplied.

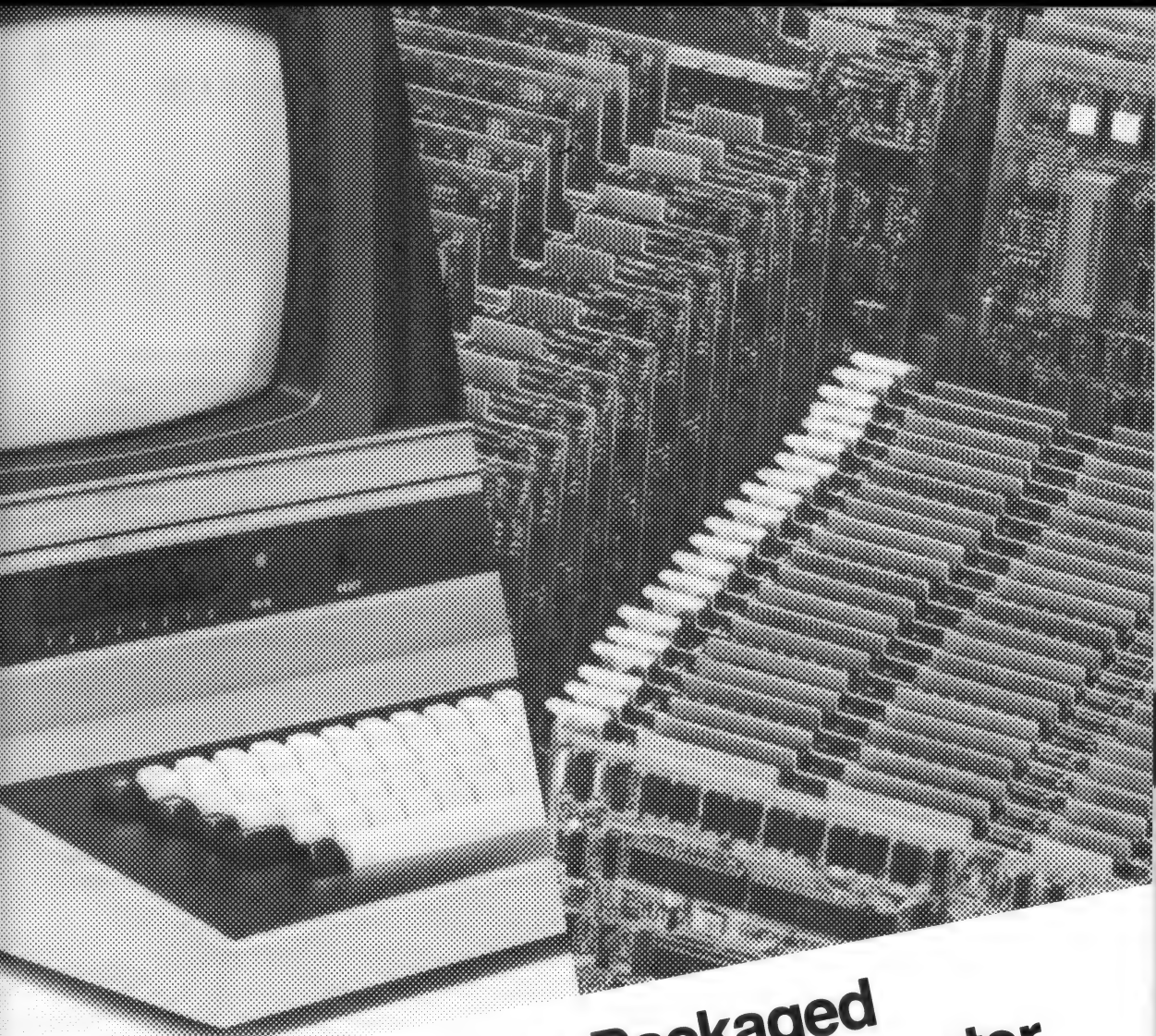
Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SBC 530 Teletypewriter adapter

PROTOTYPING
PACKAGES



7 Packaged Microcomputer Systems

PACKAGED MICROCOMPUTER SYSTEMS

INTRODUCTION

This section provides information and specifications on Intel's fully packaged OEM computers, the System 80/20-4 and the System 80/10A. These systems extend the full computer capabilities of Intel's single board computers into low cost, fully packaged, RETMA rack-mountable computers. Also included here is information on the iSBC 660 7-inch system chassis, designed specifically for use with Intel OEM computers.

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System 80/30	7-16
iSBC 660 System Chassis	7-23



SYSTEM 80/20-4

A rack mountable, packaged microcomputer for OEM applications

Processing power from the popular iSBC 80/20-4 Single Board Computer

Fully programmable I/O

- Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rate generation
- 48 lines parallel I/O standard
- Expandable with low cost digital I/O and analog I/O modules

Full MULTIBUS control logic allowing additional masters to share system bus

Two programmable 16-bit BCD or binary timers

Eight-level programmable vectored priority interrupt control

Expandable memory capacity

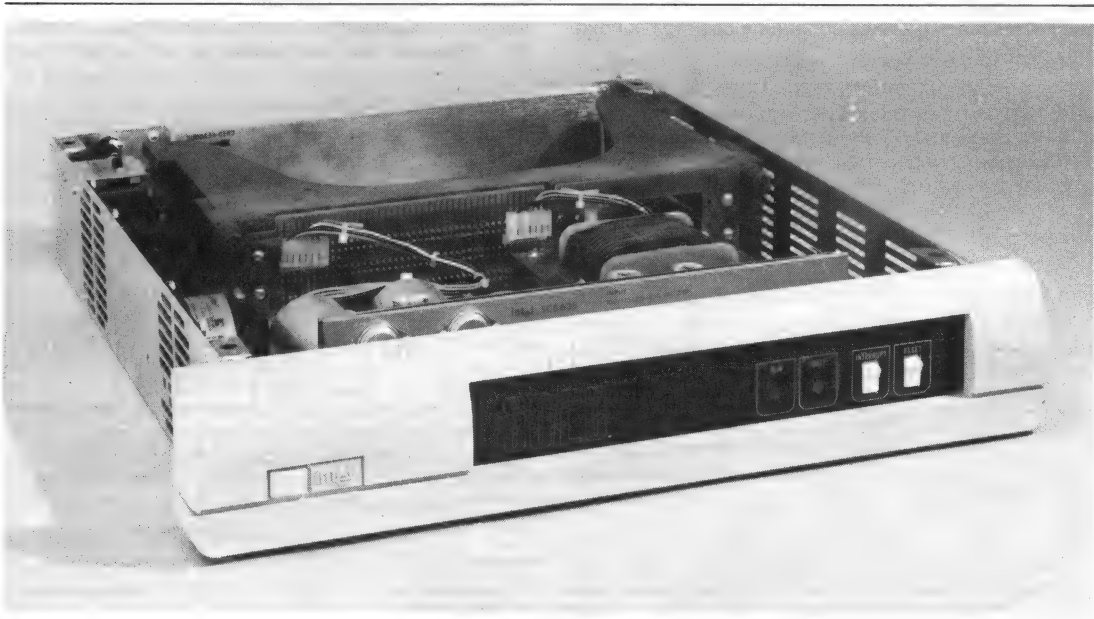
- 4K bytes RAM standard
- 8K EPROM capacity
- Expandable with low cost RAM, ROM, EPROM, and combination modules

Comprehensive system monitor for loading, executing, and debugging System 80/20-4 programs

- Display and alter memory locations
- Display and alter registers
- Single step program execution
- Read and write paper tape commands
- RS232C driver

The Intel System 80/20-4 is a fully packaged microcomputer utilizing the iSBC 80/20-4 Single Board Computer. Ideal for the OEM whose design requires low cost 19-inch RETMA compatible rack mountable packaging, the System 80/20-4 offers easy to use, fully programmable I/O and the computational power of the iSBC 80/20-4, and has both RAM and EPROM memory. The enclosed power supply is designed to support not only the single board computer, but also a full complement of expansion boards. The RETMA compatible chassis houses the computer, power supply, and fans, and has three additional slots for expansion.

PACKAGED
SYSTEMS



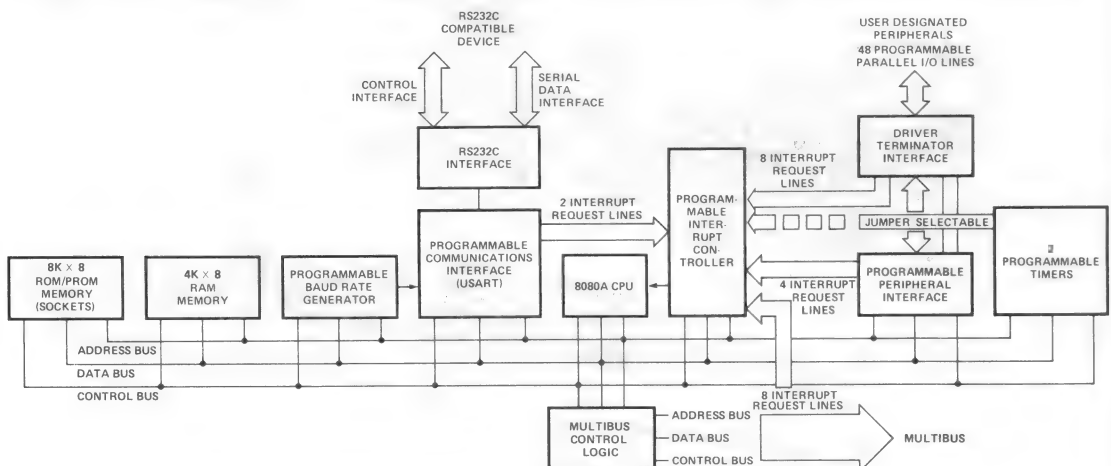
The heart of the System 80/20-4 is the iSBX 80/20-4 Single Board Computer, a complete computer on a single printed circuit board. The iSBX 80/20-4 includes an 8080A CPU, 4K bytes of static RAM memory, sockets for up to 8K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous RS232C communications interface, programmable 8-level vectored priority interrupt structure, programmable interval timers, and bus drivers for memory and I/O expansion. Read only memory may be added in 1K-byte increments using Intel 8708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs, and in 2K-byte increments using Intel 8716 EPROMs or 8316B masked ROMs. All on-board memory operations are performed at maximum processor speed. A block diagram of the System 80/20-4 functional components is shown in Figure 1.

Intel's powerful 8-bit, N-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/20-4. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

The System 80/20-4 contains 48 programmable parallel I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software may configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable, woven cable, or round cable. The user may design his own cables or order the iSBC 956 Parallel I/O Cable Set.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of the RS232C compatible interface on the board allows the system to be used directly with CRTs, RS232C compatible cassettes, and asynchronous and synchronous



7-4

Port	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X ¹
	4	X		X			X ¹
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X ²
	4	X		X			X ²

Notes
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

modems. The RS232C command lines, serial lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat cable. A 20-mil TTY compatible interface may be achieved by using the optional iSBC 530 TTY Adapter.

Multimaster Capability

The System 80/20-4 is a full computer with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the MULTIBUS), the System 80/20-4 provides full bus arbitration control logic. This control logic allows additional iSBC 80/20s, iSBC 80/05s, or other high speed controllers to share the MULTIBUS in serial (daisy chain) priority fashion, or in parallel priority fashion with the addition of an external priority network. The MULTIBUS controller provides its own clock, which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second.

Programmable Timers

The System 80/20-4 provides three fully programmable and independent BCD binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval

Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or the outputs from 8255 programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port. The systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly".

Interrupt Capability

An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level

currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage (via software) of a single byte to the interrupt mask register of the PIC.

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output goes low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square wave rate generator	Output remains high until one-half the count has been completed, and goes low for the other half of the count.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.

Table 2. Programmable Timer Functions

Interrupt Addressing — The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8080A jump instruction at each of these addresses can then provide linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation — Interrupt requests may originate from 26 sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character

is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the MULTIBUS. BUS.

Function	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority -encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Expansion Capabilities

System 80/20-4 memory may be increased by adding combinations of ISBC RAM boards and ISBC PROM boards. Input/output capacity may be increased using the ISBC digital I/O or analog I/O boards. System resources may be increased simultaneously using ISBC 80 combination and I/O and memory expansion boards. All combination boards provide 48 lines of programmable parallel I/O, one programmable serial port, and sockets for up to 8K of EPROM. A RAM increment of 4K, 8K, or 16K can be chosen with the ISBC 104, 108, or 116, respectively.

Peripherals — Mass storage capacity may be added to the System 80/20-4 with Intel's flexible diskette peripherals. The ISBC 201 Single Density Diskette Controller and ISBC 202 Double Density Diskette Controller are powerful and easy to use plug-in modules which are compatible with several manufacturers' diskette drives. For a completely tested mass storage peripheral, the ISBC 211 single drive system and the ISBC 212 dual drive system are available.

Bus Interface — A modular cardcage/backplane is installed in the chassis to house the ISBC 80/20-4 and provide an easily accessible bus interface. The cardcage also houses any additional expansion boards. All ISBC 80 bus signals are present on all mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry $\pm 5V$ and $\pm 12V$ DC.

System Monitor

A comprehensive system monitor, residing in two Intel 1K-byte ROMs, is included to facilitate loading, executing, and debugging programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display

and alter memory contents, display and alter CPU register contents, and execute single step programs. Monitor commands and resulting information may be initiated and displayed using CRT or other RS232C device.

Real-Time Software

The System 80/20-4 is totally compatible with Intel's RMX/80 Real-Time Multi-Tasking Executive. User programs (tasks) can take advantage of RMX/80 to do all necessary scheduling, intertask communication, and memory space allocation. RMX/80 also provides standard I/O support software such as the disk file handler, the Intel analog board handler, and the terminal handler.

System Development Capability

The development cycle of System 80/20-4-based products may be significantly reduced using an Intel microcomputer development system. The resident microassembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. Optional diskette operating software for the development system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-80) option

provides the capability to use the development system to develop and debug software directly on the System 80/20-4.

PL/M-80 Programming Capability

Intel's high level resident programming language, PL/M-80, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M-80 programs can be written in a much shorter time than assembly language programs.

Service Accessibility

The System 80/20-4 is designed for easy modular servability. The computer boards are accessible from the rear of the package and strain relief clamps are included to protect any I/O cabling added by the OEM. The power supply may be removed from the system to allow easy backplane servicing. An RS232C cable and connector are included as standard.

Support Documentation

The System 80/20-4 comes with all in-depth documentation needed to program and interface with the system. An 8080 assembly language manual and a hardware reference manual are included to provide clear and concise information relevant to the use of a System 80/20-4.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Time

Basic Instruction Cycle — 1.86 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-0FFF_H

On-Board RAM — 4K segments ending at any jumper selectable address on a 16K boundary (e.g., 0000_H, 4000_H, ... C000_H).

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 4K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM.

Note

ROM/EPROM may be added in 1K- or 2K-byte increments.

I/O Addressing

On-Board Programmable I/O — see Table 1

Port	8255A No. 1						8255A No. 2		USART Data	USART Control
	1	2	3	4	5	6	Control	Control		
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note

Expandable with optional I/O boards.

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		+ 16	+ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Note

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

Note

Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

Interrupts

Register Address (hex notation, I/O address space)

DA Interrupt request register
 DA In-service register
 DB Mask register
 DA Command register
 DB Block address register
 DA Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Timers

Register Address (hex notation, I/O address space)

DF Control register
 DC Timer 0
 DD Timer 1

Note

Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference	Event Rate
1.0752 MHz \pm 0.1% (0.930 μ s period, nominal)	1.1 MHz ¹

Note

1. Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Programmable one-shot	1.86 μ s	60.945 ms	3.72 μ s	1.109 hr
Rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-wave rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Software triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Hardware triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

System Clock (8080A CPU)

2.154 MHz \pm 0.1%

Physical Characteristics

Height — 3.5 in. (8.90 cm)

Width — At front panel — 19 in. (48.3 cm); behind front panel — 17 in. (43.2 cm)

Depth — 20 in. (50 cm) with all protrusions

Compatible Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat TI H312125 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the ISBC 80/04:

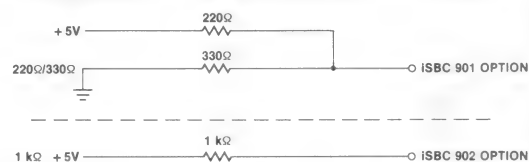
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup.



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Electrical Characteristics

Input Power

Frequency	Voltage
47-63 Hz	Standard — 115V AC \pm 10%
	Option — 230V AC \pm 10%

Output Power Available for Expansion Boards

Voltage	Supply Current	Without PROM ¹	With 4K PROM ²	With 8K PROM ³	Over Voltage Protection
+5	14A	10A	9.1A	8.8A	5.8 to 6.6V
+12	2A	1.91A	1.65A	1.91A	+14 to +16V
-5	0.9A	0.89A	0.72A	0.89A	-5.8 to -6.6V
-12	0.8A	0.78A	0.78A	0.78A	-14 to -16V

Notes

1. Does not include power required for optional PROM, I/O drivers, and I/O terminators.

2. With four 8708 EPROMs and 220 Ω /330 Ω input terminators installed for 32 I/O lines, all terminator inputs low.

3. With four 8716 EPROMs and eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.

SYSTEM 80/20-4

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800484 — iSBC 80/20-4 Hardware Reference Manual
(SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
Sys 80/20-4	System 80/20-4

PACKAGED
SYSTEMS



SYSTEM 80/10A

**A completely packaged microcomputer
for OEM applications**

**Processing power from the popular iSBC
80/10A Single Board Computer**

Multi-source interrupt

**Complete power supply with over-voltage
protection**

**Compact, 3½-inch RETMA compatible
chassis**

Three additional expansion board slots

**Software support from Intellec MDS 800
System**

Full 8080A instruction set

Fully programmable I/O

- Standard asynchronous/synchronous serial I/O port with RS232C and TTY interfaces
- 48 lines parallel I/O standard
- Expandable with low cost I/O and combination modules

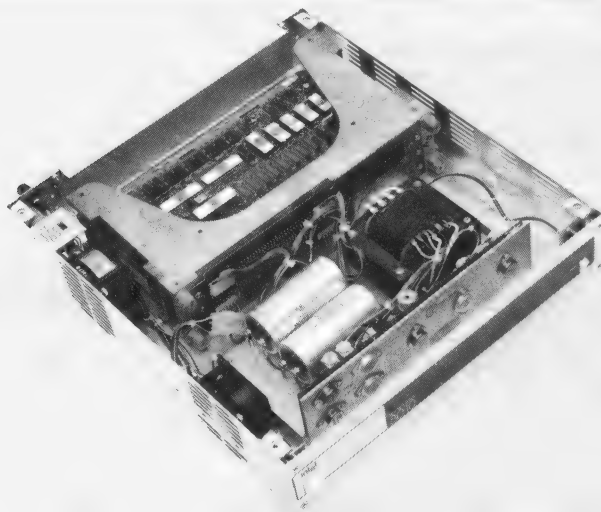
Expandable memory capacity

- 1K bytes RAM standard
- Expandable with low cost RAM, ROM, and EPROM modules

**Comprehensive system monitor
for loading, executing, and debugging
System 80/10A programs**

- Display and alter memory locations
- Read and write paper tape commands
- CRT or TTY driver

The System 80/10A is a fully packaged microcomputer utilizing the iSBC 80/10A Single Board Computer. Ideal for the OEM whose design requires low cost 19-inch RETMA compatible rack mountable packaging, the System 80/10A offers easy to use, fully programmable I/O, and the computational power of and full compatibility with Intel's iSBC 80/10A, with both RAM and EPROM memory. The enclosed power supply is designed to support not only the single board computer, but also a full complement of additional slots for expansion boards. The RETMA compatible chassis houses the computer, power supply, and fans, and has three additional slots for expansion boards.



FUNCTIONAL DESCRIPTION

The heart of the System 80/10A is the iSBC 80/10A Single Board Computer, a complete computer on a single printed circuit board. The iSBC 80/10A includes an 8080A CPU, 1K bytes of static RAM memory, sockets for 8K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous communications interface with RS232C and TTY compatibility, a multi-source, single level interrupt network, and bus drivers for memory and I/O expansion. Read only memory may be added in 1K- or 2K-byte increments using Intel 8708 EPROMs, 8758 EPROMs, 2716 EPROMs, 8308, or 2316E EPROMs. All on-board OEM read operations are performed at maximum processor speed. A block diagram of the System 80/10A functional components is shown in Figure 1.

Memory Addressing

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/10A. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

Memory Capacity

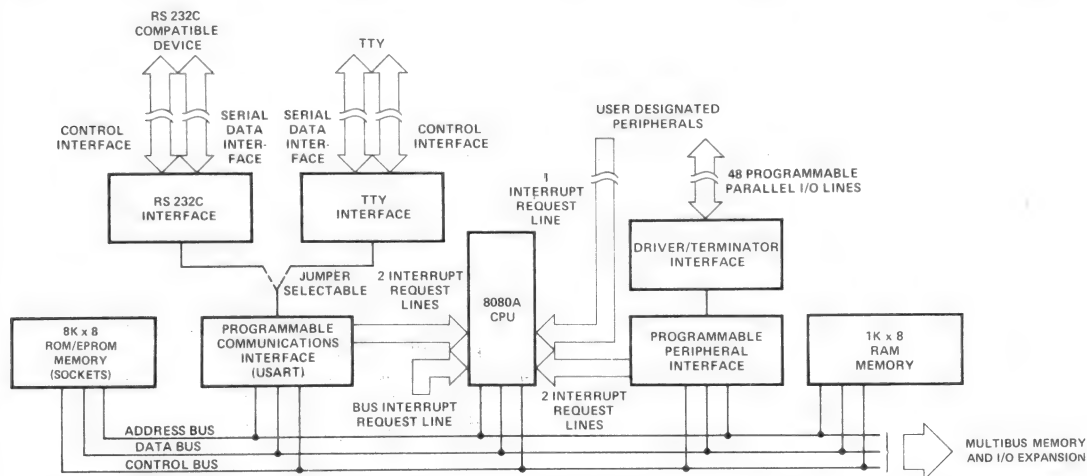
The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/last-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Parallel I/O Interface

The System 80/10A contains 48 programmable parallel I/O lines implemented using two Intel 8255A programmable peripheral interfaces. The system software may be used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable or round cable.

Serial I/O Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission techniques (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. Jumper selectable TTY or RS232C compatible interfaces are included on the board, in teletypewriters, CRTs, RS232



1. Interrupts originating from the programmable communications interface and programmable peripheral interface are jumper selectable.

Figure 1. System 80/10A Block Diagram Showing Functional Components

Port No.	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X		
2	8	X	X	X	X		
3	8	X		X		X ¹	
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

Note
1. Port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

compatible cassettes, asynchronous, and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt Request Generation — Interrupt requests may originate from six sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38₁₆.

Expansion Capabilities

System 80/10A memory and I/O capability may be increased by adding standard Intel memory and I/O boards. Memory may be expanded by adding combinations of iSBC 016 16K RAM boards and iSBC 416 16K PROM boards. Input/output capacity may be increased using iSBC 508 I/O boards, containing 32 input lines, and 32 output lines per board. Memory and I/O may be increased simultaneously by adding an iSBC 104 board containing 4K bytes of RAM, sockets for 4K bytes of PROM, 48 programmable I/O lines, and a USART.

Bus Interface — An iSBC 604 Modular Cardcage/Backplane is installed in the chassis to house the iSBC 80/10A and provide an easily accessible bus interface. The cardcage houses the iSBC 80/10A and up to three expansion boards. All iSBC 80 bus signals are present on all four mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry $\pm 5V$ and $\pm 12V$ DC.

System Monitor

A comprehensive system monitor, residing in two Intel ROMs, is included to facilitate loading, executing, and debugging programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, and display and alter CPU register contents. Monitor commands and resulting information may be initiated and displayed using a TTY or CRT terminal.

Development System Capability

The development cycle of System 80/10A-based products may be significantly reduced using an Intel microcomputer development system. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. An optional diskette operating system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-80) option provides the capability of developing and debugging software directly on the System 80/10A.

PL/M Programming Capability

Intel's high level programming language, PL/M, provides the capability to program in a natural, algorithmic

language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs.

Service Accessibility

The System 80/10A is designed for easy modular serviceability. The computer boards are accessible from the rear of the package and strain relief clamps are included to protect the I/O cabling. Wire-wrap jumpers on the iSBC 80/10A select either TTY or RS232C operation, and a jumper selectable baud rate generator on the

iSBC 80/10A is used to select the appropriate communications frequency. The System 80/10A is shipped with the jumpers set for TTY operation.

Support Documentation

The System 80/10A comes with all in-depth documentation needed to program and interface with the system. An 8080 assembly language manual, a PL/M programming manual, and a System 80/10A hardware reference manual are all included to provide clear and concise information relevant to the use of the System 80/10A.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.95 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/PROM — 0—0FFF

On-Board RAM — 3C00—3FFF

Memory Capacity

On-Board ROM/PROM — 4K bytes (sockets only)

On-Board RAM — 1K bytes

Off-Board Expansion — Up to 48K bytes using optional RAM, ROM, and PROM expansion boards.

Note

PRM/PROM may be added in 1K-byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1).

Port	8255A No. 1			8255A No. 2			8255A No. 1 Control	8255A No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note

Expandable with optional I/O boards.

Serial Baud Rates

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

System Monitor

Addresses — 0000—0560_H (ROM)

3C00_H—3C3F_H (RAM)

Commands

- D Display memory
- G Program execute
- I Insert instructions into memory
- M Move memory
- R Read hexadecimal file
- S Substitute memory
- W Write hexadecimal file
- X Examine and modify CPU registers

Drivers

- Console input
- Console output
- Reader input
- Punch output

Breakpoints — A hardware breakpoint capability may be implemented by an interrupt service routine beginning at RAM location 3C3D_H. Typically, a 2-byte call is used. Interrupt generation at the breakpoint may be accomplished by user hardware or by insertion of single byte calls at instruction boundaries.

Equipment Supplied

System 80/10A computer with power supply, cardcage, dual fans, and ROM-based system monitor.

115V power cable

Serial I/O cable

115V and 230V fuses

Compatible Equipment

Compatible Boards

iSBC 016 16K byte RAM

iSBC 032 32K byte RAM

iSBC 094 4K byte CMOS RAM

iSBC 104 4K byte RAM, 8K byte PROM, 48 programmable I/O lines, USART

iSBC 108 8K byte RAM, 8K byte PROM, 48 programmable I/O lines, USART

iSBC 116 16K byte RAM, 8K byte PROM, 48 programmable I/O lines, USART

iSBC 310 High Speed Math Unit

iSBC 416 16K byte PROM

iSBC 501 DMA Controller

iSBC 508 32 input lines/32 output lines

iSBC 517 Combination I/O Board
 iSBC 519 Programmable Parallel I/O Board
 iSBC 534 Serial Communications Board
 iSBC 556 Optically Isolated I/O Board
 iSBC 711 D/A Input Board
 iSBC 724 A/D Output Board
 iSBC 732 Combination A/D, D/A, I/O Board

Compatible Peripherals

iSBC 201 Single Density Diskette Controller
 iSBC 202 Double Density Diskette Controller
 iSBC 211 Single Diskette System
 iSBC 212 Dual Diskette System

Compatible Hardware

iSBC 530 Teletypewriter Adapter
 iSBC 956 Parallel I/O Cable Set

Compatible Software

RMX/80 Real-Time Multi-Tasking Executive

Serial Communication Characteristics

Synchronous — 5—8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5—8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Single-level with on-board logic that automatically vectors processor to location 38₁₆ using RESTART 7 instruction. Interrupt requests may originate from user specified I/O (2), the programmable peripheral interface (2), or USART (2).

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C or a 20 mA current loop TTY interface (jumper selectable)

Interrupt Requests — All TTL compatible (active-low)

System Clock

2.048 MHz \pm 0.1%

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

Line Drivers and Terminators

I/O Drivers — The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 80/10:

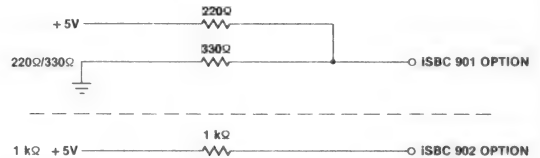
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Port 1 has 25 mA totem-pole drivers and 1k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	25
Address	Tri-state	25
Commands	Tri-state	25

Physical Characteristics

Height — 3.5 in. (8.90 cm)

Width

At Front Panel: 19 in. (48.3 cm)

Behind Front Panel: 17 in. (43.2 cm)

Depth — 20 in. with all protrusions (150.8 cm)

Weight — 37 lb (16.0 kgm)

Electrical Characteristics

Input Power

Frequency	Voltage		Current (max)
	Standard	Option	
47—63 Hz	115V AC \pm 10%	230	270W

Voltage	Supply Current	Power Available without PROM & Termination Packs Installed	Power Available with PROM & Termination Packs Installed*	Over-Voltage Protection
+12	2A	1.86A	1.6A	+14 to +16V
+5	14A	11.1A	10A	5.8 to 6.6V
-5	0.9A	0.898A	0.7A	5.8 to -6.6V
-12	0.8A	0.625A	0.625	-14 to -16V

*PROMs are 4 each of 8708's; termination packs are 10 each of 220 Ω /330 Ω .

Environmental Characteristics

Operating Temperature — 0°C to 50°C

Non-Operating Temperature — -40°C to 85°C

SYSTEM 80/10A

Reference Manuals

9800316 — System 80/10A Hardware Reference Manual (SUPPLIED)

8080 Assembly Language Manual (SUPPLIED)

iSBC 80/10A Schematics (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
Sys 80/10A	System 80/10A

PACKAGED
SYSTEMS

A rack-mountable, packaged microcomputer for OEM applications

Processing power from the 8085A based iSBC 80/30 Single Board Computer

Fully supported under Intel's RMX/80 Real-Time Multi-Tasking Executive

Full MULTIBUS control logic allowing additional masters to share system bus

Two programmable 16-bit BCD or binary timers

12-level programmable vectored priority interrupt control

Expandable memory capacity

- 16K bytes dual ported RAM standard
- Up to 8K PROM/EPROM capacity standard
- Expandable with RAM, ROM, EPROM, and peripheral controller modules

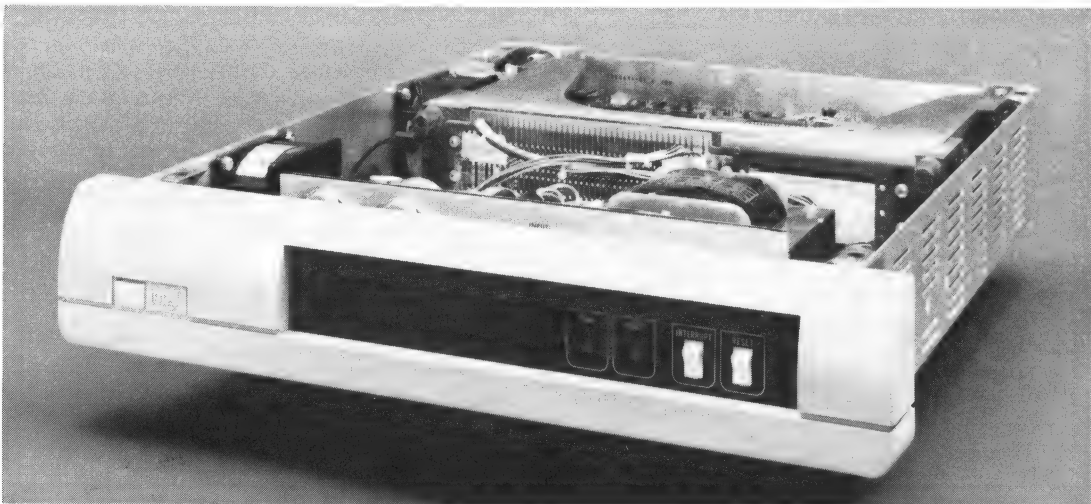
Fully programmable I/O

- Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rate generation
- Socket for 8041/8741A Universal Programmable Interface
- 24 lines parallel I/O standard
- Expandable with low cost digital and analog I/O modules

Comprehensive system monitor in PROM for loading, executing, and debugging System 80/30 programs

- Display and alter memory locations
- Display and alter registers
- Execute single step programs
- Read and write paper tape commands
- Breakpoints at execute time
- RS232 device driver

The Intel System 80/30 is a fully packaged microcomputer utilizing the iSBC 80/30 Single Board Computer. Ideal for the OEM whose design requires 19-inch RETMA compatible rack mountable packaging, the System 80/30 offers easy to use, fully programmable I/O plus the computational power and RAM, ROM, and EPROM memory of the iSBC 80/30. The enclosed power supply is designed to support both the single board computer and a full complement of expansion boards. The RETMA compatible chassis houses the computer, power supply, and fans. Three additional slots are available for expansion boards.



FUNCTIONAL DESCRIPTION

The heart of the System 80/30 is the iSBC 80/30 Single Board Computer, a complete computer on a single printed circuit board. The iSBC 80/30 includes an 8085A CPU, 16K bytes of dual ported dynamic RAM memory with on-board refresh, sockets for up to 8K bytes of ROM/EPROM memory, 24 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, sockets for the 8041/8741A Universal Programmable Interface with interchangeable line drivers and terminators, a programmable synchronous/asynchronous RS232C communications interface, programmable 12-level vectored priority interrupt structure, programmable interval timers, and bus drivers for memory and I/O expansion. Extended memory features include a dual port controller which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the iSBC 80/30 or from any other bus master in the chassis. On-board RAM accesses do not require the MULTIBUS, making the bus available for any other concurrent operations requiring the use of the MULTIBUS, such as DMA data transfers. Dynamic RAM refresh can be accomplished transparently by the iSBC 80/30 for accesses originating from the CPU. Read only memory may be added in 1K-byte increments using Intel 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel 8308 Masked ROMs, in 2K-byte increments using Intel 8716 EPROMs or 8316B Masked ROMs, and in 4K-byte increments using Intel 2332 Masked ROMs. All on-board EPROM/ROM memory operations are performed at maximum processor speed. A block diagram of the System 80/30 functional components is shown in Figure 1.

CPU

Intel's powerful 8-bit, n-channel MOS 8085A CPU, fabricated on a single LSI chip, is the central processor for

the iSBC 80/30. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

Memory Addressing

The 8085A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out stack to store the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. The stack provides subroutine nesting bounded only by memory size.

Memory Space Assignment — Memory space assignment may be selected independently for on-board and MULTIBUS RAM accesses. The on-board 8085A can access RAM anywhere within the 0 to 64K address space. The iSBC 80/30 provides extended addressing jumpers to allow the on-board RAM (as addressed by external MULTIBUS resident devices) to reside within a one megabyte address space. In addition, jumper options are provided which allow the user to reserve 8K or 16K bytes of on-board RAM for use by the on-board 8085 CPU only.

Parallel I/O Interface

The System 80/30 contains 24 programmable parallel I/O lines implemented using Intel 8255A programmable peripheral interfaces. The system software may be used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O

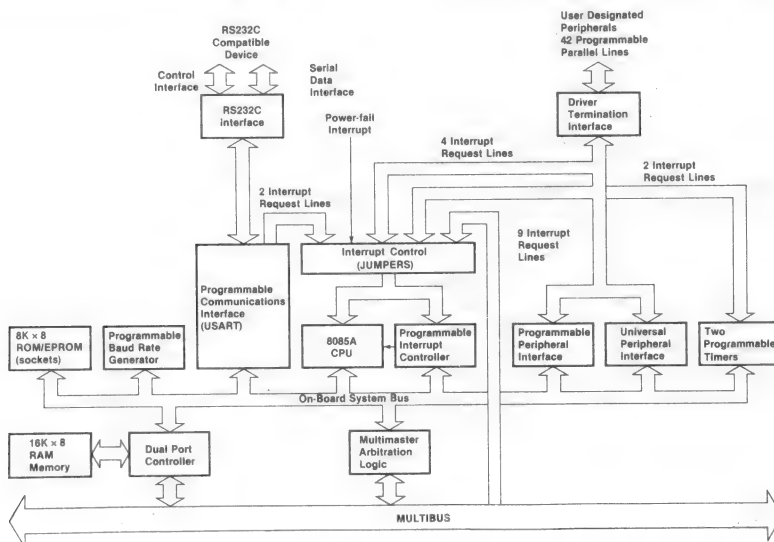


Figure 1. System 80/30 Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X		X ¹	
	4	X		X		X ¹	
Note 1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.							

Table 1. Input/Output Port Modes of Operation

configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable. The user may design his own cable or order the iSBC 956 Parallel I/O Cable Set.

Universal Programmable Interface

The iSBC 80/30 provides sockets for a user supplied Intel 8041/8741A Universal Programmable Interface (UPI) chip and the associated line drivers and terminators for the UPI's I/O ports. The 8041/8741A is a single chip microcomputer containing a CPU, 1K bytes of ROM (8041) or EPROM (8741A), 64 bytes of RAM, 18 programmable I/O lines, and an 8-bit timer. Special interface registers are included in the chip to enable the 8041 to function as a slave processor to the iSBC 80/30's 8085 CPU. The UPI allows the user to specify algorithms for controlling user peripherals directly in the chip, thereby relieving the 8085A for other system functions. The UPI socket is connected to line driver/terminator sockets by fixed traces and factory-installed jumpers; the driver/terminator sockets are wired to edge connectors on the PCB (see Figure 2). The port lines from the edge connector will thus be unidirectional in groups of four lines, the direction being determined by whether the socket is occupied by a driver or terminator and by the user programming of the 8041/8741A. The jumpers may be changed by the user to allow a mix of input and output lines on Port 2 of the 8041/8741A as shown. The 14-pin sockets accept SN7400-series drivers or Intel iSBC 901, 902 terminators. An RS232C driver and receiver are provided for applications using the UPI for simple serial interfaces (for additional information see the UPI-41 User's Manual).

Serial I/O Interface

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Re-

ceiver/Transmitter (USART) is contained on the board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmis-

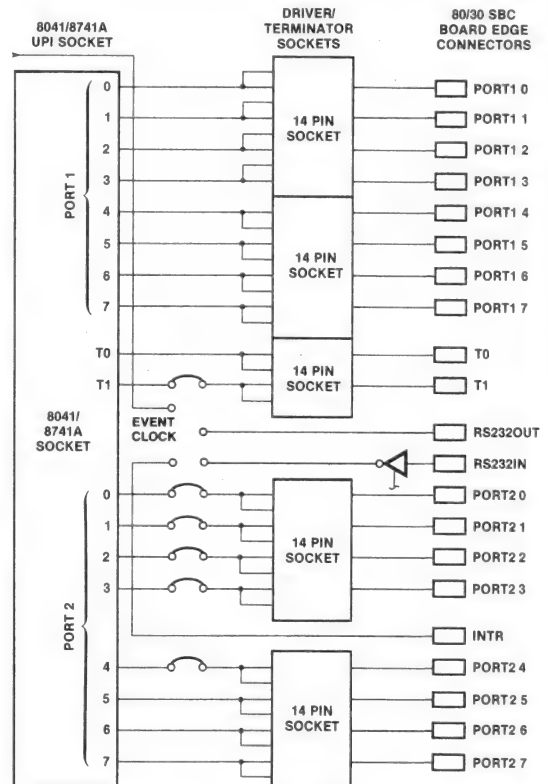


Figure 2. 8041/8741A Socket Port Schematic

sion rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of the RS232C compatible interface on the board allows the system to be used directly with CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat cable. This cable is supplied with the system. A 20 mA TTY compatible interface may be achieved by using the optional iSBC 530 Teletypewriter Adapter.

Multimaster Capability

The System 80/30 is a full computer with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capability and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the MULTIBUS), the System 80/30 provides full bus arbitration control logic. This control logic allows additional multimaster single board computers or other high speed controllers to share the MULTIBUS in serial (daisy chain) priority fashion, or in parallel priority fashion with the addition of an external priority network. The MULTIBUS controller provides its own clock, which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus may proceed asynchronously. Thus, transfer speed is dependent upon transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second.

Programmable Timers

The System 80/30 provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval Timer. Two of these timers are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or the outputs from the 8255A programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port. The systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications;

special commands are included so that the contents of each counter can be used "on the fly".

Interrupt Capability

Twelve-Level Vectored Interrupt — The iSBC 80/30 provides vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A CPU. Requests are routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority), and each input generates a unique memory address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A jump instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap input may be masked via software.

Function	Operation
Interrupt on terminal count	Generates interrupt request when terminal count is reached. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. Output goes low for one input clock cycle; the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output remains high until one-half the count has been completed, and goes low for the other half of the count.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.

Table 2. Programmable Timer Functions

Eight-Level Vectored Interrupt — An Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system re-

quirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage (via software) of a single byte to the interrupt mask register of the PIC.

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Interrupt Addressing — The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8085A jump instruction at each of these addresses can then provide linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation — Interrupt requests may originate from 18 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers and by the UPI. Eight additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the MULTIBUS, and two interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Expansion Capabilities

System 80/30 resources may be increased by adding combinations of iSBC RAM, PROM, digital I/O, and ana-

log I/O boards or combination I/O and memory expansion boards.

Peripherals — Mass storage capacity may be added to the System 80/30 with Intel's flexible diskette peripherals. The iSBC 201 Diskette Controller and iSBC 202 Double Density Controller are powerful, easy to use plug-in modules which are compatible with multiple manufacturers' diskette drives. For a completely tested mass storage peripheral, the iSBC 212 Dual Drive Diskette subsystem is available.

Bus Interface — A modular cardcage/backplane is installed in the chassis to house the iSBC 80/30 and provide an easily accessible bus interface. The cardcage also houses up to three additional expansion boards. All iSBC 80 bus signals are present on all mating connectors.

System Monitor

A comprehensive system monitor, residing in a 2716 EPROM, is included to facilitate loading, executing and debugging programs. Monitor commands give the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, display and alter CPU register contents, and execute programs in single step mode. Breakpoints may be set when starting execution; the system will stop to allow use of the monitor's other debug facilities whenever the CPU attempts to access an instruction from one of the specified breakpoint locations. Monitor commands and resulting information may be initiated and displayed using a CRT or other RS232 device.

Real-Time Software

The System 80/30 is totally compatible with Intel's RMX/80 Real-Time Multi-Tasking Executive. User programs (tasks) can take advantage of RMX/80 to do all necessary scheduling, intertask communication, and memory space allocation. RMX/80 also provides standard I/O support software such as the disk file handler, the Intel analog board handler, and the terminal handler. Refer to the RMX/80 User's Guide for complete details.

System Development Capability

The development cycle of System 80-based products may be significantly reduced using the Intellec series microcomputer development systems. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. Optional diskette operating software for the development system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-85) option provides the capability to use the development system to develop and debug software directly on the System 80/30.

Programming Capability

Intel's high level resident programming languages, PL/M-80 and FORTRAN-80, provide the capability to pro-

gram in natural, algorithmic languages and eliminate the need to manage register usage or allocate memory for system or application programs.

Service Accessibility

The System 80/30 is designed for easy modular servicing. The computer boards are accessible from the rear of the package and strain relief clamps are included to

protect any I/O cabling added by the user. The power supply may be removed from the system to allow easy backplane servicing. An RS232C cable and connector are included as standard.

Support Documentation

A documentation set that covers each component of the System 80/30 is supplied with the system.

SPECIFICATIONS

Word Size

Instruction: — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.45 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-7FF (using 8708 or 2758 EPROMs or 8308 ROMs); 0-0FFF (using 2716 EPROMs or 2316E ROMs); 0-1FFF (using 2332 ROMs)

On-Board RAM — 16K bytes ending on a 16K boundary

Memory Capacity

On-Board ROM/EPROM — Up to 8K bytes (sockets only)

On-Board RAM — 16K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM

Note

ROM/EPROM may be added in 1K-, 2K- or 4K-byte increments.

I/O Addressing

On-Board Programmable I/O — see Table 1

Port	8255A				8041/8741A		USART	
	1	2	3	Control	Data	Control	Data	Control
Address	E8	E9	EA	EB	E4	E5	EC	ED

I/O Capacity

Parallel — 42 programmable lines using Intel's 8255A (24 I/O lines) and an optional 8041/8741A (18 I/O lines). Refer to Figures 1 and 2 for details.

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Serial Baud Rates

Frequency (kHz)	Baud Rate (Hz)	
	Synchronous	Asynchronous (Program Selectable)
153.6	—	+ 16 + 64 9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
6.98	6980	— 110

Note

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253).

Interrupts

Register Address for 8259A (hex notation, I/O address space)

- DA Interrupt request register
- DA In-service register
- DB Mask register
- DA Command register
- DB Block address register
- DA Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels — Interrupt levels routed to the 8085A CPU automatically direct the processor to unique memory locations.

Interrupt Input	Memory Address	Priority	Type
TRAP	24 ₁₆	Highest	Non-maskable
RST 7.5	3C ₁₆	<div style="text-align: center;"> \updownarrow </div>	Maskable
RST 6.5	34 ₁₆		Maskable
RST 5.5	2C ₁₆		Maskable
		Lowest	

Timers

Register Address (hex notation, I/O space)

- DF Control register
- DC Timer 0
- DD Timer 1
- DE Timer 2

Note

Timer counts loaded as two sequential output operations to same address as given.

Input Frequencies

Reference ¹	Event Rate ²
2.4576 MHz \pm 0.1% (0.407 μ s period, nominal)	2.46 MHz max
1.2288 MHz \pm 0.1% (0.814 μ s period, nominal)	
or 153.60 kHz \pm 0.1% (6.510 μ s period, nominal)	

Notes

1. Above frequencies are user selectable.
2. Maximum rate for external events in event counter function.

Interfaces

MULTIBUS — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

System Monitor

Address — 0000-069C_H (ROM), 3F80_H-3FFF_H (RAM)

Commands

- D Display memory
- G Program execute
- I Insert instruction into memory
- M Move memory
- N Execute next instruction
- R Read hexadecimal file (TTY only)
- S Substitute memory
- W Write hexadecimal file (TTY only)
- X Examine and modify CPU registers

Drivers — Console input, console output, reader input (TTY only), punch output (TTY only)

Breakpoints — Program breaking may occur upon any of up to system seven conditions. Breaks are implemented via the programmable interrupt controller. When a break occurs the break level, all CPU registers, and the next instruction (OP CODE) are displayed at the console.

Baud Rate — Baud rate search capability automatically sets serial baud rate to that of the system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, 4800, and 9600.

System Clock (8085A CPU)

2.76 MHz \pm 0.1%

Compatible Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Parallel I/O	50	0.1	3M 3415-000 Flat TI H312125 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

Line Drivers and Terminators

I/O Drivers — The following line drivers are compatible with the I/O driver sockets on the iSBC 80/30

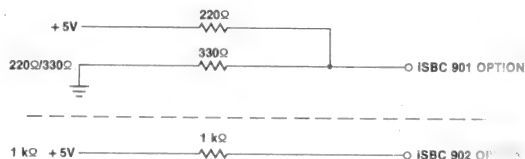
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 k Ω terminators.

I/O Terminators — 220 Ω divider or 1 k Ω pull-up.



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

Physical Characteristics

Height — 3.5 in. (8.90 cm)

Width

At Front Panel: 19 in. (48.3 cm)

Behind Front Panel: 17 in. (43.2 cm)

Depth — 20 in. (50.8 cm) with all protrusions

Electrical Characteristics

Input Power

Frequency	Voltage	Current
47-63 Hz	Standard — 115V AC \pm 10%	270W max
	Option — 230V AC \pm 10%	

Output Power Available for Expansion Boards

Voltages	+ 5	+ 12	- 5	- 12
Supply current (max)	14.0A	2.0A	0.9A	0.8A
Power available (by configuration)				
Without EPROM ¹	10.5A	1.7A	0.9A	0.7A
With 8041/8741A ²	10.4A	1.7A	0.9A	0.7A
With iSBC 530 ³	10.5A	1.6A	0.9A	0.6A
With 2K bytes EPROM ⁴ (using 8708)	9.6A	1.6A	0.8A	0.7A
With 2K bytes EPROM ⁴ (using 2758)	9.4A	1.7A	0.9A	0.7A
With 4K bytes EPROM ⁴ (using 2716)	9.4A	1.7A	0.9A	0.7A
With 8K bytes EPROM ⁴ (using 2332)	9.4A	1.7A	0.9A	0.7A
Over-voltage protection	+ 5.8 to + 6.6V	+ 14 to + 16V	- 5.8 to - 6.6V	- 14 to - 16V

Notes

- Does not include power required for optional EPROM/ROM, 8041/8741A, I/O drivers, or I/O terminators.
- Does not include power required for optional EPROM/ROM, I/O drivers, or I/O terminators.
- Does not include power required for optional EPROM/ROM, 8041/8741A, I/O drivers, or I/O terminators. Power for iSBC 530 is supplied through the serial port connector.
- Includes power required for two EPROM/ROM chips, 8041/8741A, and 220Ω/330Ω input terminators installed for 34 I/O lines (all terminator inputs low).

Environmental Characteristics

Operating Temperature — 0°C to 50°C

Equipment Supplied

iSBC 80/30; system chassis with power supply, card-cage and dual fans; ROM-based system monitor.

115V power cable

115V and 230V fuses

Connector pack with parallel and serial connectors

Reference Manuals

9800707 — System 80/30 Documentation Package (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SYS80 KIT 30	System 80/30



iSBC 660 SYSTEM CHASSIS

Eight-slot cardcage and backplane for iSBC computers and expansion boards

Attractive, versatile pop-off front panel

Heavy duty power supply with all standard iSBC voltages

19-inch wide rack mountable chassis

Compatible with all Intel single board computers

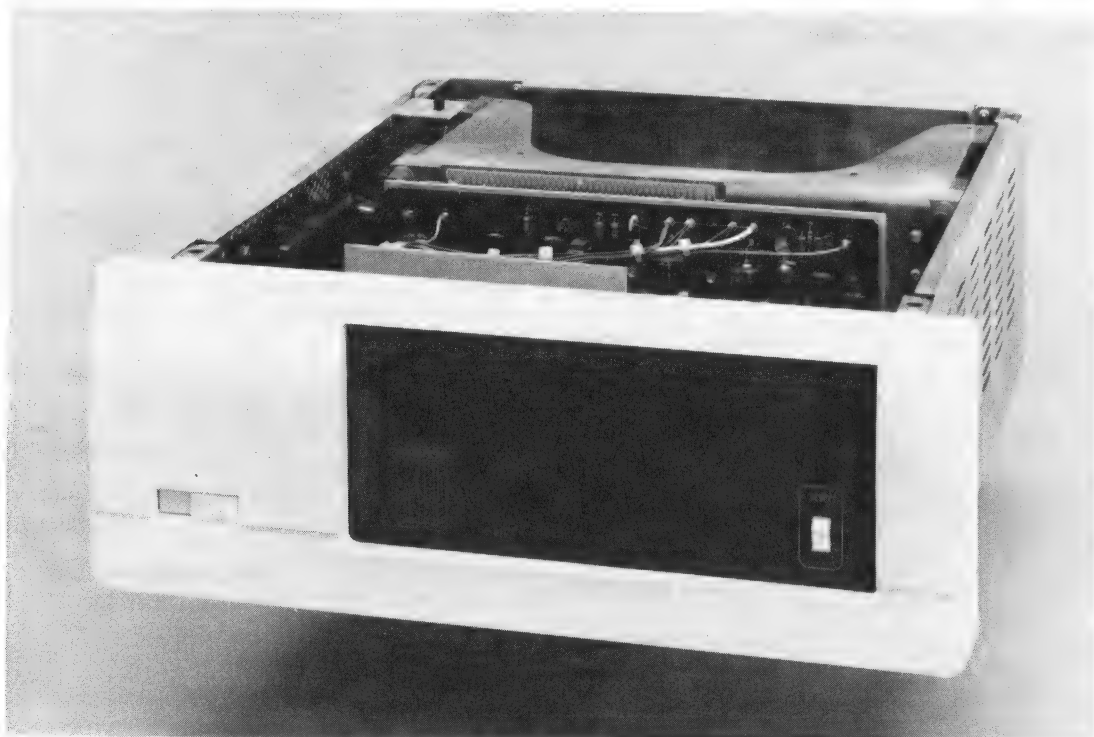
Horizontal board mounting for compactness

Forced air cooling

110/220V, 50/60 Hz operation

The iSBC 660 System Chassis is an attractive, 7-inch high system chassis designed for use with Intel OEM computers. It has eight slots for single board computers, memory, I/O, or other expansion modules. The iSBC 660 is ideal for applications requiring multiple board solutions. DC power output is provided at +12V, +5V, -12V, and -5V levels. The current capabilities of each of these output levels have been chosen to provide power over a 0°C to 50°C temperature range for the majority of applications requiring combinations of computers, memories, peripherals, and other I/O capabilities. Current limiting and over-voltage protection is provided at all outputs. Standard logic recognizes a system AC power failure and generates a TTL signal for use in power-down control. For user convenience, a reset switch is provided on the front panel. The reset signal generated and sent to the system bus can be used for external system control.

PACKAGED
SYSTEMS



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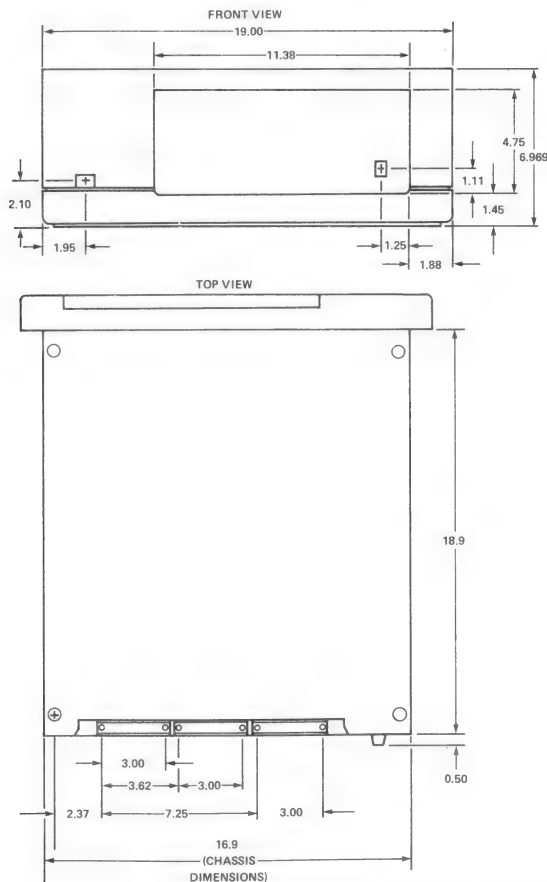


Figure 1. ISBC System Chassis Dimensions

SPECIFICATIONS

Electrical Characteristics

Input Power

Frequency: 47 to 63 Hz

Voltage: 115V $\pm 10\%$, 230V $\pm 10\%$

Current: 584W max

Output Power

Power	Output Current (max)	Over-Voltage Protection
+ 12V	4.5A	15V $\pm 1V$
+ 5V	30A	6.2V $\pm 0.4V$
- 5V	1.75A	- 6.2V $\pm 0.4V$
- 12V	1.75A	- 15V $\pm 1V$

Remote Sensing — Sensing provided for +5V output line regulation

Line Regulation — $\pm 0.1\%$ for 10% line change

Load Regulation — $\pm 0.1\%$ for 50% load change

Output Ripple and Noise — 100 mV peak-to-peak maximum (DC to 500 kHz)

Transient Response — Less than 50 μs for 50% load change

Power Failure Indication

An active high, TTL compatible output logic level is provided when input voltage falls below 102 V AC (206 V AC) to indicate low AC input voltage conditions. All output voltages will remain within spec for one-half cycle (~ 8.3 ms @ 60 Hz).

Physical Characteristics

Height — 7 in. (17.8 cm)

Width

At Front Panel: 19 in. (48.3 cm)

Behind Front Panel: 17 in. (43.2 cm)

Depth — 20 in. (50.8 cm) with all protrusions

Environmental Characteristics

Temperature

Operating: 0°C to 50°C

Non-Operating: -40°C to +85°C

Humidity — Up to 90% relative, non-condensing

Equipment Supplied

iSBC 660 System Chassis with power supply, dual fans, 8-slot cardcage and backplane, and pop-off front panel

Reference Manuals

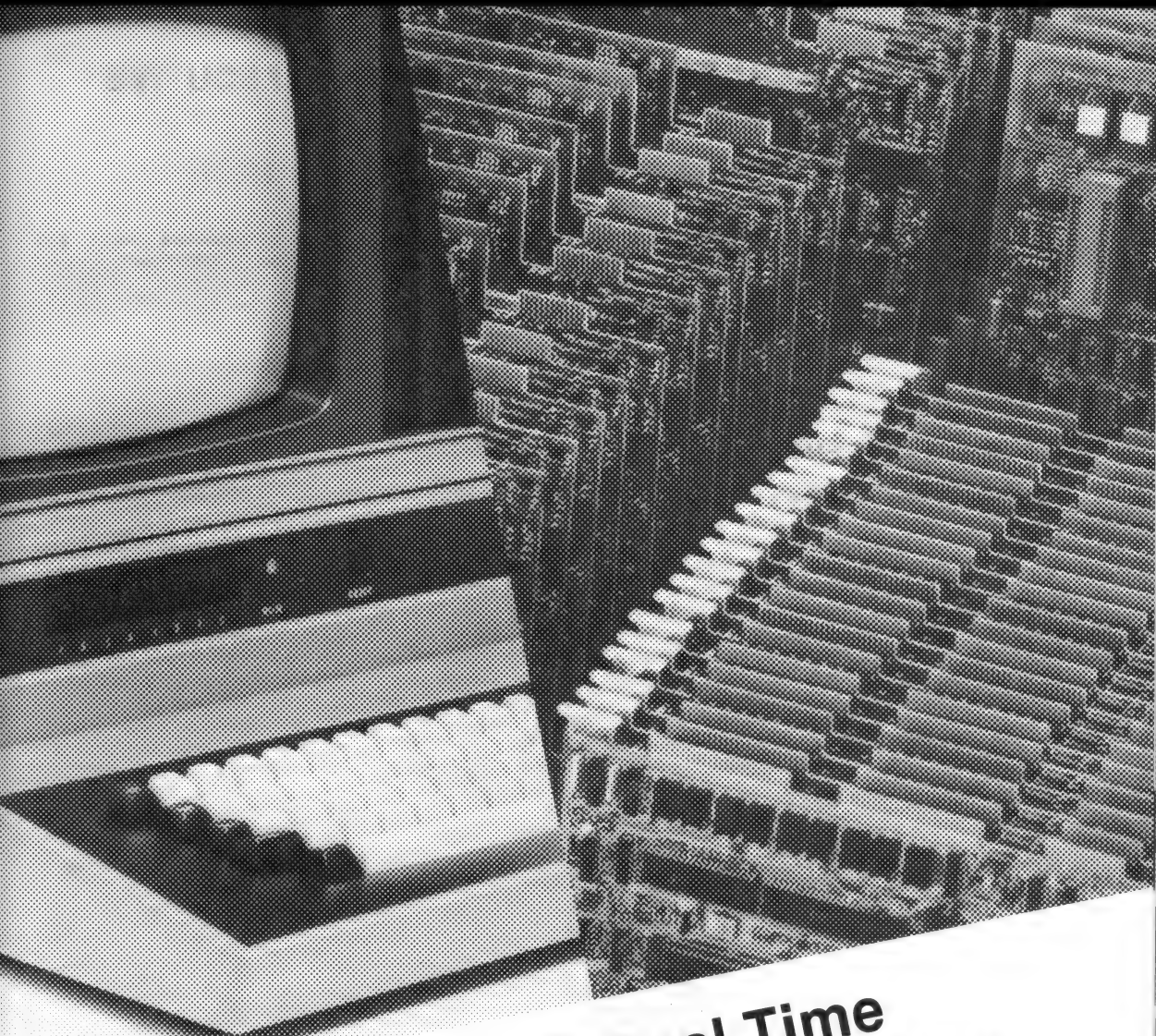
9800505A — iSBC 660 Hardware Reference Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
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SBC 660	iSBC 660 system chassis
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8 Real-Time Multi-Tasking Executive

RMX/80 REAL-TIME MULTI-TASKING EXECUTIVE

INTRODUCTION

Intel's RMX/80 Real-Time Multi-Tasking Executive provides users of Intel's single board computers (iSBC 80 and System 80 series) with a simple to use tool for implementing microcomputer systems. The RMX/80 diskette file system, terminal handler, analog driver, and debugger have all been designed and optimized specifically for the iSBC 80 series. RMX/80's modular design, consisting of a series of linkable and relocatable modules, can be configured to optimize system software for any specific application.

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RMX/80

REAL-TIME MULTI-TASKING EXECUTIVE

Operation on Intel iSBC 80 and System 80 microcomputers

2K-byte memory resident nucleus

User configurable via linkable modules

Capability for PROM resident systems

Synchronization and control of multiple tasks

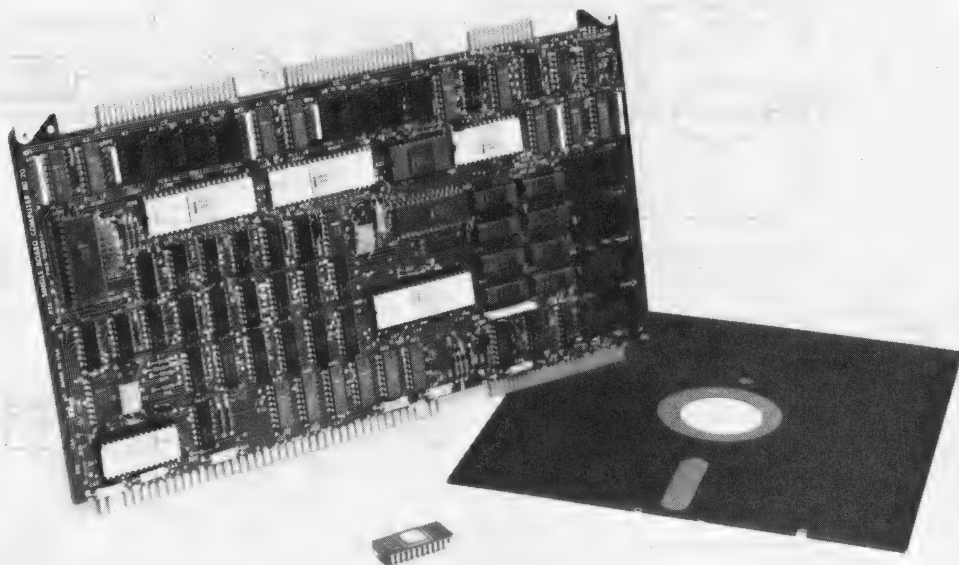
Comprehensive I/O device support

Diskette file system including program loading

Software debug module

The RMX/80 Real-Time Multi-Tasking Executive is an easy to use but sophisticated real-time multi-tasking executive designed for operation on Intel iSBC single board computers and System 80 packaged systems. It provides a means for concurrently monitoring and controlling multiple external events occurring asynchronously in real time. In such applications, RMX/80 provides a framework within which system developers may immediately implement software for their particular application, avoiding specific details of system interaction. RMX/80 contains all major real-time functions including system resource access based upon task priority, intertask communication, interrupt driven control for standard devices, real-time clock control, and interrupt handling as well as other optional features. These functions eliminate the need to implement detailed real-time coordination for specific applications, greatly simplifying application development, particularly in areas of control, test and measurement, instrumentation, data communications, and specialized data processing systems. RMX/80 is configured using Inteltec microcomputer development systems and includes support for standard iSBC 80 I/O devices, an interactive software debug module, and a free space allocation facility.

RMX/80



FUNCTIONAL DESCRIPTION

Operation

Tasks — All RMX/80 operations are based around individual tasks. A task is a program with unique data and stack which operates asynchronously with other tasks in the system. Synchronization and/or intertask data transfer is supported via exchanges, a software mechanism through which messages (information) are transferred. Actual task communication occurs via write (SEND) and read (WAIT) operations, which allow tasks to communicate with each other or with system input/output devices.

System Flow — A diagram of the RMX/80 system flow is shown in Figure 1. The four illustrations show the four main elements of RMX/80 flow. Figure 1-A shows intertask communication in which task "A" sends a message to an exchange where it is held until task "B" requests the message via an accept command. In Figure 1-B, task "B" waits for a message from task "A" until the data is available or until a certain time period has passed, whichever occurs first. Illustration 1-C shows that any task may suspend or resume any other task. In 1-D, an I/O interrupt is transformed into a message which task "A" receives via a wait command. Task "A" then performs appropriate interrupt processing. The major RMX/80 functions are shown in Table 1.

Generation

RMX/80 consists of a library from which required routines are configured with application tasks to form a full system. Users may generate the final system by

selecting appropriate modules, and relocating and linking them with user generated tasks on an Intel Intellec microcomputer development system. As shown in Figure 2, RMX/80 generation consists of creating an assembly language source file to specify options to the user's real-time application. After assembly, the relocatable object representing these parameters is linked with the relocatable object representing required RMX/80 functions (RMX/80 library), and with the user tasks, which may be written using PL/M-80 and assembly language. Output of the linker is a representation of the user's real-time system and may be placed in PROM for execution or debugging via an Intel in-circuit emulator.

RMX/80 System Organization — The RMX/80 system is organized in such a way that code, data, and stack can be placed in separate areas of memory. This means that peripheral devices are not necessary to load RMX/80. Instead, PROMs containing nonvolatile code portions of an RMX/80 system may be installed directly into ISBC systems. In the case of power failure, PROM-resident program instructions are not destroyed and the system may be restarted when power is restored.

Features

RMX/80 provides users of Intel single board computers (ISBC 80 and System 80 series) a simple to use tool for implementing microcomputer systems which monitor and/or control multiple events concurrently. Major features of RMX/80 include:

Microcomputer Operation — Operation on ISBC and System 80/10 and 80/20 microcomputers.

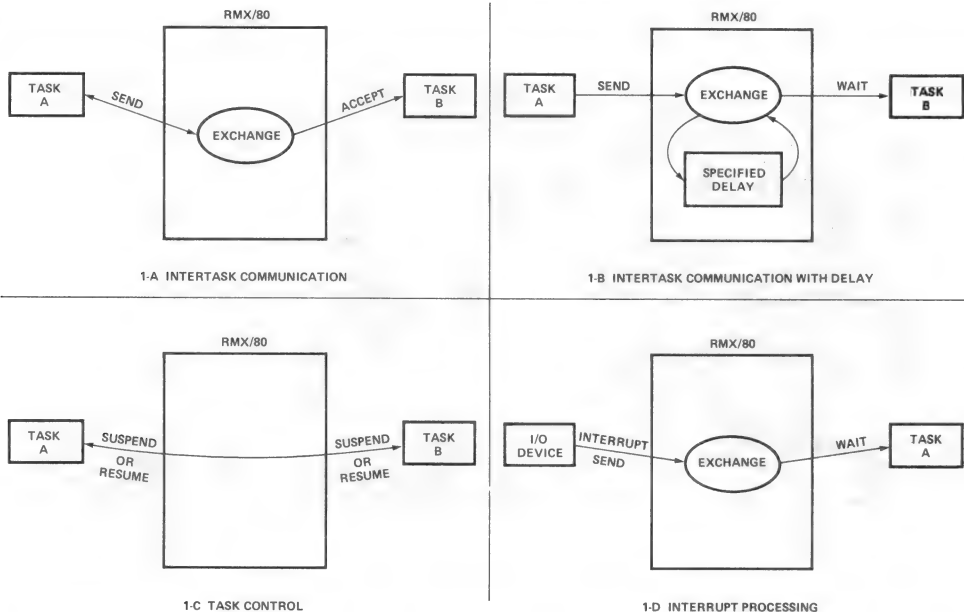


Figure 1. RMX/80 System Flow

Function	Operation
Initialize	Establishes task definition and task priority. Utilized at beginning of RMX/80 execution.
Send	Transmits message to exchange, where message is retained until accepted by another task.
Interrupt send	Accepts interrupt and converts it to message which is sent to appropriate exchange.
Wait	Delays task execution until message is available at exchange. Optionally delays task execution for specific number of time units, or until message is received, whichever occurs first.
Accept	Receives messages pending at exchange. Accept command does not delay calling task; instead it returns either message address or indicator that no message is available.
Suspend	Removes specified task from lists of tasks available for execution.
Resume	Removes task from suspended state, allowing it to execute (based upon task priority).

Table 1. Major RMX/80 Functions

2K-Byte RMX/80 Nucleus — Includes task management, real-time control, interrupt handling, and Intertask communication facilities.

Customization — Based upon system software requirements, only required RMX/80 modules are linked into final system.

Memory Segmentation — Segmentation of volatile and nonvolatile memory throughout RMX/80 permits ROM-/EPROM/PROM-resident versions, eliminating need for bootstrap devices as well as retaining program instructions in power-down situations.

Full Multi-Tasking Operation — Number of tasks is limited only by available memory.

Priority Access to System Resources — RMX/80 supports 254 separate user task priorities.

Full Intertask Communication and Synchronization — Allows tasks to send information to other tasks and to cause other tasks within the system to execute at appropriate times.

Real-Time Clock Control — Allows task activation based upon specified time delays.

Interrupt Driven Input/Output Capability — Permits concurrent I/O and task processing.

Easy Addition of Special User I/O Tasks — Allows real-time support of devices required by individual applications.

RMX/80 Support — Support of operator console (CRT or TTY) and Intel standard devices, including ISBC 201, 202, 211, and 212 diskette systems, ISBC 310 High Speed Mathematics Unit, and ISBC 711, 724, and 732 analog subsystems.

Diskette File Structure — Includes facilities to open and close files, create and delete files, provide random and sequential diskette read and write, and provide dynamic allocation of file storage. Compatible with Intel development system (ISIS-II) file structure.

Terminal Handler — Allows tasks to send and receive data via a console device. Additionally provides a task priority output path for messages that must be displayed immediately.

Program Loading from Diskette — Programs may be loaded into areas of memory specified at system generation.

Interactive Debugging Tool — Eases debugging in multi-tasking environments. Designed to operate with Intel ICE in-circuit emulators to provide additional debugging capabilities.

PL/M Compability — RMX/80 allows use of PL/M compiler and macroassembler to develop application tasks.

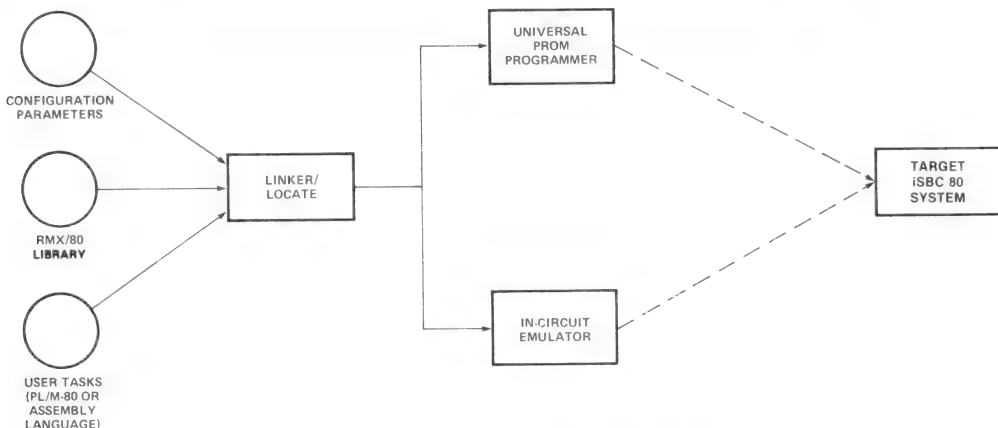


Figure 2. RMX/80 System Generation

Benefits

RMX/80's modular design and broad range of system oriented features provide the following benefits to microcomputer system builders:

Simplification of Development — Because RMX/80 provides real-time system coordination, users can concentrate on their specific software application with RMX/80 supporting details of synchronization, communication, I/O, and interrupt handling.

Earlier Project Completion — Critical projects are completed earlier because RMX/80 provides major portions of software requirements for real-time systems.

Lower Development Cost — RMX/80's real-time capabilities eliminate need to develop similar capabilities for specific applications, significantly lowering software development cost.

Low Recurring Cost — RMX/80's modular design minimizes memory requirements. RMX/80's PROM residency also lowers recurring system cost by eliminating the need for expensive bootstrap devices and core memory or battery back up to retain program instructions during power outages.

Easier Enhancement and Maintenance — RMX/80's modular structure simplifies enhancement and maintenance of real-time systems, lowering costs and reducing the time required to implement such changes.

SPECIFICATIONS

Generation Environment

Intellec Microcomputer Development System including
ISIS-II Diskette Operating System
Minimum 48K bytes of memory
Dual floppy diskettes

Shipping Media

Diskette

Reference Manuals

9800522A — RMX/80 User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

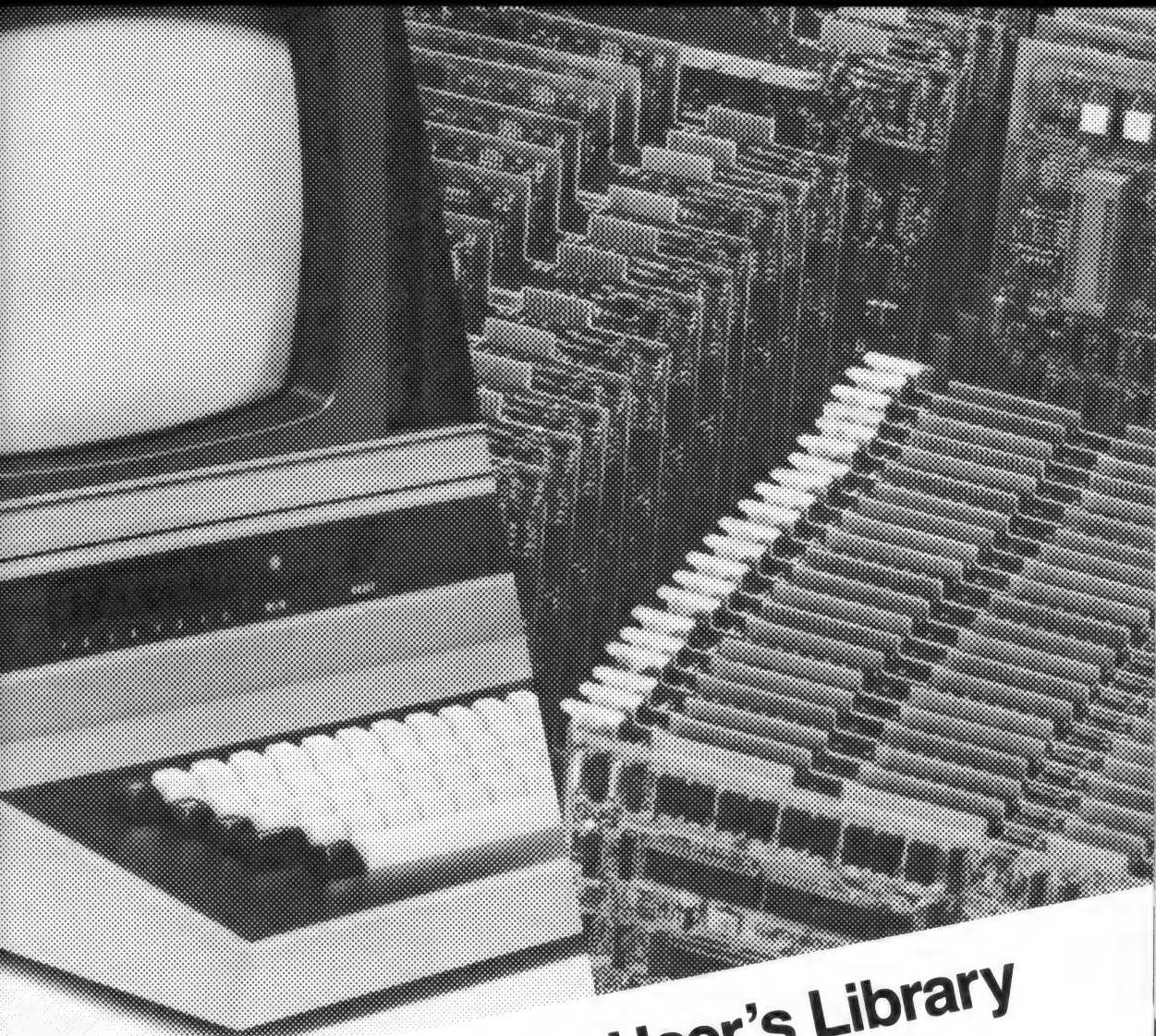
ORDERING INFORMATION

Part Number Description

RMX/80*	Real-time multi-tasking executive
---------	-----------------------------------

Note

*RMX/80 is copyrighted by Intel Corporation and is available only under a license agreement with Intel which will be required with each program delivered.



9 User's Library

INSITE USER'S PROGRAM LIBRARY

INTRODUCTION

Insite, the Intel Software Index and Technology Exchange with almost 400 contributed 8-bit programs, further facilitates the use of Intel microcomputer products and the integration of iSBC 80 single board computers and systems into OEM products. This section provides information describing Insite and includes partial listings of the 8-bit program library.

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INSITE USER'S PROGRAM LIBRARY

8-Bit programs for 8008, 8080, 8085, and 8048 processors

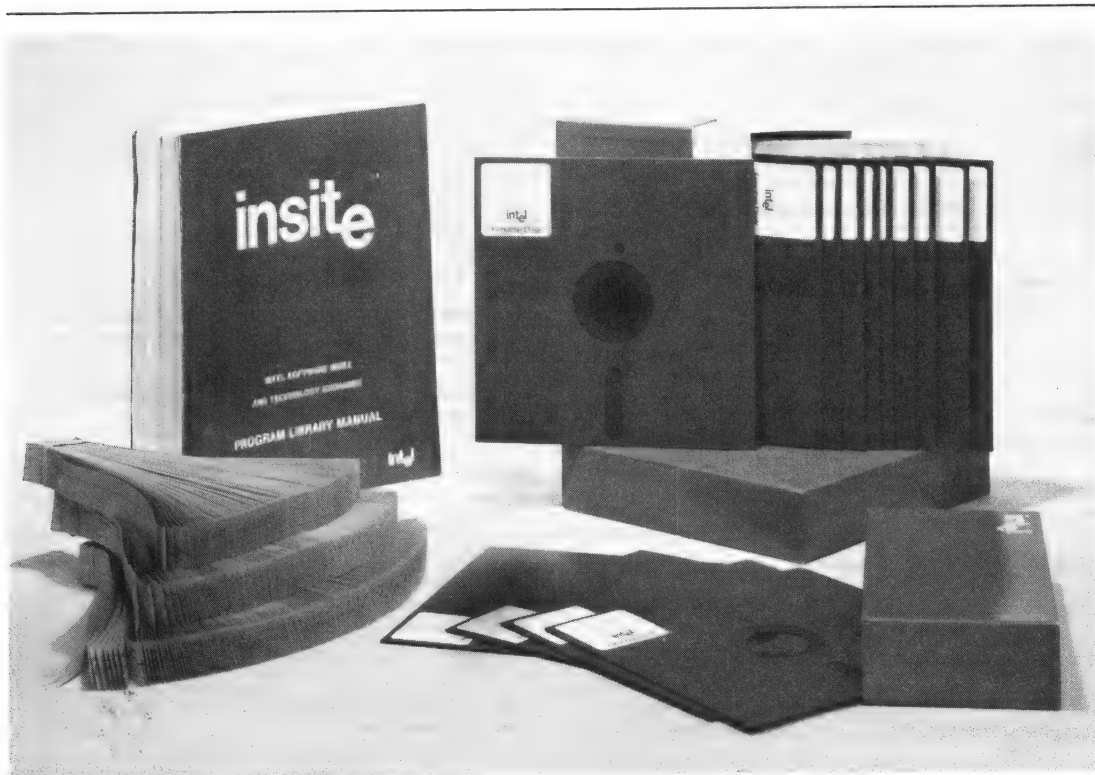
Bi-monthly updates of new programs provided for library members

Hundreds of programs provided for member use

Diskette, paper tapes, and listings available for library programs

Bonuses provided for program contributions

Insite, Intel's Software Index and Technology Exchange, is a collection of programs, subroutines, procedures, and macros written by users of Intel's 8008, 8080, 8085, and 8048 microcomputers, iSBC 80 OEM computer systems, and Inteltec development systems. Thanks to customer contributions to Insite, Intel is able to make these programs available to all users of Intel microcomputers. By taking advantage of the availability of these general purpose routines, the microcomputer design engineer and programmer may save many hours of programming and debugging time. The library of programs also serves as a good learning tool for those unfamiliar with either Intel assembly language or FORTRAN-80 and PL/M-80, Intel's high-level languages for the 8008, 8080, and 8085 microcomputers. For each accepted program submittal, Insite provides contributors with either a one year free membership, five free paper tapes, or a free program diskette.



USER'S
LIBRARY

LIBRARY DESCRIPTION

Insite Program Library Manual

Each member is sent the program library manual, a collection of source listings of library programs four pages and under. Longer programs are represented by abstracts indicating the function of the routine, the required hardware and software, and the memory requirements for each program. User's library members receive regular updates of new programs submitted to Insite during each subscription period. The yearly subscription fee is listed in the Intel OEM Price List.

Program Library Services

Paper Tapes and Listings — Available for programs in Insite. A handling fee is charged for each paper tape and listing. Ordering information may be found in the program library manual.

Diskette — Most user's library program sources are available on system diskettes. A three program minimum is required on all diskette orders, with the exception of Section 9 and other specially priced programs. Both single and double density versions are available.

Membership

Membership in Insite is available on an annual basis. Users may become members either by contributing programs or by submitting the membership fee. The membership form shown in Figure 1 may be used for new member registration.

PROGRAM SUBMITTAL

Requirements

Programs submitted for Intel review must follow the guidelines listed below:

Language — Programs must be written in a standard Intel assembly language or PL/M. These languages are documented in the following manuals:

98-019B — 8008/MCS-8 Assembly Programming Manual

9800301C — 8080/8085 Assembly Language Programming Manual

98-255C — MCS-48 and UPI-41 Assembly Language Manual

98-268B — PL/M 80 Programming Manual

9800481A — FORTRAN-80 Programming Manual

Source Listings — A source listing of the program must be included. This must be the output listing of a compile or assembly. All accepted programs should assemble or compile correctly with no syntax errors. No consideration will be given to partial programs or duplication of existing programs.

Test Program — A test program must be included showing the correct operation of the program to assure the validity of the contributed program.

Source Master — A source paper tape or diskette of the contributed program is required as a master for use in reproducing tapes for other members.

Submittal Form

The submittal form may be completed as follows (please type or print):

Processor — check appropriate box.

Program Title — give name and brief description of program function.

Function — give detailed description of operations performed by the program. Attach additional pages if necessary.

Required Hardware — provide descriptive names.
Example:

TTY or port 0 and 1
Interrupt circuitry
I/O interface
Machine line and configuration for cross products.

Required Software — provide descriptive names.
Example:

TTY driver
Floating point package
Support software required for cross products.

Input Parameters — give description of register values, memory areas, or values accepted from input ports.

Output Results — give values to be expected in registers, memory areas, or on output ports.

Program Details — give for resident products only:

- (1) Register modified
- (2) RAM required (bytes)
- (3) ROM required (bytes)
- (4) Maximum subroutine nesting level

Assembler/compiler used — provide descriptive names.
Example:

PL/M
Intellex MDS Macroassembler
IBM 370 Fortran IV

Programmer Company and Address

USER'S LIBRARY PARTIAL PROGRAM INDEXES

The Intel Insite User's Library contains and provides

hundreds of programs for member use. Partial indexes for the Insite User's Library are presented in the following table.

8-Byte Positive Fractional Multiply
8-Byte Multiply and Divide
8-Bit Random Number Generator
12 x 12 Multiply
16-Bit 2's Complement Signed Multiplication
16-Bit CRC for Polynomial $X^{16} + X^5 + 1$
16-Bit Division — 16-Bit Result
16-Bit Division — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 32-Bit Result
16-Bit Random Number Generator
16-Bit Square Root Routine
32-Bit Binary to BCD Conversion, Leading Zero Blanking
32-Bit Divide Subroutine
2708 PROM Programmer for Intellex 8/80 80
4040 Cross Assembler for Intellex 8/80 80 and MDS-800
8008 Cross Inverse Assembler for HP 2100
8008 Disassembler
8008 MACRO Definition Set for Assembly on PDP-11
8008 MACRO Assembler Version 2.0
8080 MACRO Assembler 4.1
8080 CPU Exercise Routine
8080 Cross Assembler for Tektronics 4051
8080 Double Precision ARC Tangent
8080 Disassembler
8080 Floating Point Extended Math Package
8080 Floating Point Package with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
8080 RAM Memory Test
8080 Symbol Table Dump
9600 Initialize CRT and Uart for Baud

ADCCP Remainder Routine
A/D Converter Routine
Adaptive Game Program
Algebraic Compare Subroutine
APL Graphic Display on a 5 x 7 Dot Matrix
Approximating Routine
Arctan 2 Subroutine
ASCII Display
Absorbance Calculation
ASCII to EBCDIC and EBCDIC to ASCII Converters
Assembler Oriented Centronics 306 Line Printer Handler and Error Only Assembler

Bandit Static Display
Banner Print and Punch
BASIC CPU State Vector Maintenance
Basic Digital Panel Meter Call
BASIC Interpreter
BASIC/M Translator and Interpreter
BCD to BIN Conversion Routine
BCD to/from Binary Conversion
BCD Input and Direct Conversion to Binary Routine
BCD Multiplication
BCD Sum for 8008
BCD Up/Down Counter

BIN to BCD Conversion Routine
Binary to BCD Subroutine
Binary to HEX Routine
Binary Loader for MDS
Binary Multiplication — 24-Bit
Binary Search
Binary Search Routine
Binary Tape Program
BINDEC BIN — Binary to/from BCD
BINLB — 8080 System Loader
Blackjack
BLPT
BOOT — Bootstrap Loading and Program Patching

Calendar Subroutine
Character Interpreted Memory Dump
Clock Subroutine
Compare
Compare Object Code Tape with Memory
Control Data Output
Conversion of Scientific to Easily Readable Notation
CRECH — Cyclic Redundancy Check
Cross Assembler ASMO8
Cross Assembler for PDP-11
Cross Assembler for PDP-11
Cross Assembler for NOVA 1200
Cross Assembler for Nova 1220, IBM 360/40 and CDC 3000
Cross Assembler for Varian Data Machine
Cross Reference for PAS80 PASCAL Programs — XREF80
CRTBZ — GET
Cyclic Redundancy Character Generator
Cyclic Redundancy Check
Cyclic Redundancy Check for Data String of 2¹⁶ Bytes

Data Array Move
Data General to Intellex MDS Diskette Transport Package
Data I/O PROM Processor
'DATCON B1' Analog to Digital Conversion Program
Decrement H and L Registers
Delete Comments
Diagnostic 1003 — Memory Validity Check
Digital to Analog Conversion for Eight Outputs
Disable Hold — Screen Mode
Disassembler
Disk Dump Routine for ICOM F DOS-11/MOD 80 Floppy DOS
Double Precision Integer Arithmetic Package
Double Precision Multiply
Driver for Tektronix 4010 Graphic Screen

Elementary Function Package
Enable Hold — Screen Mode
ERLIST
Examin

Factorial of a Decimal Number
Fast Floating Point Square Root Routine
Fixed and Floating Point Arithmetic Routines

Fixed Point CHEBYSHEV Sine and Cosine for PL/M Users
Flag Processing Routine
Floating Point Decimal and HEX Format Conversion
Floating Point Format Conversion Package
Floating Point Interpreter
Floating Point Math Package
Floating Point Package for Intel 8008 and 8080 Microprocessors
Floating Point Procedures
Floating Point Square Root
Fly Reader Driver
Format
Format Intel Data

Gambol
Game of Life
Generalized Stepper Motor Drive Program
GLANCE
Gray to Binary Conversion

Handler for Tally PTP
HEX Convert — Convert Intel HEX to Prolog HEX File Converter
HEX to Decimal Conversion
HEX Format Paper Tape Dump for SDK
HEX Tape Loader for SDK
High Speed Paper Tape Reader with Stepper Motor Control
Histogram

IBM Selectric Output Program
ICE-80 Disassembler
I-Command — Insert Data in HEX Form from TTY into RAM
Input/Output Commands for MDS
Intellex 8/80 80 Monitor
Intellex 8/80 — Silent 700 Interface
Intellex MDS Diagnostic Confidence Test Version 1.0
Intellex MDS Monitor Version 2.0
Intellex 8 Text Editor
Interfacing the MDS and HP 2644
Interrupt Driven Clock Routine
Interrupt Handler (Re-Entrant)
Interrupt Service Routine
INVERT Data in RAM
I/O Routine for TI Silent 700 Terminal
I/O Simulation MACROS

Julian Data Routine

K. Program Trap and Dump Routine
Kalah
Keyboard Scanner
Kill the Rotating Bit

Leer
Legible Paper Tape
Lewthwaite's Game
List
List SCR
List Device Program
List 1 — High Speed List Program for Intellex 8

List/Print/Type "List SRC" on Diskette
LOAD
Log Base 2
LSORT

MACRO Assembler for DG NOVA
Main Routine DDUMP (Diskette DUMP
Routines)
Mastermind
Match
Match Game
Maze
Maze
MBCD N1 x N2 Bytes Decimal Multiply
Subroutine

Memory Compare
Memory Diagnostic Program
Memory Dump
Memory Test for the 8080
Memory Test Program
Model 101 Centronics Printer Handler
Mon256 — 256-Byte PROM Monitor
Morse Code Generator
MUL/DIV Multi-Precision Pack for 8080

Natural Logarithm
N-Byte Binary Multiplication and Leading
Zero Blanking
Nim
Nim
Non-Encoded Key Board Subroutine
Nova Cross Assembler — Intel 8080
Numbers

Octal Code Conversion for PDP-11
Octal Debugging Program (ODT) for the
MCS-80 Computer
Octal PROM Programming
OCTHEX
ONLINE, UPLOAD, DOWNLOAD
P2708 PROM Programming Routine
Page Break for Tektronix 4010 I/O Graphics
Terminal
Page Listing Program
Paper Tape Reformatter for SDK

Paper Tape Leader I.D.
Pascal
Pass — Parameter Passing Routine
PDP-11 Binary File to Intel HEX File Con-
verter
PDP-11 Program Load to HEX, Dump &
Verify
PL/M 80 Pass 3
PL/M Floating Point Interface
PL/M Histogram Procedure and Random
Number Generator
PROM Programmer for Intellec 8
Proportional Power Control Image Builder
Punch Binary Tape
Punch Test or TTY Reader/Punch Test
Quicksort Procedures

RAM Check
RAM Test Program
RANDOMSBITS
Random Number Generator — RINGEN
Read and Interrupt Modifications for Intellec
8/MOD 80
Reader Test
Read/Write Routines for Interchange Tapes
Real Time Executive
Real Time Monitor
React
RECOVER
Relative Jump Routine
RMSTF — Integration Routine
Run 0

Save/Restore CPU State on an Interrupt
SBC 80/10 Interactive Monitor
SBC 80/10 Port I/O Exerciser
SCAN
SDK-80 Keyboard Monitor
SDK-80 Paper Tape Punch Routine
Sets Horizontal Tabs on Terminet
Shellsorting Routine
Sin X, Cos X Subroutine
Slot Machine
SMAL: Symbolic Microcontroller Assembly
Language

Snap Dump 8080
Software Stack Routines for 8008
Source Paper Tape to Magnetic Cassette
SORTF — Calculates 8-Bit Root of 16-Bit
Number
Stage 2
Statement Counter
Structured Assembler for 8080
Subroutine DMULT (Decimal Multiplication)
Subroutine Log — Common Logarithms
Subroutine SORT
Symbol Table Dump for Intellec 8/MOD 80
Symbol Table List Routine

Tabs
Tally — User Tally 2200 Line Printer in
Assembly Stage of Programming
Tally R2050 HSPTR Driver
Tape Duplicator
Tape Labeler for MDS
Teleprocessing Buffer Routine
Terminal Editor
Terminet 300
Terminet 1200
Text Storage Program
Thermocouple Linearization (Type J)
Tic-Tac-Toe
Time Sharing Communications
TIMIT — Interrupt Driven Real Time Clock
Routine
T.I. Silent 700 Interface — Intellec MDS
T.I. Silent 700 — SBC 80 Monitor Interface
TRACE Version 7.0
TRACE — Program Trace and Debugger
Trace Routine
TTY Binary Dump Routine
TTY Binary Load Routine
Type
Type K.T.C. Linearizer
Utility Macros for 8080
Video Driver
Wipe
Word Game, The

Table 1. Insite User's Library Partial Program Index of 8-Bit Programs

insiteTM

USER LIBRARY MEMBERSHIP FORM

I am interest in becoming a member of Insite
Enclosed is ☐ check, ☐ money order, ☐ purchase order*, ☐ Program Submittal

NAME: _____

COMPANY: _____

SHIP TO: _____

SEND TO NEAREST LOCATION:

North America

Intel Corporation
User's Library
Microcomputer Systems
3065 Bowers Avenue
Santa Clara, California
95051

Europe

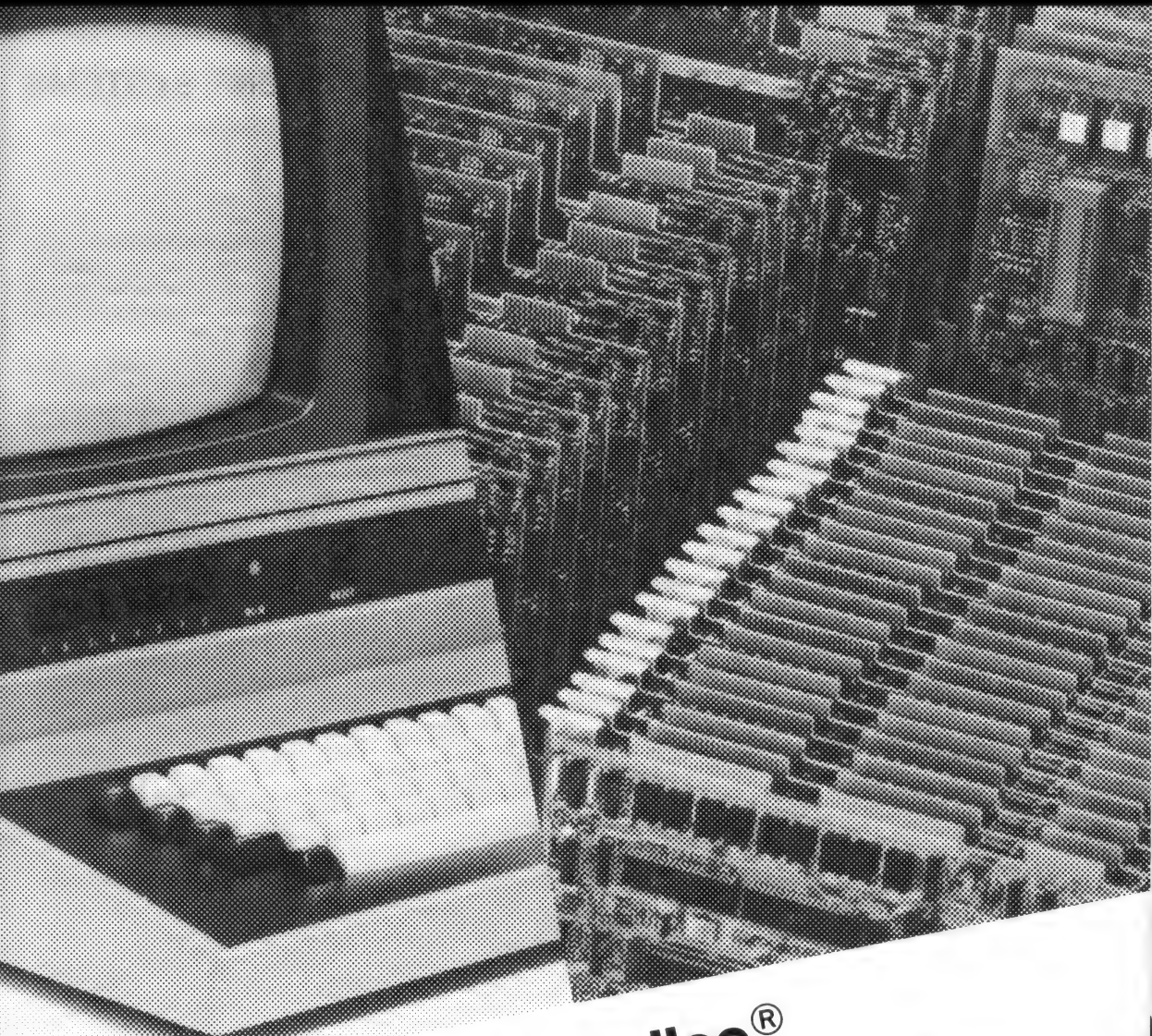
Intel International
User's Library
51 Rue du Moulin a Papier
Boite 1
B-1160 Brussels

Orient

Intel Japan K.K.
User's Library
Flowerhill Shinmachi, East Bldg
1-23-9 Shinmachi, Setagaya-ku
Tokyo 154, Japan
Ph. 03-426-9261 (PME & FSE)
03-426-9267 (CS & Fin.)

*Please refer to the OEM Price List for membership fee.

Figure 1. Insite User Library Membership Form



10 Intellec[®] Microcomputer Development Systems

**Development Systems
In-Circuit Emulators
Peripherals and Software**

INTELLEC MICROCOMPUTER DEVELOPMENT SYSTEMS

INTRODUCTION

Intel's OEM computer and development system products are supported by the most advanced system development tools available today. Foremost among these are, first, the Intellec Series II family of compatible microcomputer development systems providing a wide range of capability from a low cost ROM-based software development system to a high performance, full capability floppy-disk-based system, and second, the basic Intellec Microcomputer Development System with its complement of in-circuit emulators and advanced development software.

This section describes each system in the Series II line in detail, along with standard systems and software available for use directly on the Intellec system, including a system monitor, a resident relocatable and linkable ROM/editor/assembler, the ISIS-II diskette operating system, and other utility programs. The in-circuit emulators included here are the ICE-80 (8080), ICE-85 (MCS-85), ICE-30 (3001), ICE-41 (UPI-41), ICE-48 (MCS-48), and ICE-49 (MCS-48), all of which may be configured to support OEM computer systems and Intel microprocessors. Also included in this section is information on Intellec system peripherals and software, including technical specifications for the Intellec double density and single density diskette operating systems, which provide linkers, locators, library managers, and an Intel software library. Additional peripheral equipment includes the paper tape-based assembler, CRT keyboard display, high speed printer, high speed paper tape reader, and universal PROM programmer. Finally, both PL/M and FORTRAN-80, the high level programming language designed by Intel specifically for 8080-based systems and now resident on Intellec systems, are also described in this section along with their many features and benefits for system users.

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INTELLEC
SYSTEMS



MODEL 210 INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Low cost development system for MCS-80, MCS-85, and MCS-48 microprocessor families

Compact four-slot chassis

Single LSI electronics board with CPU, 32K bytes RAM memory, and 4K bytes ROM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for TTY, CRT, printer, high speed paper tape reader/punch and universal PROM programmer

Standard MULTIBUS with multiprocessor and DMA capabilities

ROM-based monitor, assembler, and editor

Easy upgrade to other Intellec Series II systems

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 210 Intellec Series II Microcomputer Development System is a low cost, fully supported development system providing basic hardware and software support for development of products based around Intel's MCS-80 or MCS-85 microprocessor families. Through optional software, this development capability can be extended to products based on the MCS-48 family of microprocessors. Using the user supplied system console (TTY or equivalent), the product designer may enter and correct a program source code, assemble, and begin execution, all using the Model 210 ROM-resident editor/assembler. MCS-80 and MCS-85 debugging is accomplished by means of system monitor debug commands. Completed programs may be punched to paper tape for loading into the user's system or programmed into PROM using the optional Intellec UPP-103 Universal PROM Programmer.



**INTELLEC
SYSTEMS**

FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 210 is a compact, 4-inch table-top chassis with a 4-slot cardcage, power supply, and two printed circuit cards. The CPU, interrupt, I/O, and bus interface circuitry are all fashioned from Intel's high technology LSI components and located on one PC board. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second PC board (the parallel I/O board — PIO) containing additional I/O interface logic is mounted on the rear panel. The remaining 3 slots in the cardcage are available for system expansion. A simplified block diagram of the IPB is shown in Figure 1.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics, and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

Input/Output

IBP Serial Channels — The I/O subsystem in the Model 210 consists of two parts. Two serial channels are provided directly on the IPB itself. Each channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. One channel contains current loop adapters for teletype compatibility. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as the real-time clock for the entire system. I/O activity is signaled to the system through a second 8259

interrupt controller, operating in a polled mode, nested to the primary 8259.

PIO Interface Logic — The second part of the I/O subsystem consists of the interface logic provided on the PIO board itself. Utilizing Intel's UPI-41 programmable peripheral controller, the PIO board provides device interfaces for standard Intellec peripherals, including a printer, high speed paper tape reader, high speed paper tape punch, and Universal PROM programmer. Communication between the IPB and PIO is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices specified above, as well as the two serial channels, are mounted directly on the PIO.

Control

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

MULTIBUS Capability

All Intellec Series II models implement the industry-standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microprocessor family.

Software

All standard Model 210 software is ROM-based to eliminate costly delays of loading paper tape. The capabilities of the system monitor with its "self-test" diagnostics, text editor, and MCS-80/MCS-85 or MCS-48 ROM assemblers are described on pages 10-22 to 10-25 of this catalog.

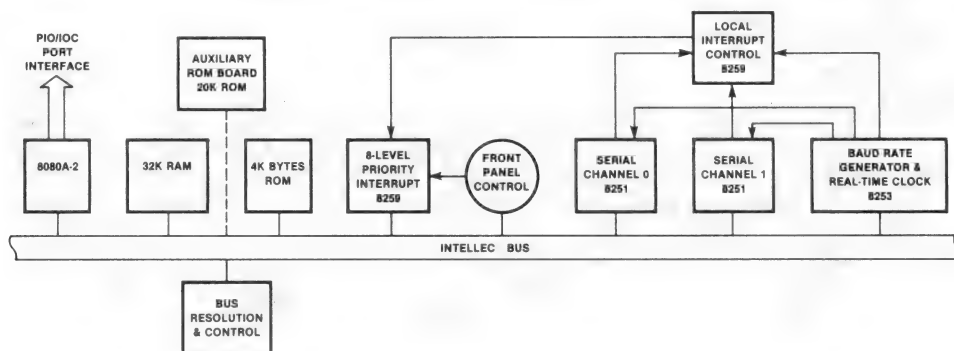


Figure 1. Simplified Integrated Processor Board (IPB) Block Diagram for the Model 210 Intellec Series II Microcomputer Development System

SPECIFICATIONS

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 32K, expandable to 64K with ISBC 032 RAM board (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic), expandable with addition of 20K auxiliary ROM board containing text editor and assembler

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

I/O Interfaces

2 serial I/O channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 4.81 in. (12.22 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 45 lb (20.5 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	24	3.5
+ 12 ± 5%	2.0	0.1
- 12 ± 5%	0.3	0.05
- 10 ± 5%	1.0	0.1

AC Requirements

50-60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0°C to 35°C (95°F)

Equipment Supplied

Model 210 chassis

Integrated processor board (IPB)

Parallel I/O board (PIO)

ROM-resident system monitor

Auxiliary ROM board with MCS-80/MCS-85 assembler and text editor

PROM programming software (paper tape)

Assembler cross reference program (paper tape)

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800557 — Inteltec Series II Model 210 User's Guide (SUPPLIED)

9800555 — Inteltec Series II Hardware Interface Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800605 — Inteltec Series II System Monitor Source Listing (SUPPLIED)

9800554 — Inteltec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

INTEL
SYSTEMS

ORDERING INFORMATION

Part Number Description

MDS-210 Inteltec Series II Model 210 microcomputer development system.



MODEL 220 INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development system in one package for MCS-80, MCS-85, and MCS-48 microprocessor families

Single LSI electronics board with CPU, 32K bytes RAM memory, and 4K bytes ROM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Integral 250K-byte floppy disk with total storage capacity expandable to over 2M bytes

Powerful ISIS-II Diskette Operating System with relocating macroassembler, linker, and locator

Standard MULTIBUS with multi-processor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 220 Intellec Series II Microcomputer Development System is a complete microcomputer development system integrated into one compact package. It includes a CPU with 32K bytes of RAM memory, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard with cursor controls and upper/lower case capability, and a 250K-byte floppy diskette drive. Powerful ISIS-II Diskette Operating System software allows the Model 220 to be used quickly and efficiently for assembling and debugging programs for Intel's MCS-80, MCS-85, or MCS-48 microprocessor families without the need for paper tape handling. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 220 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



Intel, Intellec, INSITE, Library Manager, MCS, MEGACHASSIS, MICROAMP, PROMPT, μ SCOPE, MULTIBUS, RMX/80, UPI-41, ICE, and ISBC are trademarks of Intel Corporation.

FUNCTIONAL DESCRIPTION

Hardware Components

The Inteltec Series II Model 220 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, single floppy diskette drive, and two printed circuit cards. A separate, full ASCII keyboard is connected with a cable.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt, and bus interface circuitry, fashioned from Intel's high-technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second, slave CPU card, is responsible for all remaining I/O control, including the CRT and keyboard interface and floppy disk control. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface, thus in effect creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus, thus leaving the remaining 5 slots in the cardcage available for system expansion. A block diagram of the IOC is shown in Figure 1.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Inteltec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

Input/Output

IBP Serial Channels — The I/O subsystem in the Model 220 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or data terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interfaces for the CRT, keyboard, integral floppy disk and standard Inteltec peripherals, including a printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. This CPU controls all I/O operations, as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of ROM are used for CRT screen refresh storage and the floppy disk buffer. These do not occupy any space in Inteltec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT Display — The CRT is a 12-inch raster scan-type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip, programmable CRT controller. The master processor on

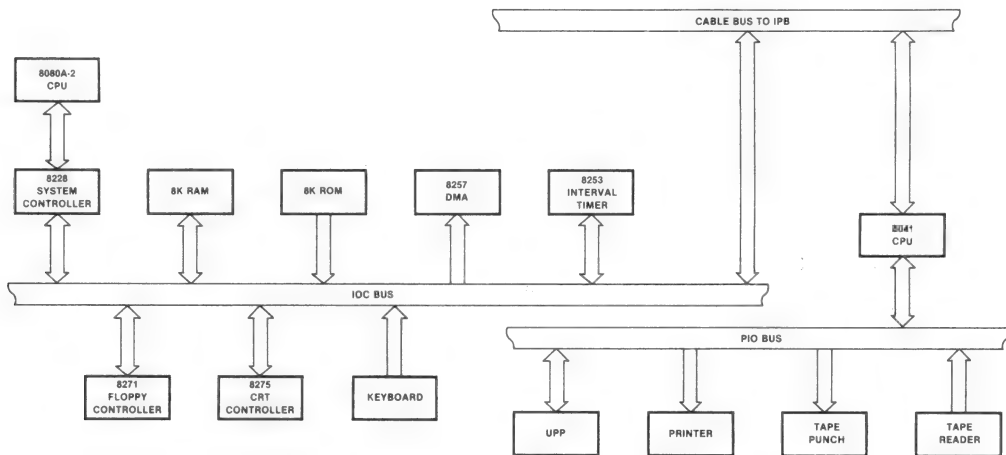


Figure 1. I/O Controller (IOC) Block Diagram for the Model 220 Inteltec Series II Microcomputer Development System

the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower-case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter-style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Floppy Disk Drive

The floppy disk drive is controlled by an Intel 8271 single chip, programmable floppy disk controller. It transfers data via an Intel 8257 DMA controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes, and reading status, all upon appropriate commands from the IOC microprocessor.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other

standard Intellec peripherals, including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate, 8-bit bidirectional data bus. Connectors for the devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

MULTIBUS Capability

All Intellec Series II models implement the industry-standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

Expansion

The Model 220 may be expanded to 64K of RAM and up to 2.25M bytes of on-line diskette storage.

SPECIFICATIONS

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 32K, expandable to 64K with ISBC 032 RAM boards (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

I/O Interfaces

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

Diskette

Diskette System Capacity — 250K bytes (formatted)

Diskette System Transfer Rate — 160K bits/sec

Diskette System Access Time

Track-to-Track: 10 ms max

Average Random Positioning: 260 ms max

Rotational Speed: 360 rpm

Average Rotational Latency: 83 ms max

Recording Mode: FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 15.81 in. (40.16 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 86 lb (39 kg)

Keyboard**Width** — 17.37 in. (44.12 cm)**Height** — 3.0 in. (7.62 cm)**Depth** — 9.0 in. (22.0 cm)**Weight** — 6 lb (3 kg)**Electrical Characteristics****DC Power Supply**

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30.0	7.5
+ 12 ± 5%	2.5	0.2
- 12 ± 5%	0.3	0.05
- 10 ± 5%	1.5	0.15
+ 15 ± 5%	1.5	1.3*
+ 24 ± 5%	1.7	1.2*

*Not available on bus.

AC Requirements

50-60 Hz. 115/230V AC

Equipment Supplied

Model 220 chassis

Integrated processor board (IPB)

I/O controller board (IOC)

CRT and keyboard

250K-byte floppy disk drive

ROM resident system monitor

ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals**9800558** — A Guide to Microcomputer Development Systems (SUPPLIED)**9800559** — Intellec Series II Installation and Service Manual (SUPPLIED)**9800306** — ISIS-II System User's Guide (SUPPLIED)**9800556** — Intellec Series II Hardware Reference Manual (SUPPLIED)**9800555** — Intellec Series II Hardware Interface Manual (SUPPLIED)**9800301** — 8080/8085 Assembly Language Programming Manual (SUPPLIED)**9800605** — Intellec Series II System Monitor Source Listing (SUPPLIED)**9800554** — Intellec Series II Schematic Drawing (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION**Part Number Description**

MDS-220 Intellec Series II Model 220 microcomputer development system (110V/60 Hz)

MDS-221 Intellec Series II Model 220 microcomputer development system (220V/50 Hz)



MODEL 230 INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development center for Intel MCS-80, MCS-85, and MCS-48 microprocessor families

LSI electronics board with CPU, RAM, ROM, I/O, and interrupt circuitry

64K bytes RAM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Powerful ISIS-II Diskette Operating System software with relocating macroassembler, linker, and locator

1 million bytes (expandable to 2.5M bytes) of diskette storage

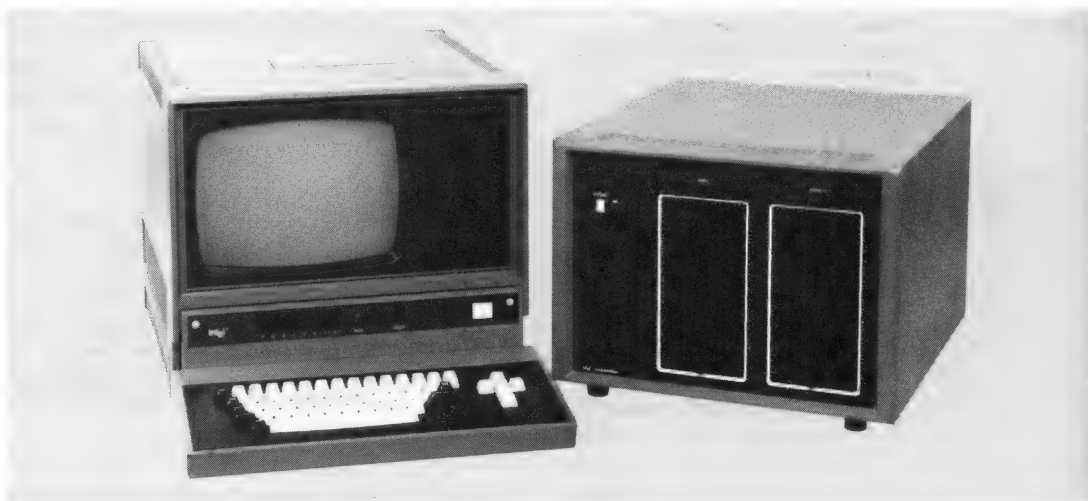
Supports PL/M and FORTRAN high level languages

Standard MULTIBUS with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 230 Intellec Series II Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, a detachable full ASCII keyboard, and dual double density diskette drives providing over 1 million bytes of on-line data storage. Powerful ISIS-II Diskette Operating System software allows the Model 230 to be used quickly and efficiently for assembling and/or compiling and debugging programs for Intel's MCS-80, MCS-85, or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations, leaving the user free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 230 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 230 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, and five printed circuit cards. A separate, full ASCII keyboard is connected with a cable. A second chassis contains two floppy disk drives capable of double-density operation along with a separate power supply, fans, and cables for connection to the main chassis. A block diagram of the Model 230 is shown in Figure 1.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry fashioned from Intel's high technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second slave CPU card is responsible for all remaining I/O control including the CRT and keyboard interface. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface logic, thus, in effect, creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU

card communicates with the IPB over an 8-bit bidirectional data bus.

Memory and Control Cards — In addition, 32K bytes of RAM (bringing the total to 64K bytes) is located on a separate card in the main cardcage. Fabricated from Intel's 16K RAMs, the board also contains all necessary address decoding and refresh logic. Two additional boards in the cardcage are used to control the two double-density floppy disk drives.

Expansion — Two remaining slots in the cardcage are available for system expansion. Additional expansion of 4 slots can be achieved through the addition of an Intellec Series II expansion chassis.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

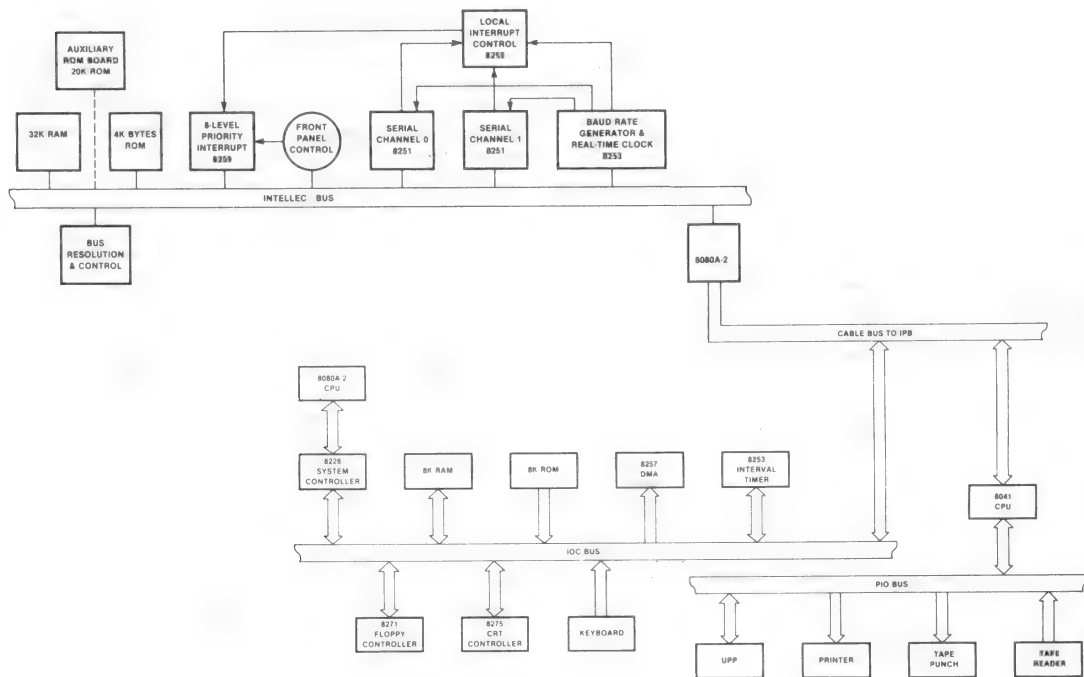


Figure 1. Intellec Series II Model 230 Microcomputer Development System Block Diagram

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 230 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interface for the CRT, keyboard, and standard Intellec peripherals including printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. The CPU controls all I/O operations as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage. These do not occupy space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT

Display — The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip programmable CRT controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals including a printer, high speed paper tape reader, high speed paper tape punch,

and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel, consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

Diskette System

The Intellec Series II double density diskette system provides direct access bulk storage, intelligent controller, and two diskette drives. Each drive provides ½ million bytes of storage with a data transfer rate of 500,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec Series II system bus, as well as supporting up to four diskette drives. The diskette system records all data in soft sector format. The diskette system is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Diskette Controller Boards — The diskette controller consists of two boards, the channel board and the interface board. These two PC boards reside in the Intellec Series II system chassis and constitute the diskette controller. The channel board receives, decodes and responds to channel commands from the 8080A-2 CPU in the Model 230. The interface board provides the diskette controller with a means of communication with the diskette drives and with the Intellec system bus. The interface board validates data during reads using a cyclic redundancy check (CRC) polynomial and generates CRC data during write operations. When the diskette controller requires access to Intellec system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intellec bus. In addition to supporting a second set of double density drives, the diskette controller may co-reside with the Intel single density controller to allow up to 2.5 million bytes of on-line storage.

MULTIBUS Capability

All Intellec Series II models implement the industry standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

SPECIFICATIONS

Host Processor (IPB)

RAM — 64K (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Diskette System Capacity (Basic Two Drives)

Unformatted

Per Disk: 6.2 megabits

Per Track: 82.0 kilobits

Formatted

Per Disk: 4.1 megabits

Per Track: 53.2 kilobits

Diskette Performance

Diskette System Transfer Rate — 500 kilobits/sec

Diskette System Access Time

Track-to-Track: 10 ms

Head Settling Time: 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm

Average Rotational Latency — 83 ms

Recording Mode — M²FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 15.81 in. (40.16 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 73 lb (33 kg)

Keyboard

Width — 17.37 in. (44.12 cm)

Height — 3.0 in. (7.62 cm)

Depth — 9.0 in. (22.86 cm)

Weight — 6 lb (3 kg)

Dual Drive Chassis

Width — 16.88 in. (42.88 cm)

Height — 12.08 in. (30.68 cm)

Depth — 19.0 in. (48.26 cm)

Weight — 64 lb (29 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30	14.25
+ 12 ± 5%	2.5	0.2
- 12 ± 5%	0.3	0.05
- 10 ± 5%	1.5	15
+ 15 ± 5%	1.5	1.3
+ 24 ± 5%	1.7	

*Not available on bus.

AC Requirements — 50/60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Model 230 chassis

Integrated processor board (IPB)

I/O controller board (IOC)

32K RAM board

CRT and keyboard

Double density floppy disk controller (2 boards)

Dual drive floppy disk chassis and cables

2 floppy disk drives (512K byte capacity each)

ROM-resident system monitor

ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800550 — Inteltec Series II Installation and Service Guide (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

9800556 — Inteltec Series II Hardware Reference Manual (SUPPLIED)

9800555 — Inteltec Series II Hardware Reference Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800292 — ISIS-II 8080/8085 Assembler Operator's Manual (SUPPLIED)

9800605 — Inteltec Series II Systems Monitor Source Listing (SUPPLIED)

9800554 — Inteltec Series II Schematic Drawings (SUPPLIED)

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INTELLEC
SYSTEMS

ORDERING INFORMATION

Part Number Description

MDS-230 Inteltec Series II Model 230 microcomputer development system (110V/60 Hz)

MDS-231 Inteltec Series II Model 230 microcomputer development system (220V/50 Hz)



EXPANSION CHASSIS INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Four expansion slots for Intellec Series II systems

Internal power supply

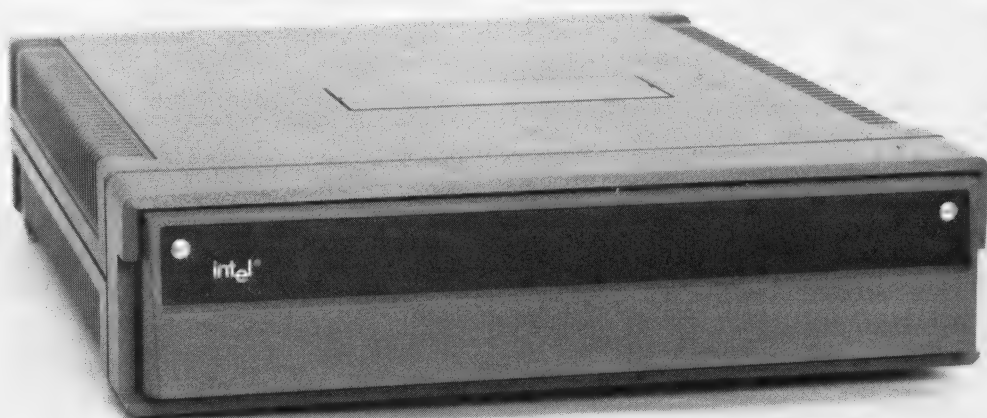
Snug fit beneath all Intellec Series II units

Cable connectable to main Intellec bus

Standard Intellec MULTIBUS with multi-processor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

The Intellec Series II Expansion Chassis provides four expansion slots for use with Intellec Series II microcomputer development systems. With its own separate power supply, the expansion chassis may be fully loaded with any boards needed to expand a user's Intellec Series II system. With the addition of the expansion chassis, Intellec Series II Models 220 and 230 contain a total of ten slots, sufficient for any configuration Intellec Series II system. The Intellec Series II Expansion Chassis is a compact chassis with a four slot cardcage, power supply, fans, and cable assemblies. It is designed to fit under any Intellec Series II system, connect directly to the system bus through an opening in the top of the chassis, and provide additional slots for the system users. The power supply is linked directly to the main chassis power supply, allowing power to flow to both chassis when the main power is turned on.



EXPANSION CHASSIS

SPECIFICATIONS

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 4.81 in. (17.22 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 42 lb. (19 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	System Requirements
+ 5±5%	24	None
+ 12±5%	2.0	None
- 12±5%	0.3	None
- 10±5%	1.0	None

AC Requirements — 50-60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Expansion chassis

Cables

Reference Manuals

9800550 — Intellec Series II Installation and Service Guide (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number

Description

MDS-201

Intellec Series II
expansion chassis



MODEL 210 ENHANCEMENT KIT INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Upgrades Model 210 system to Model 220 capability

Converts Model 210 chassis to MDS-201 expansion chassis

Includes full Model 220 capability including integral CRT and floppy disk

Eliminates the need to purchase an entire new system as development requirements increase

The Intellec Series II Microcomputer Development System Model 210 Enhancement Kit provides an easy, cost-effective way to expand the capability of a Model 210 system to the Model 220 level. The package includes a Model 220 chassis without the integrated processor board. The user simply removes the IPB from his Model 210, inserts it into his Model 220 chassis and is ready to go. The Model 210 chassis may then be used as an expansion chassis with the conversion kit provided in the upgrade package.



INTELLEC
SYSTEMS

MODEL 210 ENHANCEMENT KIT

ORDERING INFORMATION

Part Number	Description
MDS-217	Inteltec Series II Model 210 enhancement kit (110V/60 Hz)
MDS-218	Inteltec Series II Model 210 enhancement kit (220V/50 Hz)

INTELLEC
SYSTEMS



MODEL 770 PRINTER INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Provides low cost, hard copy printer for CRT-based systems

Prints original plus four copies

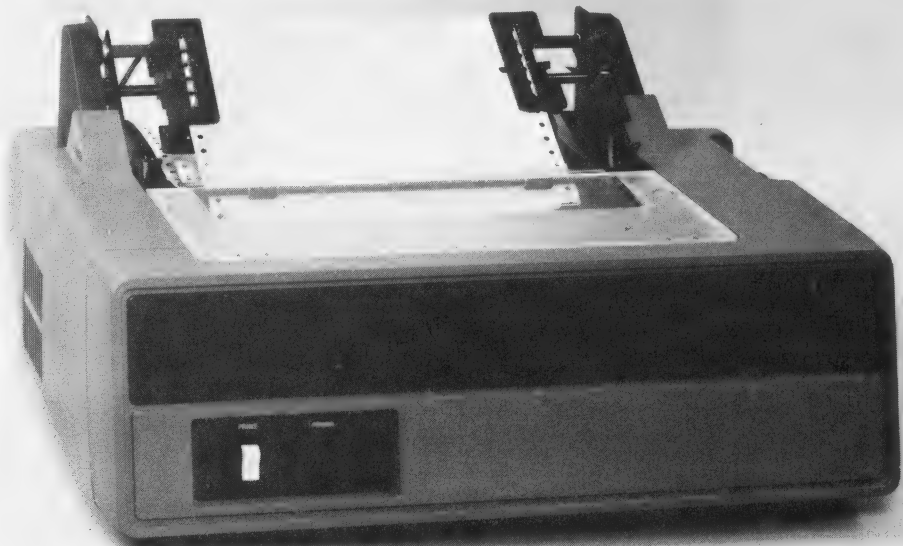
Prints 60 characters per seconds (21-90 lines per minute)

Offers 5 x 7 dot matrix character format

Provides for rear or bottom tractor feed

Provides adjustable line width from 80 to 132 columns on 8½ inch line

The Intellec Series II Microcomputer Development System Model 770 Printer is a low cost, hard copy printer designed for use with CRT-based Intellec Series II and Intellec microcomputer development systems. Unidirectional printing at 60 characters per second makes the Model 770 an ideal printer for microcomputer-based system designers with small to medium printing requirements. The 8½-inch line width may be filled with 80 to 132 characters by varying the character size. The printer uses standard fanfold paper through a tractor-feed mechanism to produce an original and up to four copies. Paper can be fed from either the bottom or the rear of the printer for versatility in any lab environment.



INTELLEC
SYSTEMS

SPECIFICATIONS

Printing Method

Impact, character-by-character printing, one line character buffer.

Printing Rate

Characters — 60 cps

Full Lines — 21 @ 80 characters/line, 90 @ 20 characters/line

Transmission Rate

Parallel — Up to 75,000 cps

Character Structure

5 × 7 dot matrix, 10 point type equivalent

Code

USASCII — 64 characters printed

Switch Controls

On-Off

Indicators

Paper Out

Format

80 to 132 characters per line, variable.

10 to 165 characters per inch, operator adjustable.

6 lines per inch.

Paper Feed

Tractor Feed — 5.5 ips slew

Paper

Standard sprocketed paper, 8½ in. to 9½ in. paper width

Number of Copies

Original plus up to four carbon copies

Physical Characteristics

Width — 24.5 in. (62.2 cm)

Height — 7.0 in. (17.8 cm)

Depth — 18.0 in. (45.7 cm)

Weight — 60 lb (27 kg)

Electrical Characteristics

50-60 Hz, 110/230V AC ± 10%

Environmental Characteristics

Temperature — Operating: -40° to 100°F (5° to 40°C),
Storage: -40° to 160°F (-40° to 50°C)

Humidity — Operating: 5% to 90% (no condensation),
Storage: 0% to 95% (no condensation)

ORDERING INFORMATION

Part Number	Description
MDS-770	60 CPS printer (110V/60 Hz)
MDS-771	60 CPS printer (220V/50 Hz)



SYSTEM MONITOR INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

ROM resident

Provides I/O interface software drivers for TTY, CRT, high speed paper tape reader, high speed paper tape punch, line/character printer, and universal PROM programmer

Expandable I/O system allows easy inclusion of user supplied device drivers

Provides bootstrap logic for all Intellec Series II systems

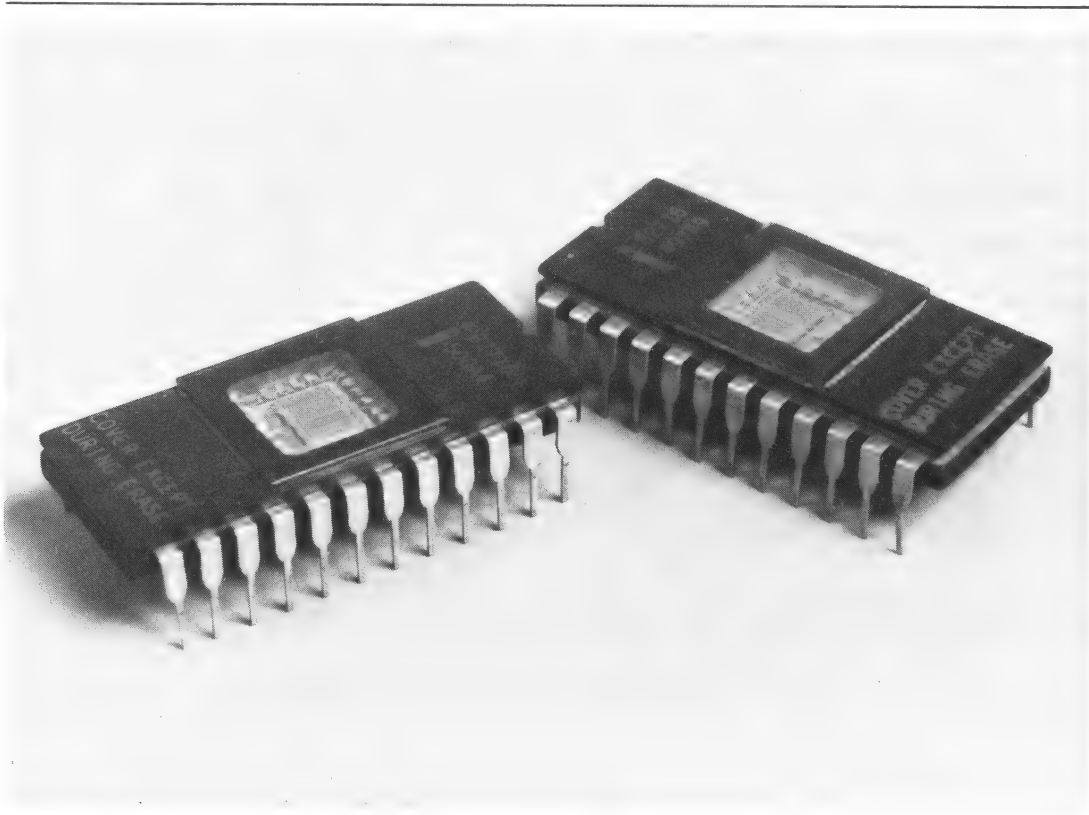
Provides self-test diagnostic capability for Intellec CPU and RAM memory

Occupies only 2K bytes of Intellec memory address space

Provides full debug capability for Intellec resident program development

Provides commands for paper tape oriented system I/O

The Intellec Series II Microcomputer Development System Monitor is an 8080A program designed to provide basic control functions for all Intellec Series II systems. These include bootstrap logic, system diagnostics, the I/O system, user interface logic for non-disk based systems, and complete debug and paper tape I/O commands.



FUNCTIONAL DESCRIPTION

Memory

The system monitor occupies 4K bytes of 8080A memory, although it only uses 2K bytes of Inteltec Series II memory space. The remaining 2K bytes of memory contain bootstrap and diagnostic code and are "shadowed" (executed only upon system reset and then disabled in favor of RAM memory present at the same locations).

Bootstrap Control

Upon system reset, the hardware enables the 2K code segment containing bootstrap and diagnostic logic, and forces a jump to the starting location. The bootstrap then determines if a diskette drive is present and ready, and transfers control either to the system monitor or ISIS-II diskette operating system. The bootstrap and diagnostic code segment is then disabled and removed from 8080A memory space.

User Commands

The monitor accepts and executes user commands. These commands include:

- read paper tape into memory
- punch memory to paper tape
- execute programs in memory with breakpoints
- display/modify memory and CPU registers
- fill memory with a constant
- hexadecimal arithmetic
- execute user diagnostics

Together these commands provide powerful program loading and debug facilities for the non-disk-based user.

Input/Output

The monitor also provides a comprehensive I/O system, including drivers for all standard Inteltec Series II devices, as well as linkage mechanism for easy inclusion of non-standard I/O devices. The monitor recognizes four logical I/O devices — a reader device, punch device, console device, and list device. Each logical device may be assigned to any one of four physical I/O devices by means of a monitor command. Device drivers are provided for each standard Inteltec peripheral selected by user command. Non-standard devices may be used by "linking" drivers through known absolute memory locations. The system is designed to operate, at a minimum, with a TTY as its sole I/O device.

ORDERING INFORMATION

Not applicable



ROM EDITOR/ASSEMBLER INTELLEC SERIES II MICROCOMPUTER DEVELOPMENT SYSTEM

Reduces or eliminates paper tape handling for Model 210 users

Editor provides powerful text entry and correction commands including string search and substitution

Available in both MCS-80/MCS-85 and MCS-48 family versions

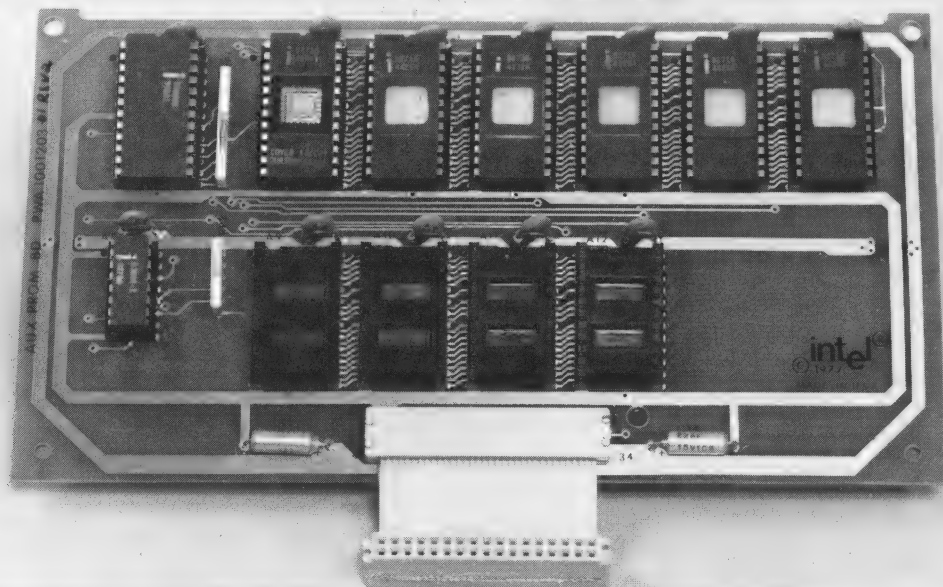
Provides total RAM-based program development capability for small programs

Assemblers accept standard Intel assembly language subset

Assemblers offer optional cross reference listing

Assemblers produce absolute code for immediate execution or PROM programming

The Intellec Series II Microcomputer Development System ROM Editor/Assembler provides a rapid, efficient means of developing software on Model 210 systems by minimizing paper tape handling. The editor and assembler may be invoked instantaneously by monitor command. Source code entered into the editor is stored in available RAM memory for easy modification. When editing is complete, the assembler will assemble directly from RAM as long as source code size, symbol table size, or object code size do not exceed available RAM storage. If they do, source code may be punched to paper tape and then re-read by the assembler. Object code produced by the assembler may be left in RAM memory for immediate execution or burned into an erasable PROM for execution in a user prototype system. An optional, paper tape-based, cross reference program is provided to list the line numbers on which each symbol is referenced. The ROM editor/assemblers are each provided on a printed circuit card designed to plug directly into the Intellec Series II's integrated processor board. Thus they do not use a slot in the system cardcage. The editor/assembler occupies 20K bytes of memory space, immediately below the monitor, starting at location B800 hexadecimal. All remaining memory space is available for RAM memory.



ORDERING INFORMATION

Part Number	Description
MDS-R48	ROM editor/assembler for MCS-80/ MCS-85 (standard with Intellec Series II Model 210). ROM editor/assembler for MCS-48 family of microprocessors



ISIS-II DISKETTE OPERATING SYSTEM MICROCOMPUTER DEVELOPMENT SYSTEM

Supports up to four double density drives and two single density drives, providing up to 2.5 megabytes of storage in one system with up to 200 files per diskette

Relocating MCS-80/MCS-85 macro-assembler contains extended macro and conditional assembly capability

Command file facility allows console commands to be submitted from diskette file

Diskette operating system functions callable from user programs

Diskette system text editor provides string search, substitution, insertions, and deletion commands

Supports resident, high level programming languages, PL/M and FORTRAN

Provides dynamic allocation and deallocation of diskette sectors for variable length files

Linker automatically combines separately assembled or compiled programs into single relocatable module

Library manager creates and updates program libraries

Supports all standard Intellec peripherals

Provides access to all Intellec monitor facilities

The ISIS-II Microcomputer Development System Diskette Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system. It provides the ability to edit, assemble, compile, link, relocate, execute, and debug programs, and performs all user file management tasks. The ISIS-II operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. Powerful system console commands are provided in an easy to use context. Monitor mode may be entered by a special prefix to any system command or program call.

INTELLEC
SYSTEMS



FUNCTIONAL DESCRIPTION

The ISIS-II operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. A diagram of the ISIS-II system program development flow is shown in Figure 1.

ISIS-II Files

A file is a user defined collection of information of variable length. ISIS-II also treats each of the standard Intellec system peripherals as files through preassignment of unique file names to each device. In this manner data may be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user chosen name unique on its diskette. Up to 200 files may be stored on each diskette.

ISIS-II System Commands

ISIS-II system commands are designed to provide the user with a powerful, easy to use program and file manipulation capability. Several commands have the capability of operating on several files at once via the wildcard file naming convention. As an example, the command DELETE *.OBJ deletes all files in the diskette directory with the suffix .OBJ. A summary of ISIS-II system commands is presented in Table 1.

Call Capability — The delete, rename, and attribute assignment commands, along with a set of file I/O routines, are callable from user written programs. This allows the user to open, close, read, and write diskette files, access standard peripheral devices, write error messages, and load other programs via simple program call statements.

Command	Operation
Initialize disk	Initializes a diskette for use by the system. Requires only one disk drive.
Attribute assignment	Assigns specified attributes to a file, such as write-protect.
Copy	Creates copies of existing diskette files or transfers files from one device to another.
Delete	Removes a file from the diskette, thereby freeing space for allocation of other files.
Directory	Lists name, size, and attributes of files from a specified diskette directory.
Rename	Allows diskette files to be renamed.
Format	Initializes a diskette for use by the system. (Use with two or more drives.)
Debug	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and or debugging.
Submit	Provides capability for executing a series of ISIS-II commands previously written to a diskette file.

Table 1. ISIS-II System Commands

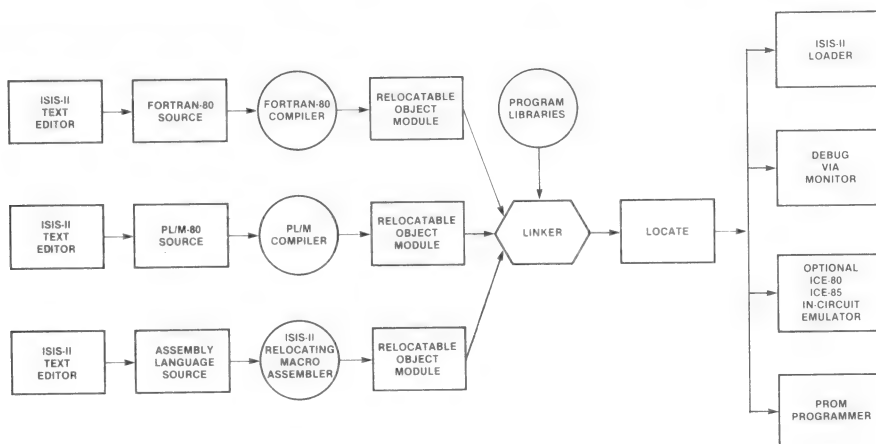


Figure 1. Program Development Flow Using ISIS-II Disk Operating System

ISIS-II Text Editor

The ISIS-II text editor is a comprehensive tool for assembly language, PL/M, and FORTRAN program entry and correction for Intel microcomputers. Its command set allows either entire lines of text or individual characters to be manipulated within a line.

Program Entry — Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

Utility Commands — To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

Storage — The contents of the workspace are stored on diskette and can be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II MCS-80/MCS-85 macroassembler.

ISIS-II MCS-80/MCS-85 Relocating Macroassembler

Address Translation — The ISIS-II MCS-80/MCS-85 macroassembler translates assembly language mnemonics into relocatable and/or absolute object code modules. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Extended macro capability eliminates the need to rewrite similar sections of code repeatedly, and thus simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code that may vary from system to system, such as the code required to handle optional external devices. Additionally, the user is allowed complete freedom in assigning the location of code, data, and stack segments.

List File — The ISIS-II Assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. A cross reference listing is also

optionally produced. The list file may then be examined from the system console or copied to a specified list device.

Object File — The relocatable object file generated by the assembler may be combined with other object programs residing on the diskette to form a single relocatable object module or it can be converted to an absolute form for subsequent loading and execution.

ISIS-II Linker

The ISIS-II linker provides the capability to combine the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module. The linker automatically resolves all external program and data references during the linking process. Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays. An optional link map showing the contents and lengths of each segment in the output module can be requested. All unsatisfied external references are also listed. If requested by the user, the ISIS-II linker can search a specified set of program libraries for routines to be included in the output module.

ISIS-II Object Locator

The ISIS-II locate program takes output from either the resident FORTRAN or PL/M compilers, the macroassembler, or the linker and transforms that output from relocatable format to an absolute format which may then be loaded via the standard ISIS-II loader, or loaded into an appropriate in-circuit emulator (ICE) module. During the locate process, code, data, and stack segments may be separately relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack are directed to RAM addresses. A locate map showing absolute addresses for each code and data segment and a symbol table dump listing symbols, attributes, and absolute address may also be requested.

ISIS-II Library Manager

The ISIS-II Library Manager program provides for the creation and maintenance of a program library containing Intel-provided and user-written programs and subroutines. These library routines may be linked to a program using the ISIS-II linker. Several libraries, each containing its own set of routines, may be created.

ORDERING INFORMATION

Part Number	Description
MDS-2DS or MDS-DDS 220	Diskette operating system



INTELLEC MICROCOMPUTER DEVELOPMENT SYSTEM

Provides modular microcomputer development system for development and implementation of MCS-48, MCS-80, MCS-85, and Series 3000 microcomputer systems

Intel 8080 microprocessor, with 2 μ s cycle time and 78 instructions, controls all Intellec functions

Supports assemblers for 8080, 8085, and 8748

16K bytes RAM memory expandable to 64K bytes

2K bytes ROM memory expandable with 6K or 16K PROM/ROM boards

Provides hardware interface and software drivers for TTY, CRT, line printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer

Eight-level nested, maskable, priority interrupt system

Provides universal bus structure with multiprocessor and DMA capabilities

ROM resident system monitor includes all necessary functions for program loading, debugging and executing

RAM resident macroassembler used to assemble all 8080 machine instructions with full macro and conditional assembly capabilities

RAM resident text editor provides powerful string search, substitution, insertion, and deletion commands

ICE (in-circuit emulator) options extend Intellec diagnostic capabilities into user configured system allowing real-time emulation of user processors

Optional PROM programmer peripheral capable of programming all Intel PROMs

Optional I/O modules expandable in groups of four 8-bit input and output ports to maximum of 88 ports (all TTL compatible)

The Intellec Microcomputer Development System is a modular microcomputer development system containing all necessary hardware and software to develop and implement Intel microcomputers and microcomputer systems. The addition of peripherals and options provides the user with a complete in-circuit microcomputer development system capability, supporting product design from program development through prototype debugging, production, and field testing.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

Hardware

The standard Intellec system consists of four micro-computer modules (CPU, 16K RAM memory, front panel control, and monitor), an interconnecting printed circuit motherboard, power supplies, fans, a chassis, and a front panel. Modular expansion capability is provided by 14 additional sockets on the motherboard. A block diagram of the Intellec system is shown in Figure 1.

8080 Microprocessor

The CPU module uses Intel's powerful NMOS 8-bit 8080 microprocessor. The 8080's 2 μ s cycle time, 78 instructions, unlimited subroutine nesting, vectored interrupt and DMA capabilities are fully utilized by the Intellec system. Bus control logic resolves bus contention conflicts between the CPU module and other modules capable of acquiring control of the bus. The CPU module interfaces with a sixteen line address bus and a bidirectional eight line data bus. 8080 status signals are decoded and utilized for memory and I/O operations. An eight-level, nested interrupt priority system, complete with an interrupt priority push-down stack, resolves contention for 8080 interrupt servicing.

Memory

The RAM memory module contains 16K bytes of Intel 2107A dynamic RAM operating at full processor speed. All necessary address decoding and refresh logic are contained on the module.

Control Functions

The front panel control module provides system initialization, priority arbitration, and real-time clock functions. System initialization routines reside in a 256-byte, PROM resident, bootstrap loader. An eight-level priority arbitration network resolves bus contention requests among potential bus masters. A 1 ms interrupt request generator, which can be disabled under program control, provides real-time clock functions. A 10 ms automatic time-out feature is also provided to force an interrupt request if nonexistent memory or I/O is addressed.

Peripheral Interface

The monitor module contains the Intellec system monitor and all Intellec peripheral interface hardware. The system monitor resides in a 2K-byte Intel 8316 ROM. The

module contains all necessary control and data transfer circuitry to interface with the standard Intellec peripherals, including a teletype, CRT, high speed paper tape reader, high speed paper tape punch, PROM programmer, and line printer.

Bus Structure

The Intellec universal bus structure enables several CPU and DMA devices to share the bus by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure contains provisions for up to 16-bit address and data transfers and is not limited to any one Intel micro-computer family.

User Interface

The Intellec front panel is intended to augment the primary user interaction medium: the system console. The simplicity of the front panel coupled with the power of the system monitor provides an efficient user/Intellec interface. The front panel contains eight interrupt request switches with corresponding indicators, CPU run and halt status indicators, a bootstrap loader switch, a reset switch, and a power on switch and indicator

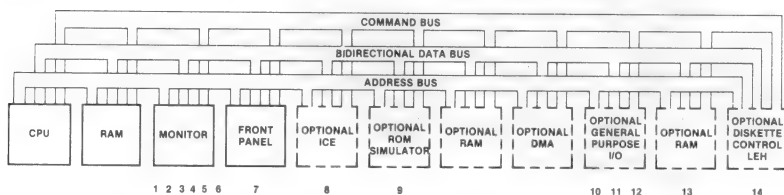
Software

Resident software provided with the Intellec includes the system monitor, the 8080 macroassembler, and the text editor. Used together, these three programs simplify program preparation and speed the debugging task.

System Monitor

The system monitor provides complete control over operation of the Intellec. It is written in 8080 assembly language, resides in 2K bytes of ROM memory, and provides all necessary functions for program loading and execution. Additional commands provide extensive debug facilities and PROM programming functions. System peripherals may be dynamically assigned either via monitor commands or with calls to the system monitor's I/O subroutines.

Commands — Programs may be loaded from the reader device in either BNPF or hexadecimal format. Utility commands aid in executing and checking out programs. Typical utility commands are shown in Table 1.



NOTES

- 1 PROM PROGRAMMER DATA STATUS COMMANDS
- 2 HIGH SPEED PUNCH DATA STATUS COMMANDS
- 3 HIGH SPEED READER DATA STATUS COMMANDS
- 4 PRINTER DATA STATUS COMMANDS
- 5 CRT DATA STATUS COMMANDS
- 6 TTY DATA STATUS COMMANDS
- 7 FRONT PANEL STATUS SWITCH INPUTS
- 8 USER SYSTEM CPU OR MCU PIN SIGNALS
- 9 USER SYSTEM ROM PIN SIGNALS
- 10 EIGHT INTERRUPT LINES
- 11 FOUR 8 BIT OUTPUT PORTS
- 12 FOUR 8 BIT INPUT PORTS
- 13 DMA DEVICE DATA STATUS COMMANDS
- 14 DISKETTE DRIVE DATA STATUS COMMANDS

Figure 1. Intellec System Block Diagram

Command	Operation
F	Initializes memory to constant.
M	Moves a block of memory to another location.
D	Displays memory.
S	Modifies RAM memory.
X(A-F)	Examines and modifies CPU registers.
G	Sets breakpoints.
G	Initiates execution at any given address.
H	Performs hexadecimal arithmetic.
X(I)	Examines and modifies interrupt mask.

Table 1. Utility Command Functions

Input/Output — The Intellec system monitor (Intellec Series II Microcomputer Development System Monitor) contains a powerful and easily expandable input/output system built around four logical device types: a console device, a reader device, a punch device, and a list device. Associated with each logical device may be any of four physical devices. The user may control the physical device assignment to each logical device with a system command.

Peripheral Interface — Drivers are provided in the system monitor for the universal PROM programmer, ASR 33 teletype, high speed paper tape reader, high speed paper tape punch, line printer, and CRT. The user may write his own drivers for other peripheral devices and easily link them to the system monitor. All system peripherals may be accessed simply by calling I/O subroutines in the system monitor. In addition, the user may dynamically reconfigure his system by monitor commands or by calling system subroutines to assign a different physical device to each logical device. The user may also determine the current system peripheral configuration, check I/O status, and determine the size of available memory.

Macroassembler

The Intellec resident macroassembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. It is written in PL/M-80, Intel's high level systems programming language and occupies 12K bytes of RAM memory, including space for over 800 symbols. The symbol table size may be expanded to a maximum of 6500 symbols by adding RAM memory. All I/O in the assembler is done by means of the system monitor, enabling the assembler to take advantage of the monitor's I/O system. The assembler is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec. Full macro capability eliminates the errors of hand translation, makes it easy to modify programs by adding or deleting instructions, eliminates the need to rewrite similar sections of one code repeatedly, and simplifies program documentation.

Functions — The assembler performs its function in three passes. The first pass builds the symbol table. The second pass produces a source listing and provides error diagnostics. The third pass produces the object code. If the punch and list devices are separate (e.g., a

high speed punch or printer is available) passes 2 and 3 may be combined into one pass.

Object Code — Object code produced by the assembler is in hexadecimal format. It may be loaded directly into the Intellec for execution and debugging or it may be converted by the system monitor to BNPF format for ROM programming.

Conditional Assembly — Conditional assembly permits the assembler to include or delete sections of variable code, such as the code required to handle optional external devices, which may vary from system to system.

Text Editor

The Intellec text editor is a comprehensive tool for entering and correcting assembly language programs for the Intel 8080 microcomputer. It is written in PL/M-80. It occupies 8K bytes of RAM memory, including over 4500 bytes of workspace. The workspace may be expanded to a maximum of 58K bytes by adding RAM memory. All I/O in the editor is done through the system monitor, enabling the editor to take advantage of the monitor's I/O system. The editor is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec. The editor's command set allows the user to manipulate either entire lines of text or individual characters within a line.

Program Entry — Programs may be entered directly from the console keyboard or from the system reader device. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

Utility commands — To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

Storage — The contents of the workspace may be listed to the system console or written to the system list or punch device for future use.

OPTIONAL FEATURES

The basic Intellec capabilities may be significantly enhanced by the addition of optional features, including in-circuit emulators, the universal PROM programmer, a diskette operating system, input/output modules, RAM/PROM memory, DMA modules, and ROM simulators.

In-Circuit Emulator

In-circuit emulators (ICE) extend Intellec diagnostic capabilities into user configured systems. The Intellec resident ICE processor operates in conjunction with the host CPU and interfaces to the user system via an external cable. The ICE processor replaces the user system processor providing real-time emulation capability. Resident memory and I/O may be substituted for equivalent

user system elements, thus allowing the hardware designer to sequentially develop his system by integrating Intellec and user system hardware. Display and debug hardware eliminate the need for specially constructed user system equivalents. Augmenting these capabilities are such powerful ICE debug functions as setting breakpoints, tracing program flow, single stepping, and examining and altering CPU registers and memory locations.

Universal PROM Programmer

The Intel UPP-103 Universal PROM Programmer is an Intellec peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, 8708, 8748, and 8755. Programming and verification operations are initiated from the Intellec system console and are controlled by programs resident in the Intellec and universal PROM programmer.

Diskette Operating System

The addition of a single or dual drive diskette operating system significantly reduces program development time. An intelligent controller, constructed around Intel's powerful Series 3000 computing elements, provides diskette interface and control. Intel's software operating system (IDOS) in conjunction with the diskette operating system hardware provides a highly efficient and easy to use method for assembling, editing, and executing programs.

Input/Output Modules

Customized user I/O requirements may be satisfied by adding I/O modules. Each I/O module contains four 8-bit

input ports (latched or unlatched), four 8-bit latched output ports (with adjustable strobe pulses), and eight system interrupt lines. All inputs and outputs are TTL compatible. Optional I/O may be expanded to a maximum of 44 input and 44 output ports.

RAM/PROM Memory

Memory may be expanded by adding RAM or PROM modules in user defined combinations. Up to 64K bytes of RAM may be added in 16K-byte increments. PROM (Intel 8702A) may be added in 256-byte increments by adding PROM modules with socket capacity for 6K bytes and populating each module with the desired number of PROMs. Maximum PROM capacity is 12K bytes. RAM/PROM memory overlap is resolved by giving PROM priority.

DMA Modules

DMA (direct memory access) modules work in conjunction with the Intellec MDS universal bus to maximize the efficiency of data transfers between MDS memory and selected I/O devices. Each module contains all the necessary control and data transfer logic to implement a complete DMA channel.

ROM Simulators

A ROM simulator composed of high speed bipolar RAM emulates Series 3000 bipolar microprogram ROM memory. Each ROM simulator module may be used in 512 x 16 or 1024 x 8 configurations.

SPECIFICATIONS

Word Size (Intel 8080 host processor)

Data — 8 bits

Instruction — 8, 16, or 24 bits

Memory Size

RAM — 16K bytes expandable to 64K bytes using optional modules.

ROM — 2K bytes expandable to 14K bytes in 256-byte increments using optional PROM modules.

PROM — 256 bytes expandable using optional 6K or 16K modules.

Total — RAM, ROM, and PROM may be combined in user defined configurations up to a maximum of 64K bytes.

Machine Cycle Time

Host Processor (Intel 8080) — 2.0 μ s

Bus Transfer Rate

Maximum bus transfer rate of 5 MHz

System Clocks

Host Processor (Intel 8080) — Crystal controlled at 2 MHz \pm 0.1%

Bus Clock — Crystal controlled at 9.8304 MHz \pm 0.1%

I/O Interfaces

CRT

Baud Rates: 110/300/600/1200/2400/4800/9600 (selectable)

Code Format: 7—12 level code (programmable)

Parity: Odd/even (programmable)

Interface: TTL/RS232C (selectable)

TTY

Baud Rate: 110

Input: 10 level or greater

Output: 11 level

Parity: Odd

Interface: 20 mA current loop

High Speed Paper Tape Reader

Transfer Rate: 200 cps

Control: 2-bit output, 1-bit input

Data: 8-bit byte

Interface: TTL

Punch

Transfer Rate: 75 cps

Control: 2-bit output, 1-bit input

Data: 8-bit byte

Interface: TTL

Printer

Transfer Rate: 165 cps
Control: 2-bit status input, 1-bit output
Data: ASCII
Interface: TTL

PROM Programmer

Control: 3 strobes for multiplexed output data
Data: 8-bit bidirectional
Interface: TTL

General Purpose I/O (Optional)

Input Ports — 8-bit TTL compatible (latched or unlatched); expandable in 4 port increments to 44 input ports

Output Ports — 8-bit TTL compatible (latched); expandable in 4 port increments to 44

Interrupts — 8 TTL compatible interrupt lines

Interrupt

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access

Standard capability on Intellec bus; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 450 ns

PROM — 1.3 μ s using Intel 8708A PROM

Software Capability

System Monitor — Devices supported include:

ASR 33 teletype
Intel high speed paper tape reader
Paper tape punch
CRT
Printer
Universal PROM programmer
4 recognized logical devices

Macroassembler — Accommodates 800 symbols in standard system; automatically expandable with additional RAM memory to 6500 symbols maximum; assembles all 78 8080 machine instructions plus 10 pseudo-operators.

Text Editor — 12K bytes of workspace in standard system; automatically expandable with additional RAM memory to 58K bytes.

Software Operational Environment

System Monitor — required hardware:

Intellec system
331 bytes RAM memory
2K bytes ROM memory
System console

Macroassembler — required hardware:

Intellec system
48K bytes RAM memory
System console
Reader device
Punch device
List device
Required software: system monitor

Text Editor — required hardware:

Intellec system
8K bytes RAM memory
System console
Reader device
Punch device
Required software: system monitor

Tape Format — Hexadecimal object format

Interface Cables/Connectors

MDS-920 — High speed punch interface cable
MDS-930 — Peripheral extension cable
MDS-940 — DMA cable
MDS-950 — General purpose I/O cable
MDS-960 — 25-pin connector pair
MDS-970 — 37-pin connector pair
MDS-980 — 60-pin motherboard auxiliary connector
MDS-985 — 86-pin motherboard main connector
MDS-990 — 100-pin connector hood

Emulators

MDS-ICE-30 — 3001 MCU In-Circuit Emulator
MDS-ICE-80 — 8080 In-Circuit Emulator
MDS-ICE-48 — MCS-48 8748 In-Circuit Emulator
MDS-ICE-85 — MCS-85 8085 In-Circuit Emulator

Peripherals

MDS-UPP — UPP-103 Universal PROM Programmer
MDS-PTR — High Speed Paper Tape Reader
MDS-DOS — Diskette Operating System

Physical Characteristics

Width — 8.5 in. (21.6 cm)
Height — 19 in. (48.3 cm)
Depth — 17 in. (43.2 cm)
Weight — 65 lb (29.5 kg)

Electrical Characteristics

DC Power Requirements

DC Power Supply (Volts)	Power Supply Current (Amps)	Basic System Current Requirements (Amps)	
		Maximum	Typical
+ 5 ± 5%	35.0	9.0	6.6
+ 12 ± 5%	3.0	0.7	0.4
- 10 ± 5%	3.0	0.2	0.2
- 12 ± 5%	0.5	—	—

AC Power Requirements

50-60 Hz; 115/230V AC; 150W

Environmental Characteristics

Operating Temperature — 0 to 55°C

Optional Equipment

MDS-016 — 16K Dynamic RAM
MDS-406 — 6K PROM (sockets and logic)
MDS-416 — 16K PROM (sockets and logic)
MDS-501 — DMA channel controller
MDS-504 — General purpose I/O module
MDS-600 — Prototype module
MDS-610 — Extender module
MDS-620 — Rack mounting kit

Equipment Supplied

Central processor module
RAM memory module
Monitor module (system I/O)
Front panel control module
Chassis with motherboard
Power supplies
Finished cabinet
Front panel
ROM resident system monitor
RAM resident macroassembler
RAM resident text editor
TTY cable
AC cord

Reference Manuals

9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)
9800292 — ISIS-II 8080/8085 Assembler Operator's Manual (SUPPLIED)
9800554 — Intellec Series II Schematic Drawings (SUPPLIED)
980065 — Intellec Series II System Monitor Source Listing (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

MDS-832 Intellec microcomputer development system



ICE-80 8080 IN-CIRCUIT EMULATOR

Connects Intellec system to user configured system via an external cable and 40-pin plug, replacing the user system 8080

Allows real-time (2 MHz) emulation of user system 8080

Shares Intellec RAM, ROM, and PROM memory and Intellec I/O facilities with user system

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates need for extraneous debugging tools residing in user system

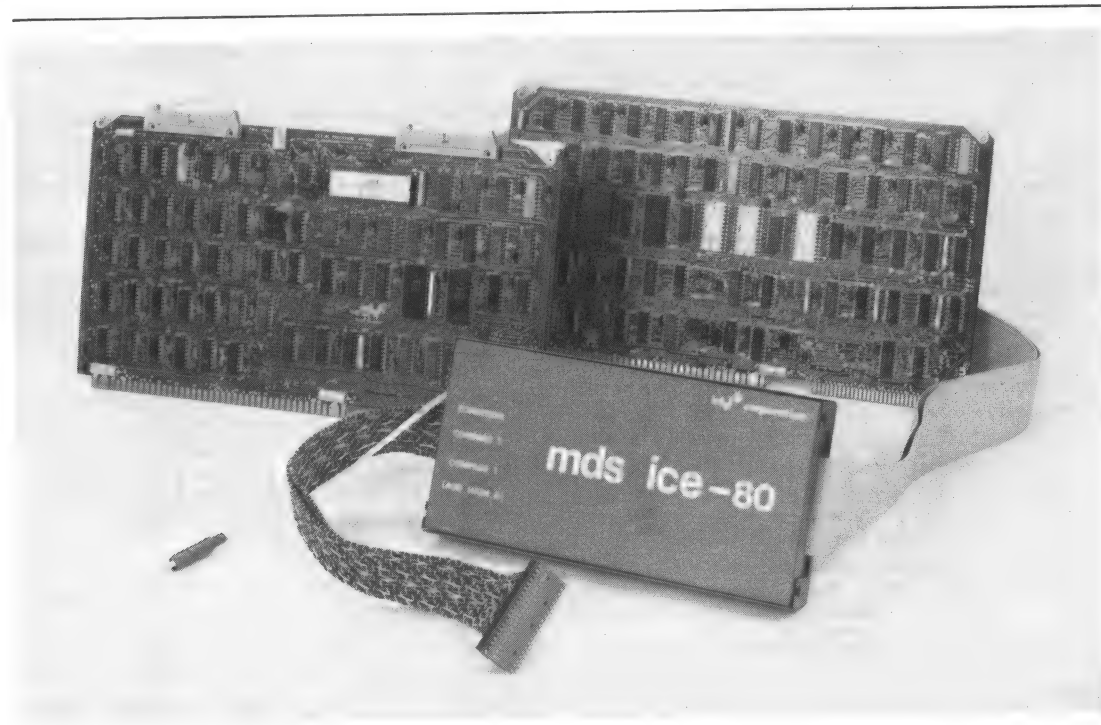
Provides address, data, and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin, and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec ICE-80 8080 In-Circuit Emulator is an Intellec resident module designed to interface with any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer may emulate the system's 8080 in real time, single step the system's program, and substitute Intellec memory and I/O for user system equivalents. Powerful Intellec debug functions are extended into the user system. For the first time the designer may examine and modify his system with symbolic references instead of absolute values.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

Integrated Hardware/Software Development

Use of the ICE-80 module enables the system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, to become a convenient two-way debug tool when begun early in the design cycle. The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. With the ICE-80 mapping capabilities, system resources may be accessed for missing prototype hardware. Hardware designs may be tested using system software to drive the final product. A functional block diagram of the ICE-80 module is shown in Figure 1.

Symbolic Debugging Capability

ICE-80 provides for user-defined symbolic references to program memory addresses and data. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is thus relieved from looking up addresses of variables or program subroutines.

Symbol Table — The user symbol table generated along with the object file during a PL/M compilation or a MAC80 or resident assembly, is loaded to memory along with the user program to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables found useful

during system debugging. By referring to symbolic memory addresses, the user may be assured of examining, changing, or breaking at the intended location.

Symbolic Reference — ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: **TIMER**, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; **ADDRESS**, the address of the last instruction emulated; **INTERRUPTENABLED**, the user 8080 interrupt mechanism status; and **UPPERLIMIT**, the highest RAM address occupied by user memory.

Debug Capability Inside User System

ICE-80 provides for user debugging of full prototype or production systems without introducing extraneous hardware or software test tools. ICE-80 connects to the user system through the socket provided for the user 8080 in the user system (See Figure 2). Intellec memory is used for the execution of the ICE-80 software, while I/O provides the user with the ability to communicate with ICE-80 and receive information on the generation of the user system. A sample ICE-80 debug session is shown in Figure 3.

I/O Mapping and Memory

Memory and I/O for the user system may be resident in the user system or "borrowed" from the Intellec system through ICE-80's mapping capability.

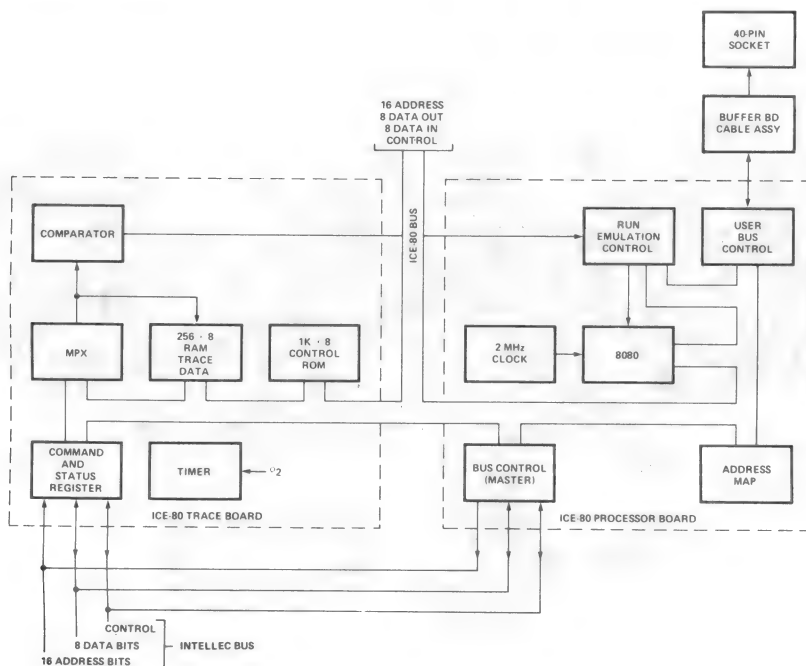


Figure 1. Functional Block Diagram of ICE-80 Module



Figure 2. ICE-80 Module Installed in User System

Memory Blocking — ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O may be defined independently. The user may assign system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, memory or I/O may be accessed in place of user system devices during prototype or production checkout.

Error Messages — The user may also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

Real-Time Trace

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition. For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

Hardware

The heart of the ICE-80 is a microcomputer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the

ICE-80 trace board. ICE-80 and the system also communicate through a control block resident in the Intellec main memory, which contains detailed configuration and status information transmitted at an emulation break. ICE-80 hardware consists of two PC boards — the processor and trace boards residing in the Intellec chassis — and a 6-foot cable interfacing to the user system. The trace and processor boards communicate with the system on the bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

Trace Board

The trace board talks to the system as a peripheral device. It receives commands to ICE-80 and returns ICE-80 responses. While ICE-80 is executing the user program, the trace board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

Breakpoint — The trace board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match to terminate an emulation. A user probe is also available for attachment to any user signal. When this signal goes true a break condition is recognized.

Interrogation — The trace board signals the processor board when a command to ICE-80 or break condition has been detected. The ICE-80 CPU then sends data stored on the trace board to the control block in memory. Snap data, along with information on 8080 registers and pin status and the reason for the emulation break, are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

Processor Board

An 8080 CPU resides on the processor board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the trace module's ROM.

Timing — The processor board contains an internal clock generator to provide clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the trace board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

On/Off Control — The processor board turns on an emulation when ICE-80 has received a run command from the system. It terminates emulation when a break condition is detected on the trace board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

Status Storage — The address map located on the processor board stores the assigned location of each user memory or I/O block. During emulation the processor board determines whether to send/receive information

ISIS 8080 MACROASSEMBLER, V1.0

PAGE 1

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;USER PROGRAM TO OUTPUT A SERIES OF
;CHARACTERS TO SDK-80 CONSOLE DEVICE
;
1320          ORG 1320H
01E3          C0 EQU 1E3H ;SDK-80 CONSOLE OUT DRIVER
;
1320 0601     START: MVI B,1 ;SET UP B VALUE
1322 3A3613    LDA DAT1 ;LOAD A WITH DAT1 VALUE
135 4F        LOOP:  MOV C,A
1326 CDE301    CALL C0 ;SEND C VALUE TO CONSOLE
1329 79        MOV A,C ;RESTORE A
132A 93        SBB B ;SUBTRACT B FROM A
132B 323713    STA RSLT ;STORE RESULT IN RSLT
132E FE40      CPI 40H ;LAST VALUE TO PRINT
1330 C22513    JNZ LOOP ;LOOP AGAIN IF A>40H
1333 C32013    JMP START ;ELSE RESTART WHOLE PROCEDURE
;
1336 5A        DAT1: DB 5AH
1337          RSLT: DS 1
0000          END

```

ISIS, V1.0 INITIAL ICE-80 SESSION
 -ICE80 (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
 ISIS ICE-80, V1.0

- ① **XFORM MEMORY 0 TO 1 U
 *XFORM IO 0FH U
- ② *LOAD PROG. HEX
 ERR = 067
 STAT = 11H TYPE = 06H CMND = 07H ADDR = 1320H GOOD = 06H BAD = 04H
 *CHANGE MEMORY 1321H = FFH
 ERR = 067
 STAT = 11H TYPE = 06H CMND = 07H ADDR = 1321H GOOD = FFH BAD = FDH
 *LOAD PROG. HEX
- ③ *GO FROM START UNTIL RSLT WRITTEN
 EMULATION BEGUN
- ④ ERR = 067
 STAT = 11H TYPE = 07H CMND = 02H
- ⑤ *DISPLAY CYCLES 5

 STAT = A2H ADDR = 1326H DATA = CDH
 STAT = 82H ADDR = 1327H DATA = E3H
 STAT = 82H ADDR = 1328H DATA = 01H
 STAT = 04H ADDR = FFFFH DATA = 13H
 STAT = 04H ADDR = FFFEH DATA = 29H
- ⑥ *CHANGE DOUBLE REGISTER SP = 13FFH
 *BASE HEX
 *EQUATE STOP = 1333H
- ⑦ *GO FROM START UNTIL STOP EXECUTED THEN DUMP
 EMULATION BEGUN
 B = 01H C = 41H D = 00H E = 00H H = 00H L = 00H F = 56H A = 40H P = 1320H * = 1333H S = 13FFH
 EMULATION TERMINATED AT 1333H
- ⑧ *EXIT
 *FFFF

Notes

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H-1FFFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).
2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H-13FFFH in the prototype system. The problem is fixed and a subsequent load succeeds.
3. A real-time emulation is begun. The program is executed from 'START' (1320H) and continues until 'RSLT' is written [in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT'].
4. An error condition results: TYPE 07, CMND 02 indicate the program accessed is a guarded area.
5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.
6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.
7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a dump of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.
8. Exit returns control to the MDS monitor.

Figure 3. Sample ICE-80 Debug Session

on the Intellec or user bus by consulting the address map. The processor board allows the ICE-80 CPU to gain access to the bus as a master to "borrow" Intellec facilities. At an emulation break, the processor board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the trace board to send stored information to a control block in Intellec memory for access during interrogation mode.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector that plugs into the user system in the socket designed for the 8080 when enabled by the processor module's user bus control logic.

Software

The ICE-80 software driver (ICE80SD) is a RAM-based program providing easy to use English language commands for defining breakpoints, initiating emulation, and interrogating and altering the user system status recorded during emulation. ICE-80 commands are con-

figured with a broad range of modifiers to provide the user with maximum flexibility in describing the operation to be performed. Listings of emulation commands, interrogation commands, and utility commands are provided in Table 1, Table 2, and Table 3, respectively.

Command	Operation
Base	Establishes mode of display for output data.
Display	Prints contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. May also be used for base-to-base conversion, or for addition or subtraction in any base.
Change	Alters contents of memory, register, output port, or 8080 flag.
XFORM	Defines memory and I/O status.
Search	Looks through memory range for specified value.

Table 2. ICE-80 Interrogation Commands

Command	Operation
Go	Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.
Step	Initiates emulation in single or multiple instruction increments. User may specify register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.
Range	Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.
Continue	Resumes real-time emulation.
Call	Emulates user system interrupt.

Table 1. ICE-80 Emulation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Equate	Enters symbol name and value to user symbol table.
Fill	Fills memory range with specified value.
Move	Moves block of memory data to another area of memory.
Timeout	Enables/disables user CPU 1/4 second wait state timeout.
List	Defines list device (diskette-based version only).
Exit	Returns program control to monitor.

Table 3. ICE-80 Utility Commands

SPECIFICATIONS

Paper Tape-Based ICE80SD Operating Environment

Required Hardware

Intellec system
System console
Reader device
Punch device
ICE-80

Required Software

System monitor

Diskette-Based ICE80SD

Operating Environment

Required Hardware

Intellec system
32K bytes RAM memory
System console
ISIS MOS floppy disk drive
ICE-80

Required Software

System monitor
ISIS-II Diskette Operating System

System Clock

Crystal controlled 2.185 MHz \pm 0.01%. May be replaced by user clock through jumper selection.

Connectors

Edge Connector — CDC VPB01E32A00A1

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Weight — 8.00 lb (3.64 kg)

Electrical Characteristics**DC Power Requirements**

V_{CC} = +5V, \pm 5%

I_{CC} = 9.81A max; 6.90A typ

V_{DD} = +12V, \pm 5%

I_{DD} = 79 mA max; 45 mA typ

V_{BB} = -9V, \pm 5%

I_{BB} = 1 mA max; 1 μ A typ

Environmental Characteristics

Operating Temperature — 0°C to 40°C

Operating Humidity — Up to 95% relative humidity without condensation

Equipment Supplied

Printed circuit modules (2)

Interface cables and buffer board

ICE-80 software driver, paper tape version

(ICE-80 software driver, diskette-based version is supplied with diskette operating systems)

Reference Manuals

9800185 — ICE-80 Operator's Manual (SUPPLIED)

9800556 — Inteltec Series II Hardware Reference Manual (SUPPLIED)

9800554 — Inteltec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION**Part Number Description**

MDS-80-ICE	8080 CPU in-circuit emulator, cable assembly and interactive software included
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ICE-85 MCS-85 IN-CIRCUIT EMULATOR

Connects the Intellec system resources to the user configured system via a 40-pin adaptor plug

Executes user system software in real time

Shares Intellec memory and I/O facilities with user system

Provides 1023 states of 8085 trace data plus 18 additional logic signals via external trace module

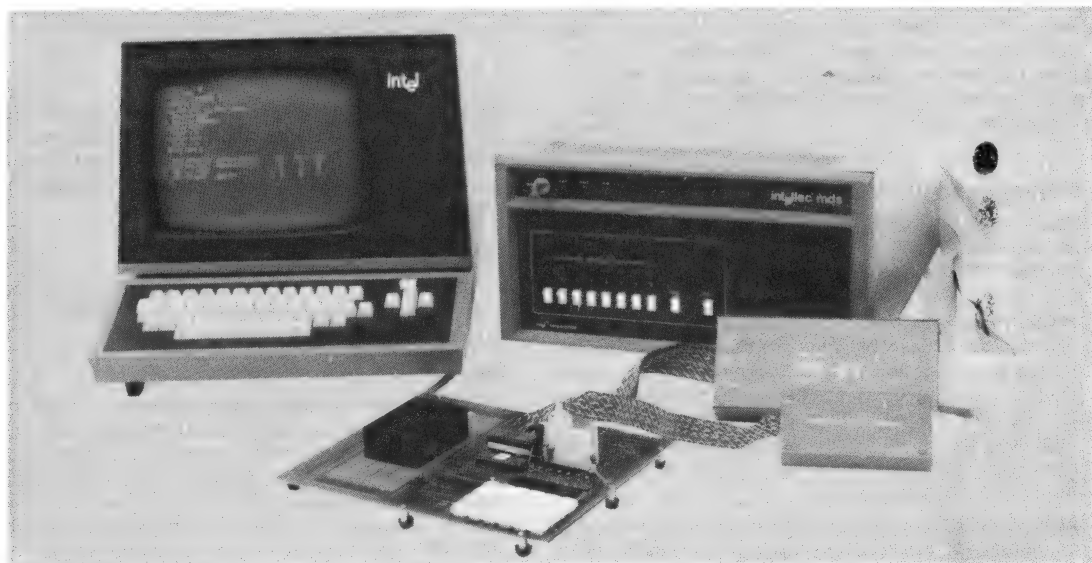
Offers full symbolic debugging capability for both assembly language and Intel's high level compiler language, PL/M-80

Displays trace data from user's 8085 in assembler mnemonics and allows personality groupings of data sampled by external 18-channel trace module

Extends ICE capabilities to prototype system peripheral circuitry by allowing user to execute peripheral chip analysis routines

Provides ability to examine and alter MCS-85 registers, memory, flag values, interrupt bits, and I/O ports

The ICE-85 MCS-85 In-Circuit Emulator is an Intellec resident module designed to interface with any user configured 8085 system. In addition, an external trace module provides access to user system peripheral circuitry via a user configured DIP clip for peripheral ICs or may be attached to as many as 18 separate prototype signal nodes via individual probe clips. Using the ICE-85 module, the designer may execute prototype software in real time or single step mode and may substitute Intellec system memory and I/O for their user system equivalents. ICE capability may be extended to the remaining user system peripheral circuitry by allowing the user to create and execute a library of user defined peripheral chip analyzer routines. All user access to the prototype system software may be done symbolically by assigning names to program locations and data, I/O ports, and groups of external trace signals. For the first time, in-circuit emulation extends beyond a user prototype CPU to the entire user system, allowing in-system emulation.



FUNCTIONAL DESCRIPTION

Symbolic Debugging Capability

ICE-85 provides for symbolic references to I/O ports, memory addresses, and data. Symbols and PL/M statement number may be substituted for numeric values in any of the ICE-85 commands. The user is relieved from looking up addresses of variables or program subroutines.

Symbol Table — The user symbol table generated along with the object file during a PL/M-80 compilation or by the ISIS-II 8080/8085 macroassembler is loaded into the Intellec system memory along with the user program to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables found to be useful during system debugging. By referring to symbol memory addresses, the user may examine, change, or break at the intended location.

Symbolic Reference — ICE-85 provides symbolic definition of all 8085 registers, interrupt bits, and flags. The following symbolic references are also provided for user convenience: TIMER, the low-order 16 bits of a register containing the number of 2 MHz clock pulses elapsed during emulation; HTIMER, the high-order 16 bits of the timer counter; PPC, the address of the last instruction emulated; and BUFFERSIZE, the number of frames of valid trace data (between 0 and 1022).

Trace Data Display

Trace data in the 1023 x 42-channel real-time trace memory buffer is displayed in easy to read format. The user has the option of specifying trace data displays in actual 8085 assembler instruction mnemonics. The data collected from the external trace module may be grouped and symbolically named according to user specifications and displayed in the appropriate number base designation. Simple ICE-85 commands allow the user to select any portion of the 42K-bit trace buffer for immediate display.

Memory and I/O Mapping

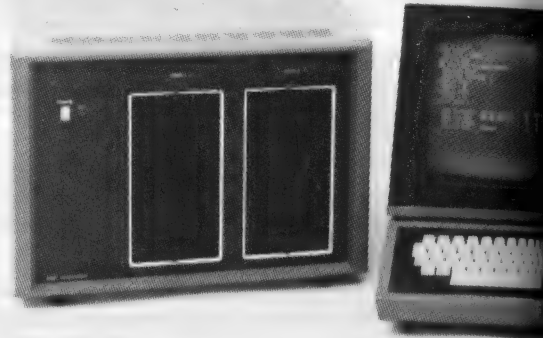
Memory and I/O for the user system may be resident in the user system or "borrowed" from the Intellec system through ICE-85's mapping capability.

Memory Blocking — ICE-85 separates user memory into 32 2K blocks. Each block of memory can be defined independently. The user may assign Intellec system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, Intellec system memory or I/O can be accessed in place of suspect user system devices during prototyping or production checkout.

Error Messages — The user may also designate a block of memory or I/O as nonexistent. ICE-85 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

Integrated Hardware/Software Development

Use of the ICE-85 module enables the system integration phase, which can be so costly when attempting to mesh completed hardware and software products, to become a convenient two-way debug tool when begun early in the design cycle. The user prototype need consist of no more than an 8085 CPU socket and a user bus to begin integration of software and hardware development efforts. With the ICE-85 mapping capabilities,



Intellec system equivalents may be accessed for missing prototype hardware. Hardware designs may be tested using the system software to drive the final product. A functional block diagram of the ICE-85 module is shown in Figure 1.

Commands

Listings of typical ICE-85 interrogation and utility commands are presented in Table 1. Typical emulation controls and commands are listed in Table 2.

Real-Time Trace

ICE-85 captures valuable trace information from the emulating CPU and the external trace module while the user is executing programs in real time. The 8085 status, the user memory or port addressed, the data read or written, and the serial lines and data from 18 external signals, is stored for the last 1023 machine states executed (511 machine cycles). This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was

user initiated or the result of an error condition. For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

External Trace Module

TTL level signals from 18 points in the user system may be synchronously sampled by the external trace module



and collected in ICE-85's trace buffer. The signals can be collected from a single peripheral chip via the supplied 40-pin DIP clip or may be placed by the user on up to 18 separate signal nodes using the supplied 18 individual probe clips. These signals are included in the 42-channel breakpoint comparisons and clock qualifiers. Also, data from these 18 channels may be displayed in each to read user defined groupings.

Synchronous Operation with Other Design Aid

ICE-85 can be synchronized with other Intellec design aids by means of two external synchronization lines. These lines are used to enable and disable ICE-85 trace data collection and to cause break conditions based on an external signal, which may not be included in the ICE-85 breakpoint registers. In addition, ICE-85 can generate signals on these lines to control other design aids.

Trace Data

ICE-85 uses two breakpoint registers to break emulation, and two trace qualifier registers to control the collection of trace data during emulation. Each register is 42 entries wide, one entry for each channel, and each entry can take any one of the three values 0, 1, or "don't care".

Trace Buffer

The trace buffer, also 42 entries wide, collects data sampled from 24 8085 processor channels and 18 external channels sampled by the external trace module. The signals collected from the 8085 include address lines, data lines, status lines, and serial input and output lines. The 18 channels extending from the external trace module synchronously sample and collect into the trace buffer any user specified TTL compatible signal from the rest of the prototype system. "Break" and "trace qualification" may therefore occur as a result of a match of any combination of up to 42 channels of CPU and external circuitry signals.

Command	Operation
Display/ Change	Display/changes the values of symbols and the constants of 8085 registers, pseudo-registers, status flags, interrupt bits, I/O ports, and memory.
Evaluate	Displays the value of an expression in binary, octal, decimal, or hexadecimal.
Search	Searches user memory between locations in a user program for specified contents.
Call (CALL)	Emulates a procedure starting at a specified memory address in user memory.
Call (ICALL)	Executes a user supplied procedure starting at a specified memory address in the Intellec system memory.
Execute	Saves emulated program registers and emulates a user supplied subroutine to access peripheral chips in the user's system.

Table 1. Typical ICE-85 Interrogation and Utility Commands

Command	Operation
Group	Defines into a symbolically named group, a channel or combination of channels from the 8085 microprocessor and/or the external trace module.
Go	Initiates real-time emulation and controls emulation break conditions.
Step	Initiates emulation in single instruction steps. User may specify the type and amount of information displayed following each step, and define conditions under which stepping should continue.
Print	Prints the user specified portion of the trace memory to the selected list device.

Table 2. Emulation Controls and Commands

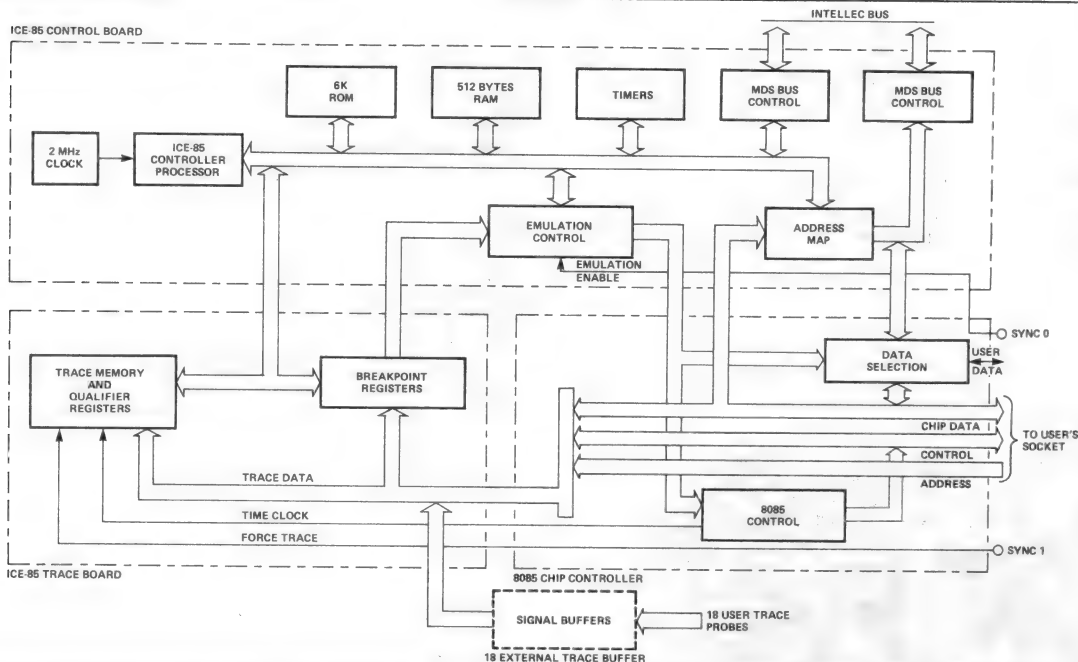


Figure 1. Functional Block Diagram of ICE-85 Module

SPECIFICATIONS

ICE-85 Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-85 module

Required Software

System monitor
ISIS-II

$I_{CC} = 12A \text{ max; } 10A \text{ typ}$
 $V_{DD} = +12V \pm 5\%$
 $I_{DD} = 80 \text{ mA max; } 60 \text{ mA typ}$
 $V_{BB} = -10V \pm 5\%$
 $I_{BB} = 30 \text{ mA max; } 10 \mu A \text{ typ}$

Environmental Characteristics

Operating Temperature — 0° to $40^\circ C$

Operating Humidity — Up to 95% relative humidity without condensation.

Emulation Clock

User's system clock or ICE-85 adaptor socket (6.144 MHz crystal)

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Packaged Weight — 6.00 lb (2.73 kg)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$

Equipment Supplied

18-channel external trace module
Printed circuit boards (2)
Interface cable and emulation buffer module
ICE-85 software, diskette-based version

Reference Manuals

9800463 — ICE-85 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

MDS-85-ICE 8085 CPU in-circuit emulator and 18-channel external trace module



ICE-30 3001 MCU IN-CIRCUIT EMULATOR

Extends Inteltec diagnostic capabilities into user configured systems, allowing in-circuit emulation of user system's 3001 MCU

Achieves direct Inteltec system connection to user configured system via external cable with 3001 compatible 40-pin connector

Provides for display of all 3001 address, status, and control lines for currently executed micro-instruction

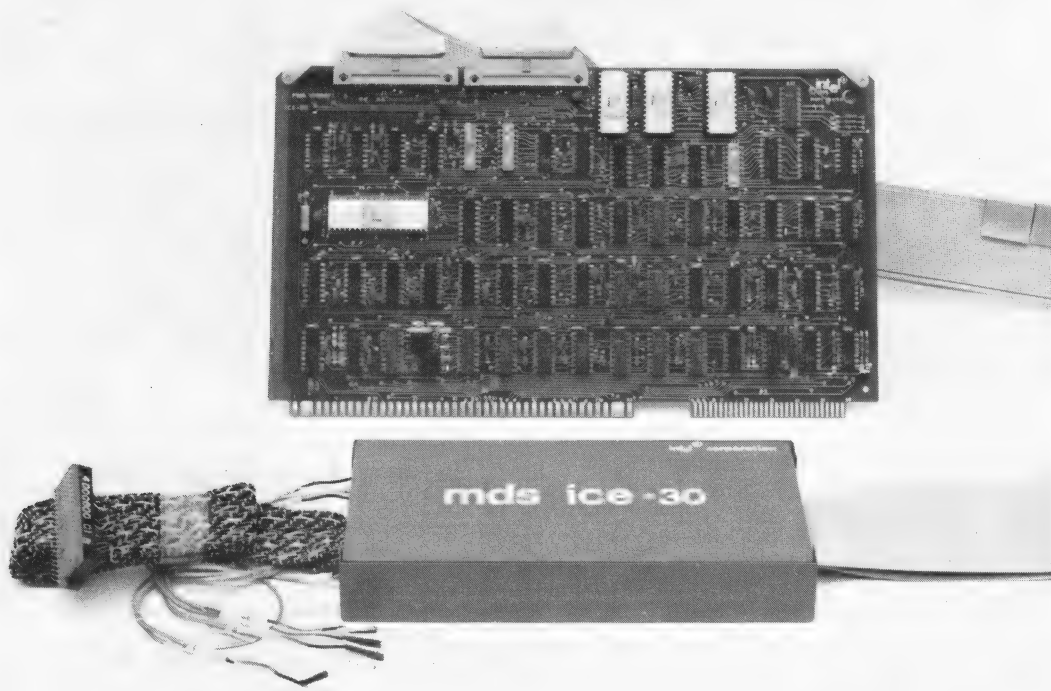
Allows for single step microprogram execution

Presets 9-bit 3001 microprogram address register and sets two independent breakpoints on micro-instruction addresses generated by 3001

Allows two independent breakpoints to be set on logical combination of any three TTL compatible signals in user system via three logic probes

Allows microprogram word contents to be displayed and modified when used with optional ROM-SIM modules

The ICE-30 3001 MCU In-Circuit Emulator is an Inteltec resident module that provides the user with direct in-circuit emulation of the 3001 microprogram control unit (MCU) and complete control over the execution of user developed microprograms. Through in-circuit emulation, the designer is able to set microprogram address breakpoints, single step microprogram execution, and monitor all of the address, status, and control lines of the 3001.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

A 3001 MCU chip in the user's system may be emulated by inserting the ICE-30 board into the Intellec bus inside a basic Intellec system. The ICE-30 board contains a 3001 MCU and peripheral logic required to monitor the 3001 operation and store trace information. The external cable carries status and control lines to and from the 3001 compatible 40-pin connector and the three logic probe lines. In addition, a MATCH line brought out on the external cable allows ICE-30 to control the user system's master clock and to perform microprogram halt and single step functions. A functional block diagram of the ICE-30 module is shown in Figure 1.

Hardware

The ICE-30 consists of a single PC board residing in an Intellec system. An external cable from the board, terminating in a 3001 compatible 40-pin connector, forms

the interface to the user system. Through the 3001 compatible connector, ICE-30 plugs directly into the user system's 3001 socket and allows the user to completely monitor and control all the activities of the MCU. The ICE-30 package hardware is shown in Figure 2.

Software

The ICE-30 software driver, ICE30SD, is an Intellec Microcomputer Development System RAM-resident program providing a user interface with the ICE-30 hardware. ICE-30 recognizes a set of commands issued by the user, translates the commands, and places the encoded results into a control block for the hardware. In this fashion, the user may establish a dialogue with the 3001 microcomputer control unit (MCU) connected to the system, thus providing the capability to monitor, control, or alter its operation. ICE-30 is capable of operating in conjunction with a RAM-based microprogram in the optional ROM-SIM modules (see ROM-SIM data

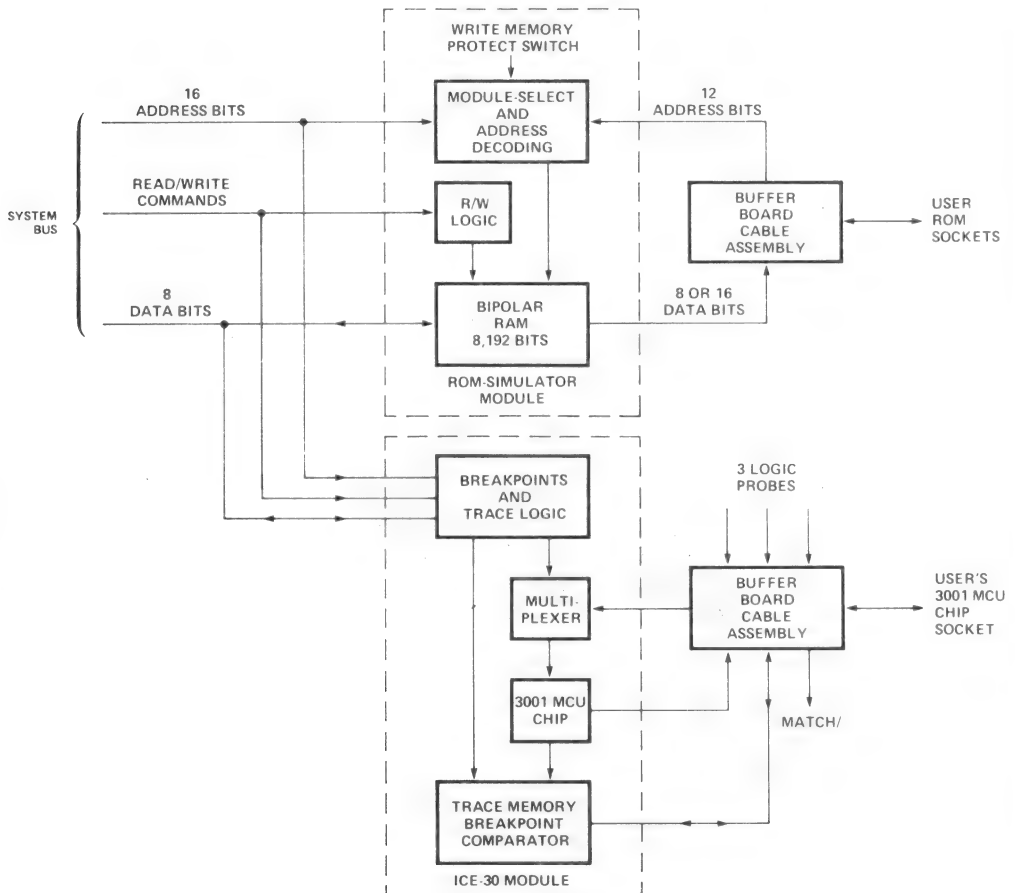


Figure 1. Functional Block Diagram of ICE-30 Module, Operating in Conjunction with ROM-Simulator Module

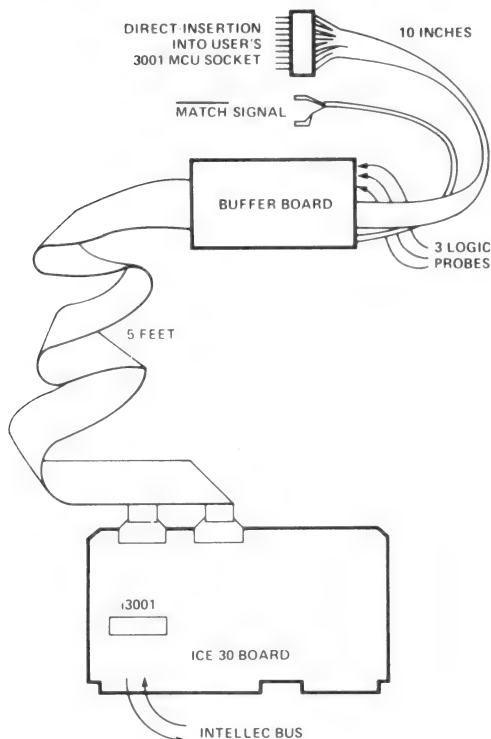


Figure 2. ICE-30 Module Hardware

sheet #98-211A). (See also Figure 1.) The commands provided by ICE30SD may therefore be divided into three categories: (1) Commands common to both ROM-SIM and ICE30SD, (2) commands supporting ICE30SD functions, and (3) commands unique to optional ROM simulator. Common commands and ICE30SD commands are represented in Table 1 and Table 2, respectively.

Command	Operation
Display	Displays contents of specified address or address range in simulated control storage.
Base	Establishes mode of display of all output data for 'display' command.
Restart	Reinitializes all program variables, except ROM-SIM configuration values, and starts execution at point following ROM-SIM configuration sequence.
Exit	Causes ICE30SD to terminate.

Table 1. Common Commands (Common to ICE-30 and Optional ROM-SIM)

Command	Operation
Set	Assigns values to both hardware breakpoint registers, 9-bit microprogram address register, and PR latch.
Go	Initiates real-time emulation, which continues until address encountered matches one of two breakpoint values.
Step	Causes execution to proceed in non-real-time single step micro-instruction mode.
Continue	Resumes step mode execution following break condition.
Enable	Activates or deactivates both hardware breakpoint registers prior to issuing 'go' command.
Trap	Sets or removes any of five-step mode software traps (software breakpoint registers).

Table 2. ICE30SD Function Commands

ROM-SIM Commands — ICE30SD provides commands necessary to drive the optional Intellec microprogram control storage simulation module, ROM-SIM. For a description of ROM-SIM capabilities, ask for the ROM-SIM Data Sheet #98-211A. ICE30SD is written in Intel's high-level programming language, PL/M, and will execute in the minimum 16K RAM Intellec configuration.

OPERATING CHARACTERISTICS

Absolute maximum characteristics for ICE-30 are shown in Table 3. DC and operating characteristics and AC characteristics are shown in Tables 4 and 5, respectively. ICE-30 timing is shown in Figure 3.

Characteristic	Rating
Temperature under bias	0°C to 45°C
Storage temperature	20°C to +75°C
All output and supply voltages	−0.5V to +7V
All input voltages	−1.0V to +5.5V
Note Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.	

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ ⁽²⁾	Max	Unit	Conditions
V _C	Input clamp voltage (All input pins)		-0.8	-1.5	V	I _C = -12 mA
I _F	Input load current: CLK input Logic probe inputs All other inputs			-2.0 -3.0 -0.4	mA mA mA	V _F = 0.45V
V _{IL}	Input low voltage			0.8	V	V _{CC} = 5.0V
V _{IH}	Input high voltage	2.0			V	V _{CC} = 5.0V
I _{CC}	Power supply current			0.0	mA	
V _{OL}	Output low voltage PR ₀ -PR ₂ All other outputs		0.35 0.35	0.45 0.45	V V	I _{OL} = 16 mA I _{OL} = 40 mA
V _{OH}	Output high voltage MA ₀ -MA ₈ , ISE, FO	2.4	3.0		V	I _{OH} = -2 mA
I _{OS}	Output short circuit current MA ₀ -MA ₈ , ISE, FO	-40		-120	mA	V _{CC} = 5.0V ⁽³⁾
I _O (OFF)	Off-state output current MA ₀ -MA ₈ , FO MA ₀ -MA ₈ , FO, PR ₀ -PR ₂			-100 100	μA μA	V _O = 0.45V V _O = 5.25V

Notes
1. T_A = 0°C to 45°C, V_{CC} = 5.0V ± 5%.
2. Typical values are for T_A = 25°C and nominal supply voltage.
3. Not more than one output should be shorted at one time

Table 4. DC and Operating Characteristics

Symbol	Parameter	Min	Typ ⁽²⁾	Max	Unit
t _{CY} ⁽³⁾	Cycle time	185	120		ns
t _{WP}	Clock pulse width	35	20		ns
t _{CS}	Clock pulse separation	150			
	Control and data input setup times:				
t _{SF}	LD, AC ₀ -AC ₆	13			ns
t _{SK}	FC ₀ , FC ₁	13			ns
t _{SX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	13			ns
t _{SI}	FI	13			ns
	Control and data input hold times:				
t _{HF}	LD, AC ₀ -AC ₆	15			ns
t _{HK}	FC ₀ , FC ₁	15			ns
t _{HX}	SX ₀ -SX ₃ , PX ₄ -PX ₇	15			ns
t _{HI}	FI	15			ns
t _{CO}	Propagation delay from clock input (CLK) to outputs (MA ₀ -MA ₈ , FO)		90	137	ns
t _{KO}	Propagation delay from control inputs FC ₂ and FC ₃ to flag out (FO)		78	130	ns
t _{FO}	Propagation delay from control inputs AC ₀ -AC ₆ to latch outputs (PR ₀ -PR ₂)		98	150	ns
t _{EO}	Propagation delay from enable inputs EN and ERA to out- puts (MA ₀ -MA ₉ , FO, PR ₀ -PR ₂)			50	ns
t _{FI}	Propagation delay from control inputs AC ₀ -AC ₆ tp interrupt strobe enable output (ISE)		86	140	ns
t _{MH}	Propagation delay from clock input (CLK) to breakpoint match (MATCH)			158	ns

Notes
1. T_A = 0°C to 45°C, V_{CC} = 5.0V ± 5%.
2. Typical values are for T_A = 25°C and nominal supply voltage.
3. t_{CY} + t_{CO} + t_{SF} + t_{WP}.
4. Pin input capacitance/output capacitance is 50 pF maximum.

Table 5. AC Characteristics

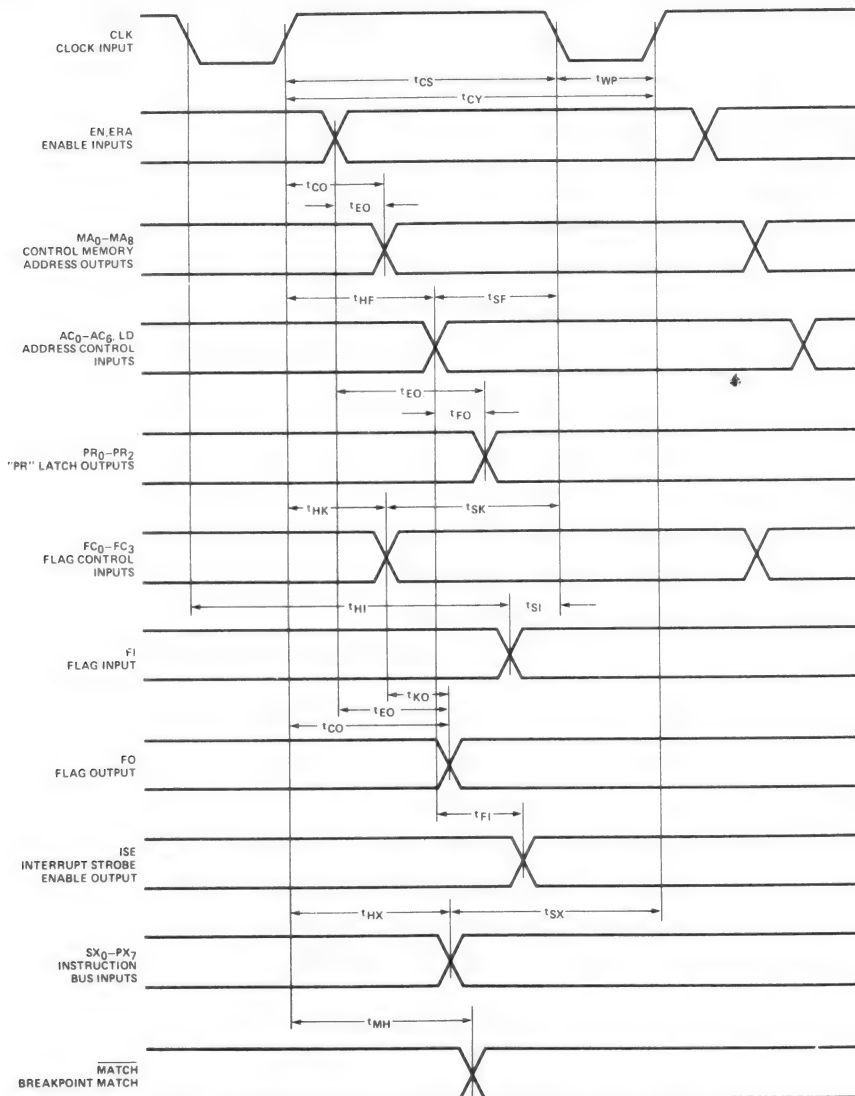


Figure 3. ICE-30 Module Timing Diagram

SPECIFICATIONS

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.50 in. (1.27 cm)

Equipment Supplied

Printed circuit board

Interface cables and buffer enclosure assembly

Software paper tape

Reference Manuals

9800220 — MDS ICE-30 Hardware Reference Manual
(SUPPLIED)

Reference manuals are shipped with each product only

if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
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MDS-30-ICE	3000 Series in-circuit emulator
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ICE-41 UPI-41 IN-CIRCUIT EMULATOR

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing user UPI-41 devices

Emulates user system UPI-41 devices in real time

Allows user configured system to use static RAM memory for program debug

Provides hardware comparators for user designated break conditions

Eliminates need for extraneous debugging tools residing in user system

Collects address, data, and UPI-41 status information on machine cycles emulated

Provides capability to examine and alter UPI-41 registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early in engineering cycle to save development time

The ICE-41 UPI-41 In-Circuit Emulator module is an Intellec system resident module that interfaces to any user configured UPI-41 system. The ICE-41 module interfaces with a UPI-41 pin-compatible plug which replaces the UPI-41 device in the system. With the ICE-41 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real time trace data. In addition, he can single step the system program during execution. Static RAM memory is available through the ICE-41 module to store UPI-41 programs. The designer may display and alter the contents of program memory, internal UPI-41 registers and flags, and I/O ports. Powerful debug capability is extended into the UPI-41 system while ICE-41 debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in the system.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

Debug Capability Inside User System

Inteltec memory is used for the execution of the ICE-41 software. The Inteltec CRT console and the file handling capabilities provide the designer with the ability to communicate with the ICE-41 module and display information on the operation of the prototype system. The ICE-41 module block diagram is shown in Figure 1.

Symbolic Debugging

Symbol Table — ICE-41 software allows the user to make symbolic references to I/O ports, memory addresses, and data in his program. The user symbol table which is generated along with the object file during a program assembly can be loaded to Inteltec memory for access during emulation. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that he may find useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location. In addition, ICE-41 provides symbolic definition of all UPI-41 registers and flags.

Symbolic Reference — Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up addresses of key locations in his program which can change with each assembly. Meaningful symbols from his source program can be used instead. For example, the command:

GO FROM .START TILL CODE. RSLT

begins execution of the program at the address referenced by the label START in the designer's assembly program. A breakpoint is set to occur the first time the microprocessor executes the program memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-41 software driver supplies them automatically from information stored in the symbol table.

Memory Replacement

The 8741 and 8041 contain internal program and data memory. When the UPI-41 microcomputer is replaced by the ICE-41 socket in a system, the ICE-41 module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-41 module has enough RAM memory available to emulate up to the total 1K control memory capability of the system.

Real-Time Trace

The ICE-41 module captures trace information while the designer is executing programs in real time. The instructions executed, program counter, port values for port 1 and port 2, and the values of selected UPI-41 status lines are stored for the last 255 instruction cycles executed. When retrieved for display, code is disassembled for user convenience. This provides data for determining how the user system was reacting prior to emulating break.

Integrated Hardware/Software Development

The user prototype systems need no more than a UPI-41 socket and timing logic to begin integration of software

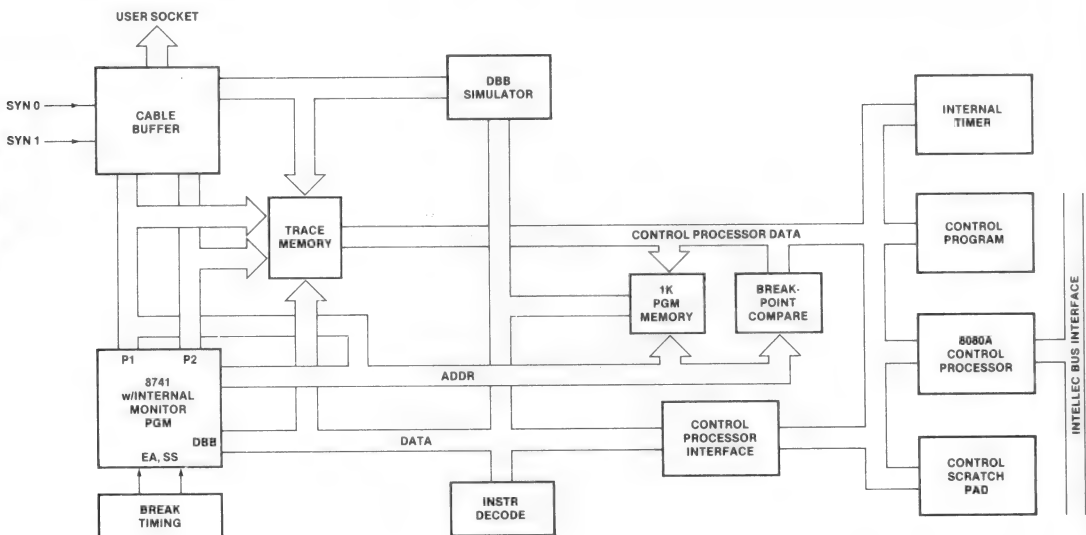


Figure 1. ICE-41 Module Block Diagram

and hardware development efforts. Through the ICE-41 module, Intellec system resources can be accessed to replace the prototype system. UPI-41 software development can proceed without the prototype hardware. Hardware designs can be tested using previously tested system software.

Hardware

The ICE-41 module is a microcomputer system utilizing Intel's UPI-41 microprocessor as its nucleus. This system communicates with the Intellec system 8080A processor via direct memory access. Host processor commands and ICE-41 status are interchanged through a DMA channel. ICE-41 hardware consists of two printed circuit boards, the controller board and the emulator board, which reside in the Intellec system chassis. A cable assembly interfaces the ICE-41 module to the user's UPI-41 system. The cable terminates in a UPI-41 pin-compatible plug which replaces any UPI-41 device in the user system.

Controller Board

The ICE-41 module interfaces to the Intellec systems as a peripheral device. The controller board receives commands from the Intellec system and responds through a DMA port. Three 10-bit hardware breakpoint registers are available which can be loaded by the user. While in emulation mode, a hardware comparator is constantly monitoring address lines for a match which will terminate an emulation. The controller board returns real-time trace data, UPI-41 registers, flag and port values, and status information to a control block in the Intellec system when emulation is terminated. This information is available to the user through the ICE-41 interrogation commands. Error conditions, when detected, are automatically displayed on the Intellec system console.

Emulator Board

The emulator board contains the 8741 and peripheral logic required to emulate the UPI-41 device in the user system. A 6 MHz clock drives the emulated UPI-41 device. This clock can be replaced with a user supplied TTL clock in the user system or can be strapped internally for 3 MHz operation.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the UPI-41 device.

Software

The ICE-41 software driver is a RAM-based program which provides the user with command language (see Table 1, Table 2, and Table 3) for defining breakpoints, initiating real-time emulation or single step operation, and interrogation and altering user system status recorded during emulation. The ICE-41 command language contains a broad range of modifiers which provide the user with maximum flexibility in defining the operation to be performed. The ICE-41 software driver is

available on diskette and operates in 32K of Intellec RAM memory.

Command	Operation
Enable	Activates breakpoint and display registers for use with go and step commands.
Go	Initiates real-time emulation and allows user to specify breakpoints and data retrieval.
Step	Initiates emulation in single instruction increments. Each step is followed by register dump. User may optionally tailor other diagnostic activity to his needs.
Interrupt	Emulates user system interrupt

Table 1. ICE-41 Emulation Commands

Command	Operation
Display	Prints contents of memory, UPI-41 device registers, I/O ports, flags, pins, real-time trace data, symbol table, or other diagnostic data on list device.
Change	Alters contents of memory, register, output port, or flag. Sets or alters breakpoints and display registers.
Base	Establishes mode of display for output data.
Suffix	Establishes mode of display for input data.

Table 2. ICE-41 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Move	Moves block of memory data to another area of memory.
Print	Prints user specified portion of trace memory to selected list device.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, octal, decimal, and hex.
Remove	Deletes symbols from symbol table.
Reset	Reinitializes ICE-41 hardware.

Table 3. ICE-41 Utility Commands

SPECIFICATIONS

ICE-41 Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-41 module

Required Software

System monitor
ISIS-II
ICE-41 diskette-based software

System Clock

Crystal controlled 6.0 MHz or 3.0 MHz internal or user supplied TTL external

Physical Characteristics

Printed Circuit Boards

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 8.00 lb (3.64 kg)

Cable Buffer Box

Width: 8.00 in. (20.32 cm)
Height: 4.00 in. (10.16 cm)
Depth: 1.25 in. (3.17 cm)
Flat Cable: 4.00 ft (121.92 cm)
User Cable: 15.00 in. (38.10 cm)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V, \pm 5\%$
 $I_{CC} = 10A \text{ max}; 8A \text{ typ}$

$V_{DD} = +12V, \pm 5\%$
 $I_{DD} = 100 \text{ mA max}; 60 \text{ mA typ}$
 $V_{BB} = -10V$
 $I_{BB} = 30 \text{ mA}$

Input Impedance

@ ICE-41 user socket pins:
 $V_{IL} = 0.8V \text{ max}; I_{IL} = 1.6 \text{ mA}$
 $V_{IH} = 2.0V \text{ min}; I_{IH} = 40 \mu A$

@ Bus:

$V_{IL} = 0.8V \text{ max}; I_{IL} = 250 \mu A$
 $V_{IH} = 2.0V \text{ min}; I_{IH} = 20 \mu A$

Output Impedance

@ P1, P2:

$V_{OL} = 0.5V \text{ max}; I_{OL} = 16 \text{ mA}$
 $V_{OH} = V_{CC} (10K \text{ pullup})$

@ Bus:

$V_{OL} = 0.5V \text{ max}; I_{OL} = 25 \text{ mA}$
 $V_{OH} = 3.65V \text{ min}; I_{OH} = 1 \text{ mA}$

Others

$V_{OL} = 0.5V \text{ max}; I_{OL} = 16 \text{ mA}$
 $V_{OH} = 2.4V \text{ max}; I_{OH} = 400 \mu A$

Equipment Supplied

Controller board
Emulator board
Interface cables and buffer module
Operator's manual
ICE-41 diskette-based software

Reference Manuals

9800465 — ICE-41 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-41-ICE	UPI-41 (8741, 8041) CPU In-circuit emulator, cable assembly and interactive diskette software included.



ICE-48 MCS-48 IN-CIRCUIT EMULATOR

Emulates 8048, 8748, 8035, and 8021 Microcomputers

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing system MCS-48 device

Emulates user system MCS-48 device in real time

Shares static RAM memory with user system for program debug

Provides hardware comparators for user designated break conditions

Eliminates need for extraneous debugging tools residing in user system

Collects bus, register, and MCS-48 status information on instructions emulated

Provides capability to examine and alter MCS-48 registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-48 MCS-48 In-Circuit Emulator module is an intellec-resident module that interfaces with any MCS-48 system. The MCS-48 family consists of the 8048, 8748, 8035, and 8021 microcomputers. The ICE-48 module interfaces with an MCS-48 system through a cable terminating in an MCS-48 pin-compatible plug which replaces the MCS-48 device in the system. With the ICE-48 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real-time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available through the ICE-48 module to emulate MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags, and I/O ports. Powerful debug capability is extended into the MCS-48 system while ICE-48 debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in this system.



INTELLEC
SYSTEMS

Memory Mapping

The 8748 and 8048 contain internal program and data memory. Both program and data memory can be expanded using external memory devices.

Internal Memory — When the MCS-48 microcomputer is replaced by the ICE-48 socket in a system, the ICE-48 module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-48 module has enough RAM memory available to emulate up to the total 4K control memory capability of the system. The ICE-48 module also provides for up to 320 bytes of data memory.

External Memory — The ICE-48 module separates replacement control memory into 16 256-byte blocks. Replacement external data memory consists of one 256-byte block. Each block of memory can be defined separately as supplied by the user system or supplied by the ICE-48 module. The user may assign ICE-48 equivalent memory to take the place of external memory not yet supplied in his system. During final debug stages when external PROM or resident 8748 is used for program execution, the designer may load the program back to ICE-48 memory to test out program changes before reassembly and reprogramming the PROM.

Symbolic Debugging

ICE-48 software provides symbolic definition of all MCS-48 registers, flags, and selected MCS-48 pins. Symbolically defined pseudo registers provide access to the sense of MCS-48 flip flops which enable time, counter, interrupt, and flag-0/flag-1 options. In addition, the user may reference locations in program and data memory, or their contents, symbolically. The user symbol table generated along with the object file during a program assembly may be loaded to Intellec memory for access during emulation. The user is encouraged to add to this symbol table any additional symbolic values for memory addresses, constants, or variables he may find useful during system debugging. Symbols may be substituted for numeric values in any of the ICE-48 commands. Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up those addresses of key locations in his program that can change with each assembly. Meaningful symbols from his source program may be used instead. For example, the command:

```
GO FROM . START TILL XDATA . RSLT WRITTEN
```

begins execution of the program at the address referenced by the label START in the designers assembly program. A breakpoint is set to occur the first time the microprocessor writes to the external data memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-48 software driver supplies them automatically from information stored in the symbol table.

Hardware

The ICE-48 module is a microcomputer system utilizing Intel's 8748 microcomputer as its nucleus. The 8748 pro-

vides the MCS-48 emulation characteristics. The ICE-48 module uses an Intel 8080 to communicate with the Intellec host processor via a DMA port. The 8080 also controls an internal ICE-48 bus for intramodule communication. ICE-48 hardware consists of two PC boards, the controller board, and the emulator board, all of which reside in the Intellec chassis. A cable interfaces the ICE-48 boards to the MCS-48 system. The cable terminates in a MCS-48 pin compatible plug which replaces any MCS-48 device in the user system. The ICE-48 module block diagram is shown in Figure 1.

Real-Time Trace

Trace Buffer

While the ICE-48 module is executing the user program, it is monitoring port, program counter, data, and status lines. Values for each instruction cycle executed are stored in a 255 x 44 real-time RAM trace buffer. A resettable timer resident on the controller board counts instruction cycles and provides timing for the trace monitor.

Controller Board

The ICE-48 module talks to the Intellec system as a peripheral device. The controller board receives commands from the Intellec system and responds through a DMA port. Three 15-bit hardware breakpoint registers are available for loading by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match to terminate an emulation. The breakpoint registers provide a signal when a match is detected. The user may disable the emulation break capability and use the signal to synchronize other debug tools. The controller board returns real-time trace data, MCS-48 register, flag, and pin values, and ICE-48 status information, to a control block in the Intellec system when emulation is terminated. This information is available to the user through the ICE-48 interrogation commands. Error conditions, when present, are automatically displayed on the Intellec system console. The controller board also contains static RAM memory, which can be used to emulate MCS-48 program and data memory in real-time. 4K of memory is available in 16,256-byte pages to emulate MCS-48 PROM or PROM program memory. A 256-byte page of data memory is available to access in place of MCS-48 external data memory. The controller board address map directs the ICE-48 module to access either replacement ICE-48 memory or actual user system external memory in 256-byte segments based on information provided by the user.

Emulator Board

The emulator board contains the 8748 and peripheral logic required to emulate the MCS-48 device in the user system. A software selectable 6 MHz or 3 MHz clock drives the emulated MCS-48 device. This clock can be disabled and replaced with a user supplied TTL clock in the user system.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the MCS-48 device.

Software

The ICE-48 software driver is a RAM-based program which provides the user with an easy to use command language (see Table 1, Table 2, and Table 3) for defining breakpoints, initiating real-time emulation or single step operation, and interrogating and altering user system status recorded during emulation. The ICE-48 command language contains a broad range of modifiers to provide the user with maximum flexibility in defining the operation to be performed. The ICE-48 software driver is available on diskette and operates in 32K of Intellec RAM memory.

Command	Operation
Enable	Activates breakpoint and display registers for use with go and step commands.
Go	Initiates real-time emulation and allows user to specify breakpoints and data retrieval.
Step	Initiates emulation in single instruction increments. Each step is followed by register dump. User may optionally tailor other diagnostic activity to his needs.
Interrupt	Emulates user system interrupt.

Table 1. ICE-48 Emulation Commands

Command	Operation
Display	Prints contents of memory, MCS-48 device registers, I/O ports, flags, pins, real-time trace data, symbol table, or other diagnostic data on list device.
Change	Alters contents of memory, register, output port, or flag. Sets or alters breakpoints and display registers.
Map	Defines memory status.
Base	Establishes mode of display for output data.
Suffix	Establishes mode of display input data.

Table 2. ICE-48 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Move	Moves block of memory data to another area of memory.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, octal, decimal, and hex.
Remove	Deletes symbols from symbol table.
Reset	Reinitializes ICE-48 program variables.

Table 3. ICE-48 Utility Commands

SPECIFICATIONS

ICE-48 Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-48 Module

Required Software

System monitor
ISIS-II

Equipment Supplied

Printed circuit boards
Interface cables and buffer module
ICE-48 software, diskette-based version

System Clock

Crystal controlled 6.0 MHz internal, 3.0 MHz internal or user supplied TTL external: software selectable.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 8.00 lb. (3.64 kg)

Electrical Characteristics

DC Power Requirements

$V_{CC} = \pm 5V \pm 5\%$
 $I_{CC} = 10A \text{ max}; 7.0A \text{ typ}$
 $V_{DD} = +12V \pm 5\%$
 $I_{DD} = 79 \text{ mA max}; 45 \text{ mA typ}$
 $V_{BB} = -10V$
 $I_{BB} = 20 \text{ mA}$

Input Impedance — @ ICE-48 user socket pins:

$V_{IL} = 0.8V \text{ (max)}, I_{IL} = 1.6 \text{ mA}$,
 $V_{IH} = 2.0V \text{ (min)}, I_{IH} = 40 \mu A$

For Bus:

$V_{IL} = 0.8V \text{ (max)}, I_{IL} = 250 \mu A$
 $V_{IH} = 2.0V \text{ (max)}, I_{IH} = 20 \mu A$

Output Impedance — @ ICE-48 user socket pins:

P1, P2:

$V_{OL} = 0.5V \text{ (max)}, I_{OL} = 16 \text{ mA}$
 $V_{OH} = V_{CC} \text{ (10K pullup)}$

For Bus:

$V_{OL} = 0.5V \text{ (max)}, I_{OL} = 25 \text{ mA}$
 $V_{OH} = 3.65V \text{ (min)}, I_{OH} = 1 \text{ mA}$

Others:

$V_{OL} = 0.5V \text{ (max)}, I_{OL} = 16 \text{ mA}$
 $V_{OH} = 2.4V \text{ (max)}, I_{OH} = 400 \mu A$

Environmental Characteristics

Operating Temperature — 0°C to 40°C

Operating Humidity — Up to 95% relative humidity without condensation

Reference Manuals

9800464 — ICE-48 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION**Part Number Description**

MDS-48-ICE	8048, 8748, 8035, 8021 CPU in-circuit emulator. Cable assembly and interactive diskette software included
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INTELLEC DOUBLE DENSITY DISKETTE OPERATING SYSTEM

Floppy diskette operating system provides high-speed input/output and data storage for Intellec microcomputer development systems

Supports all existing standard Intellec peripherals

Data on flexible diskette, addressed using soft-sectored format, allows 1/2 million-byte data capacity with up to 200 files per diskette

Software supports up to four double density drives and two single density drives, providing up to 2.5 megabytes of storage in one system

Provides access to all Intellec monitor facilities

Provides dynamic allocation and deallocation of diskette sectors for variable length files

Command file facility allows console commands submission from diskette file

Provides diskette operating system function callability from user programs

Relocating macroassembler contains full macro and conditional assembly capability

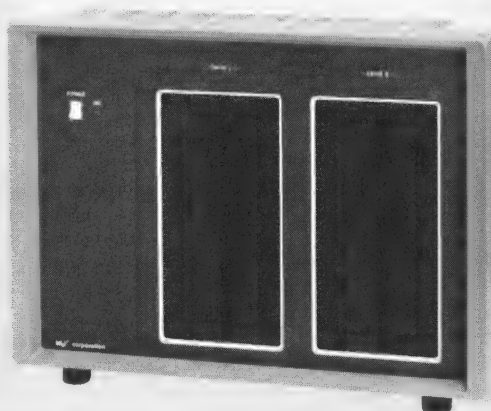
Linker automatically combines separately assembled or compiled programs into single relocatable module

Supports resident compiler for PL/M-80, Intel's high level programming language

Diskette system text editor provides string search, substitution, insertion, and deletion commands

Library Manager creates and updates program libraries

The Intellec Double Density Diskette Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system for use with Intellec microcomputer development systems and their peripherals. The user of a single or dual drive diskette operating system significantly reduces program development time. The software system known as ISIS-II (Intel Systems Implementation Supervisor) provides the ability to edit, assemble, compile, link, relocate, execute, and debug programs, and performs all file management tasks for the user.



FUNCTIONAL DESCRIPTION

The Intellec diskette system provides direct access bulk storage, an intelligent controller, and two diskette drives. Each drive provides 1/2 million bytes of storage with a data transfer rate of 500,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec system bus and supports the two diskette drives. The diskette system records all data in the IBM-compatible soft sector format and is capable of performing seven different operations: recalibrate, seek, format track, write data, wire deleted data, read data, and verify CRC. In addition to supporting a second set of double density drives, the diskette controller may co-reside with the Intel single density controller to allow conversion of single density diskettes to double density format. A functional diagram of the diskette operating system is shown in Figure 1.

Hardware

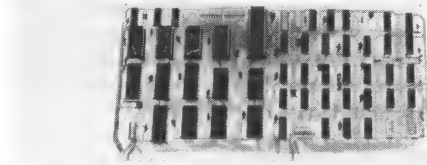
The diskette controller consists of two boards, the channel board and the interface board, as shown in the photograph in Figure 2. These two printed circuit boards reside in the Intellec system chassis and constitute the diskette controller.

Channel Board

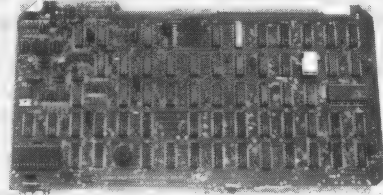
Control Function — The channel board is the primary control module within the diskette system. The channel board receives, decodes, and responds to channel commands from the 8080 central processor unit (CPU) in the Intellec system. The channel board can access a block of Intellec system memory to determine the particular diskette operations to be performed and to fetch the parameters required for successful completion of the specified operation.

Components — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512 x 32 bits of 3604 programmable read only memory

(PROM), which stores the microprogram. The execution of the microprogram by the microcomputer set effect the control capability of the channel board.



a. Channel Board



b. Interface Board

Figure 2. Two-Board Double Density Diskette Controller, Showing Channel and Interface Controller Boards

Interface Board

Communication Function — The interface board provides the diskette controller with a means of communicating with the diskette drives, as well as with the Intellec system bus. Under control of the microprogram being executed on the channel board, the interface board generates signals causing the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), and thus to move to the proper track and verify successful operation.

Read Operation — The interface board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board.

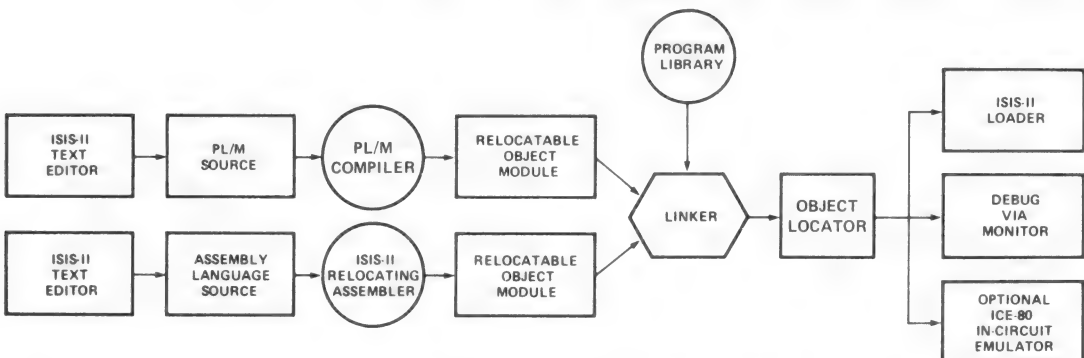


Figure 1. Double Density Diskette Operating System Program Development Flow Using ISIS-II Disk Operating System

Write Operation — During write operations, the interface board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

Memory Access — When the diskette controller requires access to Intellec system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intellec bus.

Diskette Drive Modules

Each diskette drive consists of read/write and control electronics, drive mechanisms, a read/write head, a track positioning mechanism, and the removable floppy diskette platter. These components interact to perform the following functions: interpret and generate control signals, move read/write head to selected track, and read and write data. A photograph of a double density diskette drive unit is shown in Figure 3.

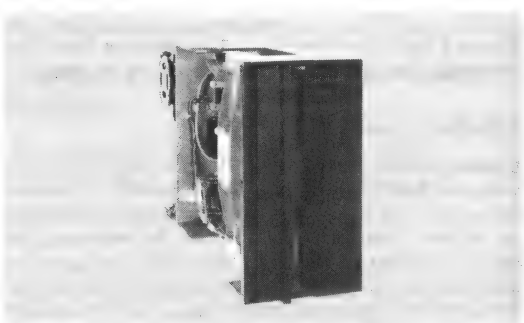


Figure 3. Double Density Diskette Drive Unit

ISIS-II Software

The Intel Systems Implementation Supervisor (ISIS-II) operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. A file is a user defined collection of information of variable length. ISIS-II also treats each of the standard Intellec system peripherals as files by pre-assigning unique file names to each device. In this manner data may be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user chosen name unique on its diskette. Up to 200 files may be stored on each 1/2 million byte diskette. Powerful system console commands are provided in an easy to use English con-

text. Monitor mode can be entered by a special prefix to any system command or program call.

ISIS-II System Commands

The ISIS-II system commands presented in Table 1 are designed to provide the user with a powerful, easy to use program and file manipulation capability. The attribute assignment (ATTRIB), delete, and directory listing (DIR) commands are also capable of operating on several files at once via the wildcard file-naming convention. As an example, the command "DELETE* .OBJ" deletes all files in the diskette directory with the suffix ".OBJ".

Command	Operation
Attribute	Assigns specified attributes to a file, such as write-protect.
Copy	Creates copies of existing diskette files or transfers files from one device to another.
Delete	Removes a file from the diskette, thereby freeing space for allocation of other files.
Directory	Lists name, size, and attributes of files from a specified diskette directory.
Rename	Allows diskette files to be renamed.
Format	Initializes a diskette and allows creation of additional system or data diskettes.
Debug	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and/or debugging.
Submit	Provides capability for executing a series of ISIS-II commands previously written to a diskette file.

Table 1. ISIS-II System Commands

Call Capability — The delete, rename, and attribute assignment commands, along with a set of file I/O routines, are callable from user written programs, thus allowing the user to open, close, read, and write diskette files, access standard peripheral devices, write error messages, and load other programs via simple program call statements.

ISIS-II Macroassembler

Capabilities — The ISIS-II 8080/8085 macroassembler translates symbolic 8080/8085 assembly language instructions into relocatable and/or absolute object code modules. The ability to refer to program addresses with symbolic names eliminates hand translation errors and makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code that may vary from system to system, such as the code required to handle optional external devices. Finally, the user is allowed complete freedom in assigning the location of code, data, and stack segments.

File Generation — The assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. The list file may then be examined from the system console or copied to a specified list device. The relocatable object file generated by the assembler may be either combined with other object programs residing on the diskette to form a single relocatable object module or converted to an absolute form or for subsequent loading and execution.

ISIS-II Linker

The ISIS-II linker combines the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module, automatically resolving all external program and data references during the linking process. Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays. An optional link map showing the contents and lengths of each segment in the output module may be requested. All unsatisfied external references are also listed. Upon user request, the ISIS-II linker searches a specified set of program libraries for routines to be included in the output module.

ISIS-II Object Locator

The ISIS-II object locator program takes output from either the PL/M-80 resident compiler, the macroassembler, or the linker and transforms that output from a relocatable format to an absolute format, which may then be loaded either via the standard ISIS-II loader or into the appropriate in-circuit emulator (ICE) module. During the locate process, code, data, and stack segments can be separately relocated, allowing code to be put into areas subsequently specified as ROM, while data and the stack can be directed to RAM addresses. A load map

showing absolute load addresses for each code and data segment and a symbol table dump listing symbols, attributes, and absolute addresses may also be requested.

ISIS-II Text Editor

The ISIS-II text editor is a comprehensive tool for entering and correcting assembly language and PL/M-80 programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line. Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace are stored on the diskette and may be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II macroassembler.

ISIS-II Library Manager

The ISIS-II Library Manager program provides for the creation and maintenance of a program library containing Intel-provided and user written programs and sub-routines. These library routines may be linked to a program using the ISIS-II linker. Several libraries, each containing its own set of routines, may be created.

SPECIFICATIONS

ISIS-II Operational Environment

32K bytes RAM memory
48K bytes when using macroassembly feature
64K bytes when using PL/M-80
System console
Floppy disk drives

Hardware Media

Double density specified flexible diskette
One recording surface
Soft sector format
77 tracks/diskette
52 sectors/track
128 bytes/sector

Diskette Drive Performance

Capacity (Unformatted)
Per Disk: 6.2 megabits
Per Track: 82 kilobits

Capacity (Formatted)

Per Disk: 4.10 megabits
Per Track: 53.2 kilobits

Data Transfer Rate — 500 kilobits/sec

Access Time

Track-to-Track: 10 ms
Head Settling Time: 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm

Average Latency — 83 ms

Recording Mode — M²FM

Physical Characteristics

Width — 16.88 in. (42.88 cm)

Height — 12.08 in. (30.68 cm)

Depth — 19.0 in. (48.26 cm)

Weight — 2 drives 64 lb (29 kg)

Mounting — Table-top or standard 19-in. RETMA cabinet

DOUBLE DENSITY DISKETTE

Electrical Characteristics

DC Power Requirements (Chassis)

Voltage	Current
5V	3A \pm 5%
-5V	600 mA \pm 5%
24V	4A \pm 5%

DC Power Requirements (Intellec DOS Controller)

Control Board	Voltage	Current
Channel board	5V	3.75A typ, 5A max
Interface board	5V	1.5A typ, 2.5A max
	-10V	0.1A typ, 0.2A max

AC Power Requirements — 3 wire input with center conductor (earth ground) tied to chassis; single-phase, 115/230V AC; 50-60 Hz; 160W

Environmental Characteristics

Media

Temperature: 15.6°C to 51.7°C operating; 5°C to 55°C non-operating

Humidity: 20% to 80% (wet bulb 2.67°C) operating; 5% to 95% non-operating

Drives and Chassis

Temperature: 10°C to 38°C operating; -35°C to 65°C non-operating

Humidity: 20% to 80% (wet bulb 26.7°C) operating; 5% to 95% non-operating

Controller Boards

Temperature: 0 to 55°C operating; -55°C to 85°C non-operating

Humidity: Up to 90% relative humidity without condensation, operating; all conditions without condensation of water or frost, non-operating.

Equipment Supplied

Cabinet, power supplies, line cord, single drive
FDC channel board
FDC interface board
Floppy disk controller cable
Floppy disk peripheral cable
ISIS-II double density system diskette

Optional Equipment

MDS-640 rack mount kit
MDS-BLD 10 blank diskettes
MDS-RLD ISIS-II system diskette
MDS-DDR second drive cabinet with two additional drives

Reference Manuals

9800422 — Double Density Diskette Operating System Hardware Reference Manual (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-DDS/110V /220V	Diskette unit with two double density drives, controller, and software
MDS-DDR/110V /220V	Add-on dual drive system. Includes two double density drives and cable. Allows support for four drives by ISIS-II software



INTELLEC SINGLE DENSITY DISKETTE OPERATING SYSTEM

Floppy diskette operating system provides high speed input/output and data storage for Intellec microcomputer development systems

Supports all existing standard Intellec peripherals

Data on flexible diskette, addressed using IBM soft-sectored format, allows 1/4 million-byte data capacity with up to 200 files per diskette

Provides access to all Intellec monitor facilities

Provides dynamic allocation and deallocation of diskette sectors for variable length files

Command file facility allowing console command submission from diskette file

Provides diskette operating system function callability from user programs

Relocating macroassembler contains full macro and conditional assembly capability

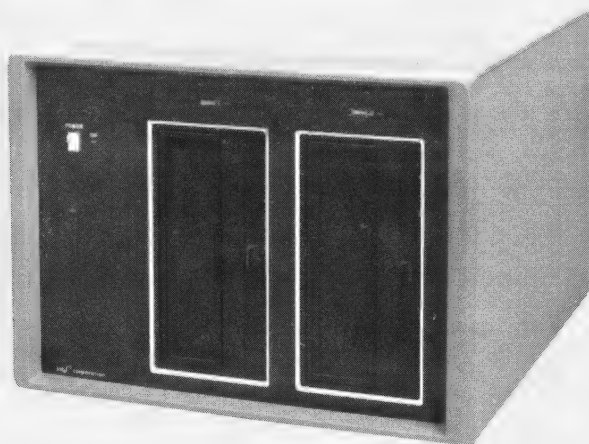
Linker automatically combines separately assembled or compiled programs into single relocatable module

Supports resident compiler for PL/M-80, Intel's high level programming language

Diskette system text editor provides string search, substitution, insertion, and deletion commands

Library Manager creates and updates program libraries

The Intellec Single Density Diskette Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system for use with Intellec microcomputer development systems and their peripherals. The user of a single or dual drive diskette operating system significantly reduces program development time. The software system known as ISIS-II (Intel Systems Implementation Supervisor) provides the ability to edit, assemble, compile, link, relocate, execute, and debug programs, and performs all file management tasks for the user.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

The Intellec diskette system provides direct access bulk storage, an intelligent controller, and up to two diskette drives. Each drive provides $\frac{1}{4}$ million bytes of storage with a data transfer rate of 250,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec system bus and supports the two diskette drives. The diskette system records all data in the IBM-compatible soft sector format and is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC. A functional diagram of the diskette operating system is shown in Figure 1.

Hardware

The diskette controller consists of two boards, the channel board and the interface board as shown in the photograph in Figure 2. These two printed circuit boards reside in the Intellec system chassis and constitute the diskette controller.

Channel Board

Control Function — The channel board is the primary control module within the diskette system. The channel board receives, decodes, and responds to channel commands from the 8080 central processor unit (CPU) in the Intellec system. The channel board can access a block of Intellec system memory to determine the particular diskette operations to be performed and to fetch the parameters required for successful completion of the specified operation.

Components — The control functions of the channel board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 bipolar microcomputer set. This 8-bit processor includes four 3002 central processing elements (2-bit slice per CPE), a 3001 microprogram control unit, and 512×32 bits of 3604 programmable read only memory (PROM), which stores the microprogram. The execution of the microprogram by the microcomputer set effects the control capability of the channel board.

a. Channel Board

b. Interface Board

Figure 2. Two-Board Single Density Diskette Controller, Showing Channel and Interface Controller Boards

Interface Board

Communication Function — The interface board provides the diskette controller with a means of communicating with the diskette drives, as well as with the Intellec system bus. Under control of the microprogram being executed on the channel board, the interface board generates signals causing the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), and thus to move to the proper track and verify successful operation.

Read Operation — The interface board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the channel board.

Write Operation — During write operations, the interface board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

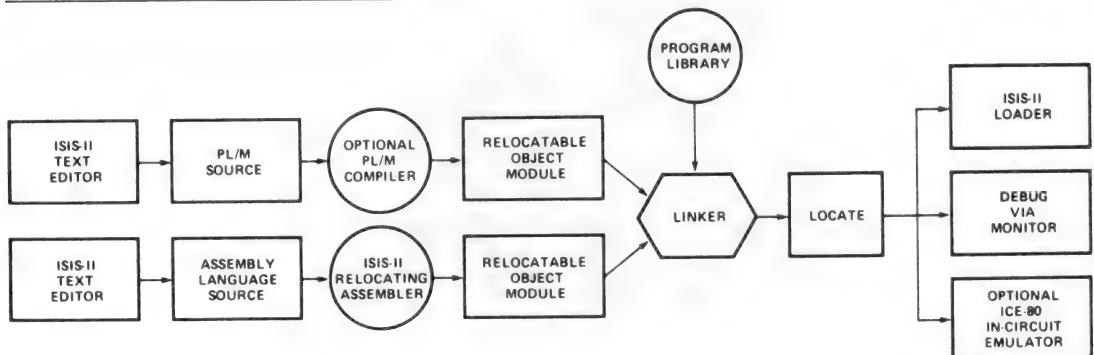


Figure 1. Single Density Diskette Operating System Program Development Flow Using ISIS-II Disk Operating System

Memory Access — When the diskette controller requires access to Intellec system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intellec bus.

Diskette Drive Modules

Each diskette drive consists of read/write and control electronics, drive mechanisms, a read/write head, a track positioning mechanism, and the removable floppy diskette platter. These components interact to perform the following functions: interpret and generate control signals, move read/write head to selected track, and read and write data. A photograph of a single density diskette drive unit is shown in Figure 3.

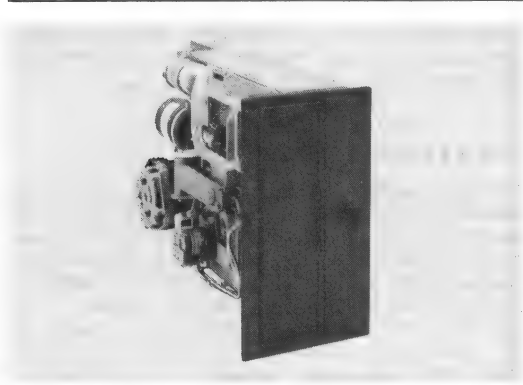


Figure 3. Single Density Diskette Drive Unit

ISIS-II Software

The Intel Systems Implementation Supervisor (ISIS-II) operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. A file is a user defined collection of information of variable length. ISIS-II also treats each of the standard Intellec system peripherals as files by pre-assigning unique file names to each device. In this manner data may be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user chosen name unique on its diskette. Up to 200 files may be stored on each ¼ million byte diskette. Powerful system console commands are provided in an easy to use English context. Monitor mode can be entered by a special prefix to any system command or program call.

ISIS-II System Commands

The ISIS-II system commands presented in Table 1 are designed to provide the user with a powerful, easy to use program and file manipulation capability. The attribute assignment (ATTRIB), delete, and directory listing (DIR) commands are also capable of operating on several files at once via the wildcard file-naming convention. As an example, the command "DELETE* .OBJ" deletes all files in the diskette directory with the suffix ".OBJ".

Command	Operation
Attribute	Assigns specified attributes to a file, such as write-protect.
Copy	Creates copies of existing diskette files or transfers files from one device to another.
Delete	Removes a file from the diskette, thereby freeing space for allocation of other files.
Directory	Lists name, size, and attributes of files from a specified diskette directory.
Rename	Allows diskette files to be renamed.
Format	Initializes a diskette and allows creation of additional system or data diskettes.
Debug	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and/or debugging.
Submit	Provides capability for executing a series of ISIS-II commands previously written to a diskette file.

Table 1. ISIS-II System Commands

Call Capability — The delete, rename, and attribute assignment commands, along with a set of file I/O routines, are callable from user written programs, thus allowing the user to open, close, read, and write diskette files, access standard peripheral devices, write error messages, and load other programs via simple program call statements.

ISIS-II Macroassembler

The ISIS-II 8080/8085 macroassembler translates symbolic 8080/8085 assembly language instructions into relocatable and/or absolute object code modules. The ability to refer to program addresses with symbolic names eliminates hand translation errors and makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code that may vary from system to system, such as the code required to handle optional external devices. Finally, the user is allowed complete freedom in assigning the location of code, data, and stack segments.

File Generation — The assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. The list file may then be examined from the system console or copied to a specified

list device. The relocatable object file generated by the assembler may be either combined with other object programs residing on the diskette to form a single relocatable object module or converted to an absolute form or for subsequent loading and execution.

ISIS-II Linker

The ISIS-II linker combines the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module, automatically resolving all external program and data references during the linking process. Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays. An optional link map showing the contents and lengths of each segment in the output module may be requested. All unsatisfied external references are also listed. Upon user request, the ISIS-II linker searches a specified set of program libraries for routines to be included in the output module.

ISIS-II Object Locator

The ISIS-II object locator program takes output from either the PL/M-80 resident compiler, the macroassembler, or the linker and transforms that output from a relocatable format to an absolute format, which may then be loaded either via the standard ISIS-II loader or into the ICE-8080 In-Circuit Emulator. During the locate process, code, data, and stack segments can be separately relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack can be directed to RAM addresses. A load map showing absolute load addresses for each code and data segment and a symbol table dump listing symbols, attributes, and absolute addresses may also be requested.

ISIS-II Text Editor

The ISIS-II text editor is a comprehensive tool for entering and correcting assembly language and PL/M-80 pro-

grams for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individuals characters within a line. Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace are stored on the diskette and may be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II macroassembler.

ISIS-II Library Manager

The ISIS-II Library Manager program provides for the creation and maintenance of a program library containing Intel-provided and user written programs and sub-routines. These library routines may be linked to a program using the ISIS-II linker. Several libraries, each containing its own set of routines, may be created.

ISIS-I 16K Absolute System

For owners of Intellec systems with less than 32K of memory, the limited capability ISIS-I diskette operating system is available. Included in ISIS-I is a text editor and absolute assembler. No relocation or linkage facilities exist with ISIS-I.

SPECIFICATIONS

ISIS-II Operational Environment

Intellec Microcomputer Development System
32K bytes RAM memory (non-macroassembler)
48K bytes of RAM memory (macroassembler)
System console
Single floppy disk

ISIS-I Operational Environment

Intellec Microcomputer Development System
16K bytes RAM memory
System console
Single floppy disk drive

Hardware Media

Flexible diskette
One recording surface
IBM soft sector format
77 tracks/diskette
26 sectors/track
128 bytes/sector

Diskette Drive Performance

Capacity (Unformatted)

Per Disk: 3.1 megabits
Per Track: 41 kilobits

Capacity (Formatted)

Per Disk: 2.05 M bits
Per Track: 26.6 K bits

SINGLE DENSITY DISKETTE

Data Transfer Rate — 250 kilobits/sec

Access Time

Track-to-Track: 10 ms

Head Settling Time: 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm

Average Latency — 83 ms

Recording Mode — Frequency modulation

Physical Characteristics

Width — 16.88 in. (42.88 cm)

Height — 12.08 in. (30.68 cm)

Depth — 19.0 in. (48.26 cm)

Weight — 1 drive 51 lb (23 kg), 2 drives 64 lb (29 kg)

Mounting — Table-top or standard 19-in. RETMA cabinet

Electrical Characteristics

DC Power Requirements (Chassis)

Voltage	Current
5V	3A \pm 5%
-5V	600 mA \pm 5%
24V	4A \pm 5%

DC Power Requirements (Intellec DOS Controller)

Control Board	Voltage	Current
Channel board	5V	3.75A typ, 5A max
Interface board	5V	1.5A typ, 2.5A max

AC Power Requirements — 3 wire input with center conductor (earth ground) tied to chassis; single-phase, 115/230V AC; 50-60 Hz; 160W

Environmental Characteristics

Media

Temperature: 15.6°C to 51.7°C operating; 5°C to 55°C non-operating

Humidity: 8 to 80% (wet bulb 29.4°C) operating; 8 to 90% non-operating

Drives and Chassis

Temperature: 10°C to 38°C operating; -35°C to 65°C non-operating

Humidity: 20% to 80% (wet bulb 26.7°C operating; 5% to 95% non-operating)

Controller Boards

Temperature: 0 to 70°C operating; -55°C to 85°C non-operating

Humidity: Up to 90% relative humidity without condensation, operating; all conditions without condensation of water or frost, non-operating.

Equipment Supplied

Cabinet, power supplies, line cord, single drive

FDC channel board

FDC interface board

Dual auxiliary board connector

Floppy disk controller cable

Floppy disk peripheral cable

ISIS-II system diskette

ISIS-I system diskette

Optional Equipment

Rack mount kit

MDS-DRV additional drive unit

Blank diskettes

ISIS-II system diskette

ISIS-I system diskette

Reference Manuals

9800212 — Single Density Diskette Operating System Hardware Reference Manual (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

MDS-1DS/110V /220V	Diskette unit with one drive, controller, and software
MDS-2DS/110V /220V	Diskette unit with two drives, controller, and software
MDS-DRV/110V /220V	Additional drive unit



PL/M-80 HIGH LEVEL PROGRAMMING LANGUAGE INTELLEC RESIDENT COMPILER

Provides resident operation on Intellec Microcomputer Development System and Intellec Series II microcomputer development systems

Speeds project completion with increased programmer productivity

Produces relocatable and linkable object code

Cuts software development and maintenance costs

Sophisticated code optimization reduces application memory requirements

Improves product reliability with simplified language and consequent error reduction

Eases enhancement as system capabilities expand

The PL/M-80 High Level Programming Language Intellec Resident Compiler is an advanced, high level programming language for Intel 8080 and 8085 microprocessors, iSBC-80 OEM computer systems, and Intellec microcomputer development systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs. PL/M is an algorithmic language in which program statements naturally express the algorithm to be programmed, thus freeing programmers to concentrate on system development rather than assembly language details (such as register allocation, meanings of assembler mnemonics, etc.). The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080/8085 instructions. Substantially fewer PL/M statements are necessary for a given application than would be using assembly language or machine code. Since PL/M programs are problem oriented and thus more compact, programming in PL/M results in a high degree of productivity during development efforts, resulting in significant cost reduction in software development and maintenance for the user.

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FUNCTIONAL DESCRIPTION

The PL/M compiler is an efficient multiphase compiler that accepts source programs, translates them into object code, and produces requested listings. After compilation, the object program may be first linked to other modules, then located to a specific area of memory, and finally executed. The diagram shown in Figure 1 illustrates a program development cycle where the program consists of three modules: PL/M, FORTRAN, and assembly language. A typical PL/M compiler procedure is shown in Table 1.

Features

Major features of the Intel PL/M-80 compiler and programming language include:

Resident Operation — on Intel microcomputer development systems eliminates the need for a large in-house computer or costly timesharing system.

Object Code Generation — of relocatable and linkable object codes permits PL/M program development and debugging in small modules, which may be easily linked with other modules and/or library routines to form a complete application.

Extensive Code Optimization — including compile time arithmetic, constant subscript resolution, and common subexpression elimination, results in generation of short, efficient CPU instruction sequences.

Symbolic Debugging — fully supported in the PL/M compiler and ICE-85 in-circuit emulators.

Compile Time Options — includes general listing format commands, symbol table listing, cross reference listing, and "innerlist" of generated assembly language instructions.

Block Structure — aids in utilization of structured programming techniques.

Access — provided by high level PL/M statements to hardware resources (interrupt systems, absolute addresses, CPU input/output ports).

Data Definition — enables complex data structures to be defined at a high level.

Re-entrant Procedures — may be specified as a user option.

Benefits

PL/M is designed to be an efficient, cost-effective solution to the special requirements of microcomputer software development as illustrated by the following benefits of PL/M use:

Low Learning Effort — even for the novice programmer, because PL/M is easy to learn.

Earlier Project Completion — on critical projects, because PL/M substantially increases programmer productivity while reducing program development time.

Lower Development Cost — because increased programmer productivity requiring less programming resources for a given function translates into lower software development costs.

Increased Reliability — because of PL/M's use of simple statements in the program algorithm, which are easier to correct and thus substantially reduce the risk of costly errors in systems that have already reached full production status.

Easier Enhancement and Maintenance — because programs written in PL/M are easier to read and easier to understand than assembly language, and thus are easier to enhance and maintain as system capabilities expand and future products are developed.

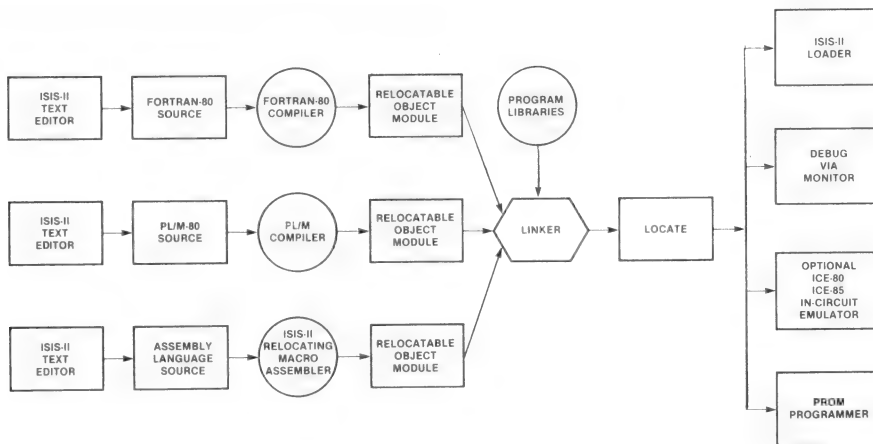


Figure 1. Program Development Cycle Block Diagram

Simpler Project Development — because the Intellec microcomputer development system with resident PL/M-80 is all that is needed for developing and debug-

ging software for 8080 and 8085 microcomputers, and the use of expensive (and remote) timesharing or large computers is consequently not required.

		\$OBJECT(:F1:FACT.OB2)
		\$DEBUG
		\$XREF
		\$TITLE('FACTORIAL GENERATOR — PROCEDURE')
		\$PAGEWIDTH(80)
1		FACT:
		DO;
2	1	DECLARE NUMCH BYTE PUBLIC;
3	1	FACTORIAL: PROCEDURE (NUM,PTR) PUBLIC;
4	2	DECLARE NUM BYTE, PTR ADDRESS;
5	2	DECLARE DIGITS BASED PTR (161) BYTE;
6	2	DECLARE (I,C,M) BYTE;
7	2	NUMCH = 1; DIGITS(1) = 1;
9	2	DO M = 1 TO NUM;
10	3	C = 0;
11	3	DO I = 1 TO NUMCH;
12	4	DIGITS(I) = DIGITS(I)*M + C;
13	4	C = DIGITS(I)/10;
14	4	DIGITS(I) = DIGITS(I) — 10*C;
15	4	END;
16	3	IF C<>0 THEN
17	3	DO;
18	4	NUMCH = NUMCH + 1; DIGITS(NUMCH) = C;
20	4	C = DIGITS(NUMCH)/10;
21	4	DIGITS(NUMCH) = DIGITS(NUMCH) — 10*C;
22	4	END
		END;
24	2	END FACTORIAL;
25	1	END;

Table 1. PL/M-80 Compiler Sample Factorial Generator Procedure

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec microcomputer development system
65K bytes of memory
Dual diskette drives
System console — teletype

Optional Hardware

CRT as system console
Line printer

Required Software — ISIS-II diskette operating system

Shipping Media

Diskette

Reference Manuals

980026 — PL/M-80 Programming Manual (SUPPLIED)

9800300 — ISIS-II PL/M-80 Compiler Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code Description

MDS-PLM High level language compiler



FORTRAN-80 8080/8085 ANS FORTRAN 77 INTELLEC RESIDENT COMPILER

Provides resident operation on Intellec Microcomputer Development System and Intellec Series II microcomputer development systems

Meets and exceeds ANS FORTRAN 77 Subset Language Specification

Produces relocatable and linkable object code compatible with resident PL/M-80 and 8080/8085 macroassembler

Supports Intel floating point standard

Provides full FORTRAN 77 language I/O support when used with ISIS-II runtime library

Sophisticated code optimization insures efficient program implementation

Supports full symbolic debugging with ICE-80 and ICE-85

FORTAN-80 is a computer industry standard, high level programming language and compiler that translates FORTRAN statements into relocatable object modules. When the object modules are linked together and located into absolute program modules, they are suitable for execution on Intel 8080/8085 microprocessors, ISBC-80 OEM computer systems, and Intellec microcomputer development systems. FORTAN-80 meets and exceeds the ANS FORTRAN 77 Language Subset Specification¹. The compiler operates on Intellec microcomputer development systems under ISIS-II disk operating systems and produces efficient relocatable object modules compatible for linkage with PL/M-80 and 8080/8085 macroassembler modules. The ANS FORTRAN 77 language specification offers many powerful extensions to the FORTRAN language that are especially well suited to Intel 8080/8085 microprocessor software development. Because FORTAN-80 conforms to the ANS FORTRAN 77 standard, the user is assured of compatibility with existing FORTRAN software meeting the standard as well as a guarantee of upward compatibility to other computer systems supporting an ANS FORTRAN 77 compiler.

¹ ANSI X3J3/90



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FUNCTIONAL DESCRIPTION

The FORTRAN-80 compiler is an efficient, multiphase compiler that accepts source programs, translates them into relocatable object code, and produces requested listings. After compilation, the object program may be linked to other modules, then located to a specific area of memory, and finally executed. The diagram shown in Figure 1 illustrates a program development cycle where the program consists of modules created by FORTRAN-80, PL/M-80, and the 8080/8085 macroassembler. A sample of a FORTRAN-80 program source listing is shown in Table 1.

Language Features

Major ANS FORTRAN 77 features supported by the Intel FORTRAN-80 programming language include:

Structured Programming — supported with the IF... THEN... ELSE IF... ELSE... END IF constructs.

Character Data Type — permitting alphanumeric data to be handled as strings rather than as characters stored in array elements.

Full I/O Capabilities — including sequential and direct access files; error handling facilities; formatted, free-formatted, and unformatted data representation; internal (in-memory) file units providing capability to format and reformat data in internal memory buffers; and list directed formatting.

Support Array — up to seven dimensions.

Logical Operator Support — including .EQV (logical equivalence) and .NEQV. (logical nonequivalence).

Language Extensions

Major extensions to FORTRAN 77 in Intel FORTRAN-80 include:

Input/Output — direct 8080/8085 port I/O supported by intrinsic subroutines.

Versatility — binary and hexadecimal integer constants.

Storage Capacity — user defined integer storage lengths of 1, 2, or 4 bytes; user defined logical storage lengths of 1, 2, or 4 bytes; real storage lengths of 4 bytes.

Boolean Logic — bitwise Boolean operations using logical operators on integer values.

Hollerith Data Constants

Automatic Formatting — implicit extension of the length of an integer or logical expression to the length of the left-hand side in an assignment statement.

End Record — a format descriptor to suppress carriage return on a terminal output device at the end of the record.

Compiler Features

Expandability — supports multiple compilation units in single source file.

Listings — comprehensive cross-reference, symbol attribute, and error listing; optional assembly language code listing.

Compatibility — compiler controls and directives compatible with other Intel language translators.

Optional Re-entrancy

Default Storage — user defined default storage lengths.

Semantics — optional FORTRAN 66 Do loop semantics.

Source Files — may be prepared in free format.

Include Control — permits specified source files to be combined into a compilation unit at compile time.

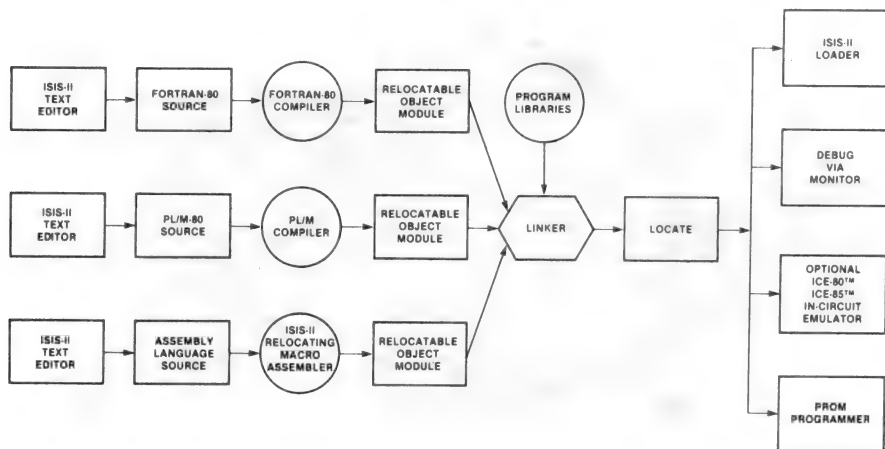


Figure 1. Program Development Cycle Block Diagram

```

C THIS PROGRAM IS AN EXAMPLE OF ISIS-II FORTRAN-80 THAT
C CONVERTS TEMPERATURE BETWEEN CELSIUS AND FAHRENHEIT
C
  PROGRAM CONVRT
  CHARACTER*1 CHOICE,SCALE
  PRINT 1
1  FORMAT (' TEMPERATURE CONVERSION PROGRAM'/,
  ' TYPE C FOR FAHRENHEIT TO CELSIUS OR /,
  ' F FOR CELSIUS TO FAHRENHEIT'/)
10 PRINT 2
2  FORMAT (/, ' CONVERSION? ', $)
  READ (5,3) SCALE
3  FORMAT (A1)
  IF (SCALE.EQ.'C') THEN
    PRINT 4
4    FORMAT (/, ' ENTER DEGREES FAHRENHEIT? ', $)
    READ (5,*) DEGF
    DEGC = 5./9. * DEGF - 32.
    WRITE (6,5) DEGF,DEGC
5    FORMAT (/,F7.2, ' DEGREES FAHRENHEIT = ',F7.2, ' DEGREES CELSIUS'/)
11  PRINT 6
6    FORMAT (/, ' AGAIN (Y OR N)? ', $)
    READ (5,3) CHOICE
    IF (CHOICE.EQ.'Y') THEN
      GOTO 10
    ELSE IF (CHOICE.EQ.'N') THEN
      CALL EXIT
    ELSE
      GOTO 11
    END IF
  ELSE IF (SCALE.EQ.'F') THEN
    PRINT 7
7    FORMAT (/, ' ENTER DEGREES CELSIUS? ', $)
    READ (5,*) DEGC
    DEGF = 9./5. * DEGC + 32.
    WRITE(6,8) DEGC,DEGF
8    FORMAT (/,F7.2, ' DEGREES CELSIUS = ',F7.2, ' DEGREES FAHRENHEIT'/)
    GOTO 11
  ELSE
    WRITE (6,9) SCALE
9    FORMAT (/,1H,A1, ' NOT A VALID CHOICE — RETRY!'/)
    GOTO 10
  END IF
END
  
```

Table 1. Sample FORTRAN-80 Program Source Listing

Benefits

FORTRAN-80 provides a means of developing application software for Intel MCS-80/85 products in a familiar, widely accepted, and computer industry-standardized programming language. FORTRAN-80 will greatly enhance the user's ability to provide cost-effective solutions to software development for Intel microprocessors as illustrated by the following:

Complete Complementarity to Existing Intel Software Design Tools — because object modules are linkable with new or existing assembly language and PL/M modules.

Incremental Runtime Library Support — because run-time overhead is limited only to facilities required by the program.

Low Learning Effort — because FORTRAN-80, like PL/M, is easy to learn and use. Existing FORTRAN software can be ported to FORTRAN-80, and programs developed in FORTRAN-80 can be run on any other computer with ANS FORTRAN-77.

Earlier Project Completion — on critical projects, because FORTRAN-80 substantially increases programmer productivity and complements PL/M modules by providing comprehensive arithmetic, I/O formatting, and data management support in the language.

Lower Development Cost — because increased programmer productivity requiring less programming resources for a given function translates into lower software development costs.

Increased Reliability — because the nature of high level languages, including FORTRAN-80, is that they lend themselves to simple statements of the program algorithm, and thus substantially reduce the risk of costly errors in systems that have already reached production status.

Easier Enhancements and Maintenance — because, like PL/M, program modules written in FORTRAN-80 are easier to read and understand than assembly language, and thus are easier to enhance and maintain as system capabilities expand and future products are developed.

Comprehensive, Yet Simple Project Development — because the Intel Microcomputer Development System, with the 8080/8085 macroassembler, PL/M-80, and FORTRAN-80 is the most comprehensive software design facility available for the Intel MCS-80/85 microprocessor family, and the use of expensive (and remote) timesharing or large computers is consequently not required.

SPECIFICATIONS

Operating Environment

Required Hardware

Intel Microcomputer Development System: MDS-800, MDS-888; Series II Model 220, Model 230

64K bytes of RAM memory

Dual diskette drives, single or double density

System console: CRT or hardcopy interactive device

Optional Hardware

ICE-80, ICE-85

Line printer

Required Software — ISIS-II diskette operating system, single or double density

Shipping Media

Flexible Diskettes — Single and double density

Reference Manuals

9800481 — FORTRAN-80 Programming Manual (SUPPLIED)

9800480 — ISIS-II FORTRAN-80 Compiler Operator's Manual (SUPPLIED)

9800547 — FORTRAN-80 Programming Reference Card (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code	Description
MDS-301	FORTRAN-80 Compiler for Inteltec microcomputer development systems



MCS-48 DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec microcomputer development system to support MCS-48 development

Takes advantage of powerful ISIS-II file handling and storage capabilities

MCS-48 assembler provides conditional assembly and macro capability

Provides assembler output in standard Intel hex format

The MCS-48 Diskette-Based Software Support Package is provided with the Intel ISIS-II system diskette and contains both the MCS-48 assembler and the diskette version of the universal PROM mapper. The assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes, and provides both conditional and macroassembler programming. Output may be loaded either to an ICE-48 module for debugging or into an Intellec microcomputer development system for 8748 PROM programming using the universal PROM programmer.



FUNCTIONAL DESCRIPTION

The MCS-48, a software support assembler package, is provided with the ISIS-II system diskette and contains both the MCS-48 assembler and the diskette version of the universal PROM mapper. The MCS-48 assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. The ability to refer to program addresses with symbolic names eliminates the errors of hand translation and makes it easier to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify which portions of the master source document should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices. Macro capability allows the programmer use of a single label to define a routine. The MCS-48 assembler will assemble the code required by the reserved routine whenever the macro label is inserted in the text. Output from the assembler is in standard Intel hex format. It may be either loaded directly to an in-circuit emulator (ICE-48) module for integrated hardware/software debugging, or loaded into an Intel development system for 8748 PROM programming using the universal PROM programmer. A sample assembly listing is shown in Table 1.

ISIS-II 8048 MACROASSEMBLER, V1.0		PAGE 1	
LOC	OBJ	SEQ	SOURCE STATEMENT
		1	.DECIMAL ADDITION ROUTINE ADD BCD NUMBER
		2	.AT LOCATION BETA TO BCD NUMBER AT ALPHA WITH
		3	.RESULT IN ALPHA LENGTH OF NUMBER IS COUNT DIGIT
		4	.PAIRS. (ASSUME BOTH BETA AND ALPHA ARE SAME LENGTH
		5	.AND HAVE EVEN NUMBER OF DIGITS OR MSD IS 0 IF
		6	.ODD)
		7	INIT MACRO AUGND,ADDND,CNT
		8	MOV R0,#AUGND
		9	MOV R1,#ADDND
		10	MOV R2,#CNT
		11	ENDM
		12	
0001E		13	ALPHA EQU 30
0028		14	BETA EQU 40
0032		15	COUNT EQU 5
0100		16	ORG 100H
		17	INIT ALPHA, BETA, COUNT
0100 B01E		18+	MOV R0,#ALPHA
0102 B928		19+L1:	MOV R1,#BETA
0104 BA32		20+	MOV R2,#COUNT
0108 97		21	CLR C
0107 F0		22	LP: MOV A,@R0
0108 71		23	ADDC A,@R1
0109 57		24	DA A
010A A1		25	MOV @R0,A
010B 18		26	INC R0
010C 19		27	INC R1
010D EA07		28	DJNZ R2,LP
			END
USER SYMBOLS			
ALPHA	0001E	BETA	0028
L1	0102	COUNT	0005
		LP	0107
ASSEMBLY COMPLETE, NO ERRORS			
ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V1.0		PAGE 1	
SYMBOL CROSS REFERENCE			
ALPHA	13#	17	
BETA	14#	17	
COUNT	15#	17	
INIT	7#	17	
L1	10#		
LP	22#	28	

Table 1. Sample MCS-48 Diskette-Based Assembly Listing

SPECIFICATIONS

Operating Environment

Required Hardware

Intel microcomputer development system

System console

Intel diskette operating system

32K RAM (non-macroassembler)

48K RAM (macroassembler)

Optional Hardware

Universal PROM programmer

Shipping Media

Diskette

Reference Manuals

9800255 — MCS-48/UPI-41 Assembly Language Programming Manual (SUPPLIED)

9800236 — Universal PROM Mapper Operator's Manual (SUPPLIED)

9800306 — ISIS-II User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code Description

MDS-D48 Diskette-based assembler for MCS-48 family of microprocessors



INTELLEC SYSTEM CRT KEYBOARD DISPLAY

**Teleprinter compatible CRT terminal
with detachable keyboard**

**Asynchronous data transfer rates switch
selectable up to 9600 baud**

RS232C compatible

System tested with Intellec system

**2000-character capacity in 25 lines of 80
characters each**

**Cursor positioning (left, right, up, or
down) and cursor homing capability**

**Each CRT complete with cable and
power supply**

The Intellec System CRT Keyboard Display Unit is fully compatible with the Intellec microcomputer development systems and diskette operating systems, and with the entire range of the Intellec system in-circuit emulator design aids.



INTELLEC
SYSTEMS

SPECIFICATIONS

Display Format

25 lines x 80 characters

Display Size

Approximately 6.5 in. high x 8.4 in. wide

CRT Size

12 in., measured diagonally

Character Size

Approximately 0.2 in. high x 0.1 in. wide

Character Type

5- x 7-dot matrix, 2-dot spacing between characters, white on black

Character Set

64-character ASCII

Character Generation

MOS ROM

Refresh Rate

60 Hz, 50 Hz optional

Refresh Memory

MOS shift register

Cursor Control

Left, right, up, down, home, carriage return, line feed

Communications Interface

Serial RS232C

Transmission Rate

Switchable to 9600 baud; monitor program supports 300, 1200, and 2400 baud

Communication Mode

Full duplex, half duplex, 10- or 11-bit word asynchronously only

Parity

Odd, even mark, space + transmit and receive check or no check on received data

Character Mode

Character by character transmission

Erase Mode

Erase to end of line, erase to end of memory, clear

Bell

Audible alarm when control G is received or 70th character of line

Keyboard

Standard TTY keyboard, custom designed, detachable module, color coordinated by Intel

Terminal Finish

Textured vinyl

Operator Controls

Keyboard — Brightness, on-line/local

Rear Panel — Power, full duplex/half duplex

I/O Baud Rate — Contrast

Physical Characteristics

Monitor

Width: 16.5 in (41.9 cm)

Height: 15.0 in. (38.1 cm)

Depth: 15.0 in. (38.1 cm)

Weight: 45 lb (20.6 kg) approximately

Keyboard

Width: 16.5 in (41.9 cm)

Height: 3.5 in (8.9 cm)

Depth: 9.7 in. (24.6 cm)

Weight: 7 lb (3.2 kg) approximately

Electrical Characteristics

Input Voltage

115V AC $\pm 10\%$ 60 Hz

115V AC $\pm 10\%$ 50 Hz (optional)

230V AC $\pm 10\%$ 50 Hz (optional)

Environmental Characteristics

Operating Temperature — 5°C to 40°C after warmup

Reference Manuals

None

ORDERING INFORMATION

Part Number	Description
MDS-CRT	Keyboard display unit



INTELLEC PRINTER

Provides listing of hard copy output at 55 lines per minute

Switch selectable to 80 or 132 characters per 8½-inch line

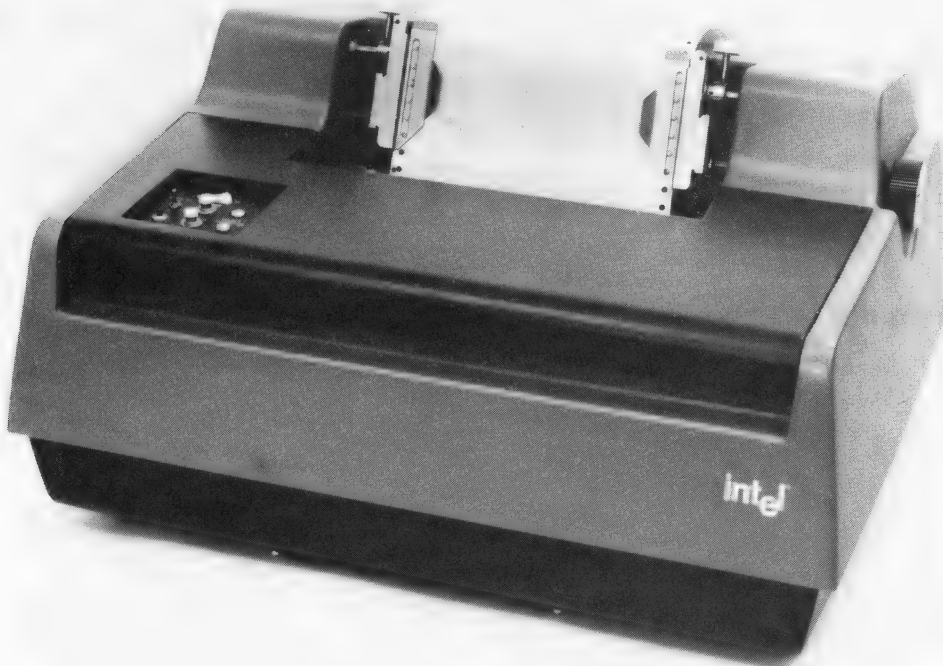
Employs 5 × 7 dot matrix with standard 2-channel, vertical control format

Prints up to four copies on standard 8½-inch fanfold paper

Provides automatic on-off motor switch for quiet operation

Provides optional finished metal stand and paper takeup tray

The Intellec Printer provides hard copy listings at 10 to 16 times the speed of a teleprinter. The automatic on-off motor control allows the user to maintain a low noise environment and yet send information to the printer from the Intellec system console without additional manipulation of line printer switches. The user may select a column width of 80 characters per line (10 characters per inch) or 132 characters per line (16.5 characters per inch) either manually or under program control. Top of page spacing capability is available under user programmable format control. The printer uses standard 8½-inch fanfold paper and can produce up to four carbon copies along with the original. Paper may be fed either from the bottom or from the rear of the printer for versatility in any lab environment.



INTELLEC
SYSTEMS

SPECIFICATIONS

Printing Method

Impact, character-by-character printing, one line character buffer

Printing Rate

Characters — 100 or 165 cps

Full Lines — 55 lines per minute (80- or 132-character line)

Transmission Rate

Parallel — Up to 75,000 characters per second

Data Input

Parallel

Character Structure

5 × 7 dot matrix, 10-point type equivalent

Code

USASCII — 64 characters printed

Switch Controls

On/off

Select

Forms override

Normal/condensed top of form

Indicators

Paper out

Select

Manual Controls

Form thickness

Paper advance knob

Buffer

One line character buffer

Format

80 or 132 characters maximum per line, 6 lines per inch

Paper Feed

Sprocket fed, 4 I.P.S. slew, adjustable to 9½-in. width

Paper

Standard sprocketed paper

Number of Copies

Original and up to four carbon copies

Warranty

The MDS-PRN is warranted against defects in materials and workmanship for a period of one (1) year on mechanical parts, 90 days on electrical parts, and 45 days on labor.

Physical Characteristics

Width — 23.25 in. (59.1 cm)

Height — 12.75 in. (32.4 cm)

Depth — 18.75 in. (47.6 cm)

Weight — 66 lb (30.2 kg)

Electrical Characteristics

115V AC ± 10%, 60 Hz (or 230V AC ± 10%, 50 Hz as option)

Environmental Characteristics

Temperature — 40° to 100°F, operating; -40° to 160°F, storage

Humidity — 5% to 90% (no condensation) operating; 0% to 95% (no condensation) storage

Optional Equipment

MDS-STD finished metal stand and paper tray

Reference Manuals

None

ORDERING INFORMATION

Part No.	Description
MDS-PRN	Printer unit
MDS-STD	Stand and paper tray



INTELLEC HIGH SPEED PAPER TAPE READER

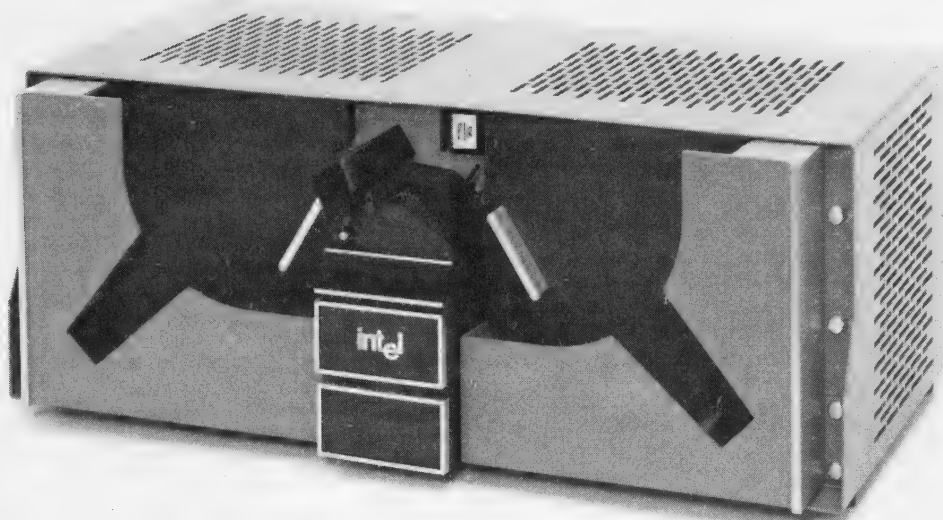
**Reads paper tape twenty times faster
than standard ASR-33 teletype reader**

**Transfers data at asynchronous rates in
excess of 2000 characters per second**

**Loads 16K Intellec program memory in
less than three minutes**

**Usable as rack-mountable or stand-alone
unit**

The Intellec High Speed Paper Tape Reader is an Intellec peripheral that reads paper tape at a speed over twenty times faster than the standard ASR-33 teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations. A general purpose paper tape reader driver is included in the Intellec monitor to enable all system software or user written application programs to utilize the high speed reader features. The monitor also provides dynamic I/O reconfiguration, permitting reassignment of the high speed reader to other logical input devices. Reader data and command interface hardware is provided with the basic Intellec. A reader/Intellec system interface cable is included with the unit. A fanfold tape guide is also included to provide fanfold punch capability to the ASR-33 teletype. The high speed reader may be used either as a table top unit or mounted in a standard 19-inch RETMA cabinet.



INTELLEC
SYSTEMS

HIGH SPEED PAPER TAPE READER

SPECIFICATIONS

Tape Movement

Tape Reader Speed — 0 to 200 cps asynchronous

Tape Stopping — stops "on character"

Tape Characteristics

Reads tape of any material with thickness between 0.0027 in. and 0.0045 in. with transmissivity less than or equal to 57% (oiled buff paper tape). Tape must be prepared to ANSI X 3.18 or EMCA 10 standards for base materials and perforations.

Tape Loading — in line

Tape Width — 1 inch

Physical Characteristics

Width — 19.25 in. (48.90 cm)

Height — 7.75 in. (19.69 cm)

Depth — 11.62 in. (29.52 cm)

Weight — 13 lb (5.9 kg)

Electrical Characteristics

AC Power Requirements — 3-wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127V AC, single phase at 3.0 amps or 220 or 240V AC and 1.5 amps; 47 to 63 Hz.

Environmental Characteristics

Temperature — 0 to 55°C (free air), operating; -55°C to +85°C, non-operating

Humidity — up to 90% relative humidity without condensation, operating; all conditions without condensation of water or frost, storage.

Equipment Supplied

Paper tape reader

Reader cable

Fanfold tape guide

Fanfold paper tape

Reference Manuals

None

ORDERING INFORMATION

Part Number	Description
MDS-PTR	Paper tape reader



UPP-103* UNIVERSAL PROM PROGRAMMER

**Replaces UPP-101, UPP-102 Universal PROM Programmers*

**Intellec development system peripheral
for PROM programming and verification**

**Provides personality cards for program-
ming all Intel PROM families**

**Provides zero insertion force sockets for
both 16-pin and 24-pin PROMs**

**Universal PROM mapper software pro-
vides powerful data manipulation and
programming commands**

**Provides flexible power source for
system logic and programming pulse
generation**

**Holds two personality cards to facilitate
programming operations using several
PROM types**

The UPP-103 Universal PROM Programmer is an Intellec system peripheral capable of programming and verifying the following Intel programmable ROMs (PROMs): 1702A, 2704, 2708, 2716, 3601, 8702A, 8704, and 8708. In addition, the UPP-103 programs the PROM memory portions of the 8748 microcomputer and the 8755 PROM and I/O chip. Programming and verification operations are initiated from the Intellec development system console and are controlled by the universal PROM mapper (UPM) program.



INTELLEC
SYSTEMS

FUNCTIONAL DESCRIPTION

Universal PROM Programmer

The basic Universal PROM Programmer (UPP) consists of a controller module, two personality card sockets, a front panel, power supplies, a chassis, and an Intellec development system interconnection cable. An Intel 4040-based intelligent controller monitors the commands from the Intellec System and controls the data transfer interface between the selected PROM personality card and the Intellec memory. A unique personality card contains the appropriate pulse generation functions for each Intel PROM family. Programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card. The front panel contains a power-on switch and indicator, a reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides power for system logic and for PROM programming pulse generation. The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19-inch RETMA cabinet.

Universal PROM Mapper

The Universal PROM Mapper (UPM) is the software program used to control data transfer between paper tape

or diskette files and a PROM plugged into the Universal PROM Programmer. It uses Intellec system memory for intermediate storage. The UPM transfers data in 8-bit HEX, BNPF, or binary object format between paper tape or diskette files and the Intellec system memory. While the data is in Intellec system memory, it can be displayed and changed. In addition, word length, bit position, and data sense can be adjusted as required for the PROM to be programmed. PROMs may also be duplicated or altered by copying the PROM contents into the Intellec system memory. Easy to use program and compare commands give the user complete control over programming and verification operations. The UPM eliminates the need for a variety of personalized PROM programming routines because it contains the programming algorithms for all Intel PROM families.

Optional Versions

There are two versions of the UPM: one that runs under the Intellec system monitor (paper tape system), and one that runs under ISIS-II, the Intellec diskette operating system (diskette-based system). The paper tape version is included with the Universal PROM Programmer. The diskette-based version of the UPM is available on all ISIS-II system diskettes.

SPECIFICATIONS

Hardware Interface

Data — Two 8-bit unidirectional buses

Commands — 3 write commands, 2 read commands, one initiate command

Physical Characteristics

Width — 6 in. (14.7 cm)

Height — 7 in. (17.2 cm)

Depth — 17 in. (41.7 cm)

Weight — 18 lb (8.2 kg)

Electrical Characteristics

AC Power Requirements — 50–60 Hz; 115/230V AC; 80W

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Optional Equipment

Personality Cards

UPP-361: 3601 personality card

UPP-816: 2716 personality card

UPP-848: 8748 personality card with 40-pin adaptor socket

UPP-855: 8755 personality card with 40-pin adaptor socket

UPP-865: 3602, 3622, 3602A, 3622A, 3621, 3604, 3624,

3604A, 3624A, 3604AL, 36046-6, 3605, 3625, 3608, 3628

UPP-872: 8702A/1702A personality card

UPP-878: 8708/8704/2708/2704 personality card

PROM Programming Sockets

UPP-501: 16-pin/24-pin socket pair

UPP-502: 24-pin/24-pin socket pair

UPP-562: Socket adaptor for 3621, 3602, 3622, 3602A, 3622A

UPP-555: Socket adaptor for 3604AL, 36046-6, 3608, 3628

UPP-565: Socket adaptor for 3605, 3625

Equipment Supplied

Cabinet

Power supplies

4040 intelligent controller module

Specified zero insertion force socket pair

Intellec development system interface cable

Universal PROM Mapper program (paper tape version — disk-based version available on ISIS-II diskettes)

Reference Manuals

9800133 — Universal PROM Programmer Hardware Reference Manual (SUPPLIED)

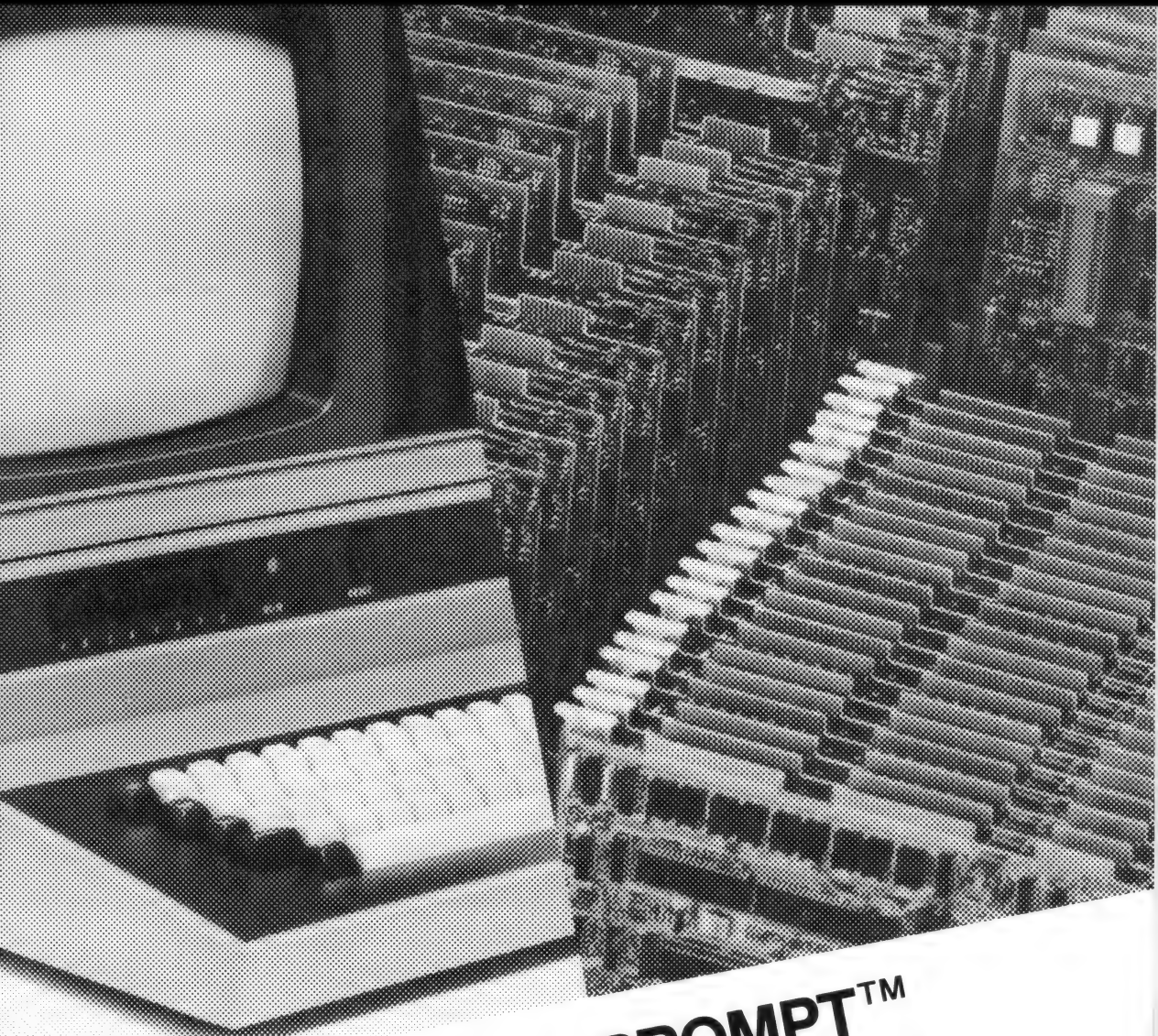
9800554 — Intellec Series II Schematics Drawings (SUPPLIED)

9800236 — Universal PROM Mapper Operator's Manual (SUPPLIED)

ORDERING INFORMATION

Part Number Description

UPP-103	Universal PROM programmer with 16-pin/24-pin socket pair and 24-pin/24-pin socket pair
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**11 PROMPT™
Design Aids**

PROMPT DESIGN AIDS

INTRODUCTION

"PROMPT" stands for PROgraMing Tool. The two Intel PROMPT design aids described in this section are low cost programming design tools used to simplify microcomputer programming by preparing and verifying small, modular routines that together may comprise sizable programs. The PROMPT 80/85 simplifies the programming of 8080/8085 processors and iSBc 80 and System 80 microcomputers, as well as 8708/8755 EPROMs and 8255/8251 programmable I/O devices. PROMPT 48 simplifies the programming of MCS-48 systems. Like the MCS-48 8748 processor, it is radically new, highly integrated, and expandable. Like the entire MCS-48 family, it is low cost and ideal for small applications and programs.

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INTELLEC PROMPT 80/85 8080/8085 MICROCOMPUTER DESIGN AID

Simplifies microcomputing, allowing user to enter, run, debug, and save machine language programs with calculator-like ease

Complete, low cost fully-assembled microcomputer design aid and EPROM programmer for:

- Standard 8080A CPU on popular iSBC 80/10 Single Board Computer
- 1K-byte RAM, 3K-byte ROM, and two spare 1K-byte 8708 EPROM memories
- 24 programmable parallel I/O (TTL) lines, including two 8-bit ports, fully implemented switches and displays, and two programmable serial I/O ports interfacing directly with most terminals

110 or 230V AC power requirement

PROM Programmer for UV Erasable, Electrically Reprogrammable ROMs (EPROMs):

- 8708/2708/2704 standard
- 8755 with adapter

Integral keyboard and 16-digit display (no teletypewriter or CRT terminal required)

Extensive system monitor software in ROM

Self-programmable, allowing user to add functions

Includes comprehensive design library

The Intellec PROMPT 80/85 8080/8085 Microcomputer Design Aid is a low cost, fully assembled microcomputer design aid developed to simplify the programming of iSBC 80 and System 80 microcomputers, as well as 8080/8085 processors, 8708/2708/2704/8755 EPROMs, and 8255/8251 programmable I/O devices. 8080 programs may be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing. PROMPT 80/85's iSBC 80/10 may be expanded using an iSBC modular cardcage. PROMPT 80/85 may serve as an economical 8708/8755 Specialized PROM Programmer (SPP) peripheral in Intellec microcomputer development systems.



DESIGN
AIDS

FEATURES

Prom Programmer

8708 UV Erasable, Electrically Reprogrammable ROMs (EPROMs) can be easily programmed, compared, and transferred to RAM using the zero-insertion force socket on the panel. A new technique allows 8708 to be partially programmed in multiple blocks of 16 bytes. Thus, small modular routines can be entered, tested, and readily saved using EPROM. EPROMs can also be conveniently duplicated. The master (original) device plugs into the ISBC 80/10 inside PROMPT 80 and can be copied to the panel programming socket. 8755 EPROMs can also be programmed, compared and transferred over any address range using the optional adaptor PROMPT 875.

Register/Display Group

All 8080 registers can be displayed, even while single stepping programs. The registers are shown in three rows:

First row	B	C	D	E
Second row	H	L	Flags	A
Third row	Program counter		Stack pointer	

One register row is visible at a time. Three small LEDs to the left of these rows indicate which row is displayed. The scroll register display command displays the next row (first, second, third, etc.)

Reset, Interrupts

The system reset command (SYS RST) resets the system, initializes the PROMPT 80/85 registers, and enters the monitor. The monitor interrupt command (MON INT) interrupts a user program and enters the monitor saving the user registers. The user interrupt command (USR INT) traps PROMPT 80/85 to location 3C02₁₆.

Monitor

A comprehensive system monitor resides in three 1K ROMs. It displays, drives PROMPT's keyboard, and responds to commands and functions. The monitor is modular, organized so that the third ROM may be removed if functions are not required. This allows sizable user routines — as much as 2K ROM/EPROM and nearly 1K RAM — to be exercised.

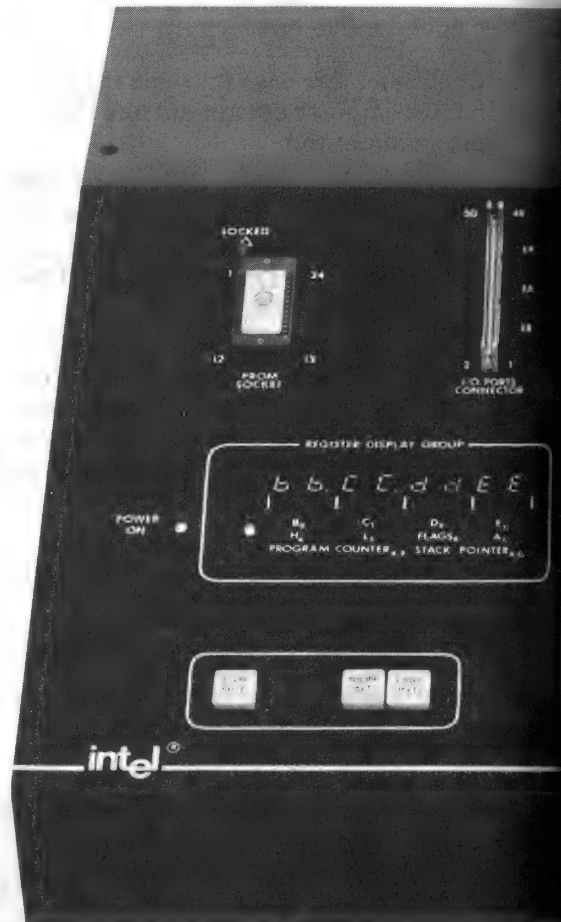
Commands

PROMPT 80/85 commands are compatible with those used by Intel's SDK ISBC, and Intellec monitors. A register command may be operated with either an examine/modify command or display/modify memory command. Then either the next or previous register and memory locations can be opened with one button. The go command executes programs, allowing multiple optional breakpoints. Or a program can be single stepped, executed one instruction at a time. The scroll register display command displays the next row of the register/display group. Commands are entered naturally, like phrases in a sentence: the next (NEXT) parameters are separated by commas and command sentences end with EXECUTE/END. The commands do what makes sense. For example:

GO ☐ 100 ☐ EXECUTE/END
starts the program at address 100.

GO ☐ 100 ☐ NEXT 200 ☐ EXECUTE/END
starts the program at 100, but stops at 200, a breakpoint.

GO ☐ ☐ EXECUTE/END
starts the program where it was last stopped.





Input/Output Group

The input/output (I/O) group features two fully implemented 8-bit ports, both with displays, and with latch switches for the input port E9. The port addresses are clearly marked E8 and E9. Those two ports and a third, at EA, are easily accessible on the I/O ports connector. Negative true logic is used throughout the I/O group and ports connector to enhance noise immunity and allow wire-ANDing.

Parallel I/O

The I/O ports connector provides easy access to 24 parallel, TTL compatible lines. These lines are addressed as three ports (each 8 lines), port E8, E9, and EA. These ports can be defined to be input or output by software. Defining control words, tabulated in "Specifications," are sent out (OUT) to port EB, the control word register.

Serial I/O

PROMPT's programmable serial I/O readily interfaces with most terminals. Jumpers select either 20 mA teletypewriter (TTY) current loop or RS232C operation, and the appropriate communications frequency. Asynchronous or synchronous transmission, data format, control characters, parity, and transmission rate can be programmed. A serial cable kit, PROMPT-SER, connects PROMPT to either a teletypewriter or RS232C standard (CRT) terminal through a rear chassis access slot. Teletypewriters may require minor reader control modifications.

Command/Function Displays

The command/function displays show addresses and data when displaying memory, and parameters for commands and functions are entered.

Functions

Eight functions are provided by PROMPT. Others may be added by the user. Pressing a hex data/functions key (0-7) starts a function as shown in Table 1.

Key	Function	Operation
0 is	F0	Read paper tape
1 is	F1	Write paper tape
2 is	F2	Program 8708 EPROM, compare
3 is	F3	Compare 8708 EPROM
4 is	F4	Transfer 8708 EPROM to RAM
5 is	F5	Move block memory
6 is	F6	Hexadecimal calculator, +, -
7 is	F7	Byte search memory, optional mask
8 is	F8	Word search memory, optional mask
9 is	F9	Program 8755 EPROM, compare
A is	FA	Compare 8755 EPROM
B is	FB	Transfer 8755 EPROM

Table 1. PROMPT 80/85 Functions

FUNCTIONAL DESCRIPTION

PROMPT is a low cost programming tool. It is a micro-computer design aid — not a development system with sophisticated software and peripherals. Intellec PROMPT 80/80 simplifies the programming of 8080/8085 processors and ISBC 80 and System 80 microcomputers, as well as 8708/8755 EPROMs and 8255/8251 programmable I/O devices. The heart of PROMPT 80/85 is the popular ISBC 80/10 Single Board Computer, a complete computer on a single printed circuit board. The ISBC 80/10 includes an 8080A, 1K bytes of static RAM memory, and sockets for 4K bytes of EPROM memory. Signals to the ISBC 80/10 include 48 programmable, parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable serial channel, a multi-source single level interrupt network, and bus

drivers for memory and I/O expansion. Read only memory may be added in 1K-byte increments using Intel 8708 EPROMs or 8308 ROMs. A block diagram of the PROMPT 80/85 is shown in Figure 1.

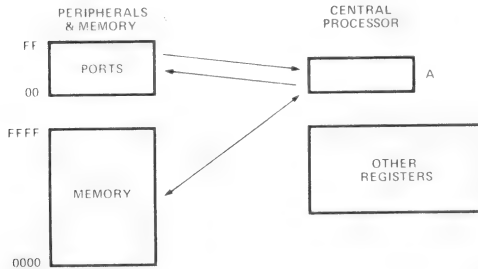


Figure 1. PROMPT 80/85 Block Diagram

8080A Processor

The central processor for PROMPT's iSBC 80/10 is Intel's powerful 8-bit n-channel MOS 8080A CPU. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

Addressing

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located anywhere in read/write memory, may be used as a last-in/first-out store. The contents of the program counter, accumulator, flags, and all of the general purpose registers are stacked using a 16-bit pointer. Subroutine nesting is bounded only by memory size.

Programming

PROMPT encourages the preparation and verification of small, modular routines which together may comprise sizable programs. These are written in assembly language, then entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Many 8080 operations can be specified with only two strokes. Once entered, programs can be exercised one instruction (single step) or many instructions at a time. And, any of the 8080 registers can be watched while single stepping.

Memory

Programs are readily saved and instantly reloaded via UV Erasable, Electrically Reprogrammable ROMs (EPROMs). PROMPT 80/85 can program the popular 8708 EPROMs in small blocks, so routines can be debugged and saved incrementally. Several programs are prerecorded as examples on PROMPT's spare 8708 EPROMs.

Interface

PROMPT 80/85 is a complete, fully assembled and powered 8080 microcomputer, including RAM, I/O, and system monitor in ROM. Twenty-four lines of programmable, TTL-compatible, parallel I/O are easily accessed

on a panel connector. Two 8-bit ports are fully implemented, one with displays for output, the other with displays and switches for input. PROMPT's programmable serial I/O interfaces directly with most terminals. A teletypewriter or CRT can be used, but neither is required because of PROMPT's built-in keyboard and display.

Optional Expansion

PROMPT 80/80's iSBC 80/10 may be expanded via the iSBC 604 Modular Cardcage as shown in Figure 2. The cardcage houses the iSBC 80/10 and up to three expansion boards. Memory and I/O can be added in various combinations. Additional power may be required.

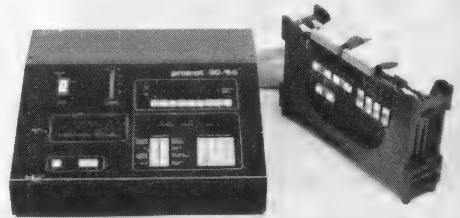


Figure 2. PROMPT 80/85 Expanded with iSBC 604 Modular Cardcage

Applications

A Specialized PROM Programmer kit, the PROMPT-SPP, allows PROMPT 80/85 to serve as an economical 8708/8755 Specialized PROM Programmer peripheral in Intel microcomputer development systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intel Microcomputer Development System, as shown in Figure 3.



Figure 3. PROMPT 80/85 Used as an Intel Microcomputer Development System Peripheral

Documentation

The PROMPT 80/85 manual includes chapters for the reader with little or no programming experience. Topics treated range from the number system to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPS — simplify microcomputer concepts. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and applications notes, make Intellec PROMPT 80/85 ideal for the newcomer to microcomputing.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Timing

Basic Instruction — 1.95 μ s

Cycle Time — $t_{CY} = 488 \mu$ s

Clock — 2.058 MHz $\pm 0.1\%$

Memory Bytes

Up to 48K bytes may be added using optional RAM, ROM, or PROM expansion boards and the ISBC 604 Cardcage.

Memory	Addressing	On Board	Monitor Uses
ROM/PROM	0-0FFF ₁₆	4096	2048 or 3072
RAM	3C00-3FFF ₁₆	1024	114

I/O Addressing

Ports E4 to E7 are dedicated to PROMPT's display/key-board groups. Ports E8 to EB drive the panel I/O ports connector and PROM socket.

Dedicated to Display/Keyboard					I/O Ports Connector PROM Socket				Serial I/O USART	
	A	B	C	Control	A	B	C	Control	Data	Control
Port	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED

Parallel I/O

The panel I/O ports can be defined input or output by outputting control words to port address EB.

HEX Control Word (OUT this to EB)	Port E8 Bits 7-0	Port E9 Bits 7-0	Port EA	
			Bits 7-4	Bits 3-0
80	Output	Output	Output	Output
81	Output	Output	Output	Input
82	Output	Input	Output	Output
83	Output	Input	Output	Input
84 or 85	Output	Strobed output	Output	Bits 2, 1, 0 are strobes
86 or 8	Output	Strobed input	Output	

All input ports are TTL compatible. Ports E8 and EA are one-load fully TTL compatible as output. Port E9 is ordinarily used as input. When used as output, E9 can sink at least one low power TTL load.

Serial I/O

The serial I/O port is defined by software and jumper. PROMPT is configured at the factory for 20 mA current loop TTY interface, but can easily be jumpered for RS-232C levels. Asynchronous or synchronous transmission, data format, control characters, parity, and transmission rate can be programmed.

Interrupts

PROMPT 80/85 provides a panel user interrupt to 3C02₁₆. The ISBC 80/10 supports single level vectoring to location 38₁₆. Request may originate from user specified I/O (2), the parallel ports (2), or serial port (2).

EPROM Programming

8708/2708/2704 EPROMs can be programmed in multiple blocks of 16 bytes. Starting and ending memory address need only differ by a multiple of 16, and starting EPROM address and XX0 hexadecimal (X = don't care). Programming time is 115 sec for 1K byte, 3 sec for 16 bytes. 8755 EPROMs can be programmed at any addresses using the optional PROMPT 875 adaptor. Programming time is 52 sec for 1 K byte. EPROMs may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (UV intensity \times exposure time) is 10W-sec/cm².

System Monitor

Resides in three 8308 ROMs, 0 to 3FF₁₆, 400₁₆ to 7FF₁₆ and 800₁₆ to BFF₁₆. The third ROM implements F functions and can be removed. PROMPT has an unused ROM/EPROM socket at address C00₁₆ to FFF₁₆.

Commands

Examine/modify register

Go (with optional breakpoints)

Scroll register display

Next ☐

Display/modify memory

Single step

Open previous/clear entry

☐ Execute/end

Functions

☐ Read tape

☐ Write tape

☐ Program 8708, compare

☐ Compare 8708

☐ Transfer 8708 to RAM

☐ Move block memory

☐ Hexadecimal calculator, +, -

☐ Byte search memory, optional mask

☐ Word search memory, optional mask

With 875 adaptor

☐ Program 8755, compare

☐ Compare 8755

☐ Transfer 8755

Software Drivers

Panel keyboard input

Console terminal input

TTY reader input

Panel display output

Console terminal output

TTY punch output

Connectors

PROMPT panel I/O ports

ISBC 80/10 parallel I/O

ISBC 80/10 serial I/O

ISBC 80/10 bus

ISBC 80/10 auxiliary bus

3M 3425 flat

3M 3415 flat

3M 3462 flat

CDC VPB01E43D00A1

TI H312130

Equipment Supplied

PROMPT 80/85 — Mainframe with ISBC 80/10, display/keyboard

PROM — Programmer, power supply, cabinet, and ROM-based system monitor.

8708 EPROMs — 2 each, with pre-recorded example programs

110V AC power cable — 110 or 220V AC fuse

Compatible Equipment

PROMPT-875 Optional 8755 programming adaptor.

PROMPT-SER Serial cable connects PROMPT to TTY, CRT.

PROMPT-SPP Specialized PROM programmer kit connects PROMPT 80/85 to Intellec micro-computer development systems for 8708/8755 EPROM programming.

Physical Characteristics

Height — 5.3 in. (13.5 cm) max

Width — 17 in. (43.2 cm)

Depth — 17 in. (43.2 cm) max

Weight — 21 lb. (9.6 kg)

Electrical Characteristics

Either 115 or 230V AC ($\pm 10\%$) may be switch selected on the mainframe. 1.8 amps max current (at 125V AC). Frequency is 47-63 Hz. Fixed over-voltage protect on 5V supply 6.2-6.7 volts.

AC Power Requirements

Voltage	Internal PROMPT 80/85 Supply	PROMPT 80/85 Requires
+26.5	0.1A	0.03A
+12	1.2A	0.5A
+5	6.0A	5.0A
-5	0.3A	0.1A
-12	0.3A	0.2A

Environmental Characteristics

Operating Temperature — 10°C to +40°C

Non-Operating Temperature — 20°C to +65°C

Reference Manuals

9800307 — Intellec PROMPT 80/85 User's Manual (SUPPLIED)

9800452 — 8080/8085 Floating-Point Arithmetic Library User's Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800316 — System 80/10 Reference Manual (SUPPLIED)
Design Library of Application Notes, Article Reprints (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

PROMPT-80 or Intellec PROMPT 80/85 MCS80/85
PROMPT-80-220V Micro-Computer Design Aid. Complete with ISBC 80/10 Single Board Computer (8080 CPU), integral keyboard, displays, and EPROM programmer.



INTELLEC PROMPT 48 MCS-48 MICROCOMPUTER DESIGN AID

Complete low cost design aid and EPROM programmer for revolutionary MCS-48 single component computers

Simplifies microcomputing, allowing user to enter, run, debug, and save machine language programs with calculator-like ease

Utilizes two removable 8-bit MCS-48 CPUs

- 8748 CPU with erasable, reprogrammable on-chip program memory
- 8035 CPU with off-chip program memory

1K-byte erasable, reprogrammable on-chip (8748), expandable program memory, 1K-byte RAM in PROMPT system

64 bytes RAM on-chip, expandable register memory

The Intellec Prompt 48 MCS-48 Microcomputer Design Aid is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs may be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing. PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1K bytes provided internally. PROMPT 48 can serve as an economical 8748 Specialized PROM Programmer (SPP) peripheral in Intellec microcomputer development systems.

256 bytes expandable RAM data memory in PROMPT system

27 on-chip TTL compatible expandable I/O lines

On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack control

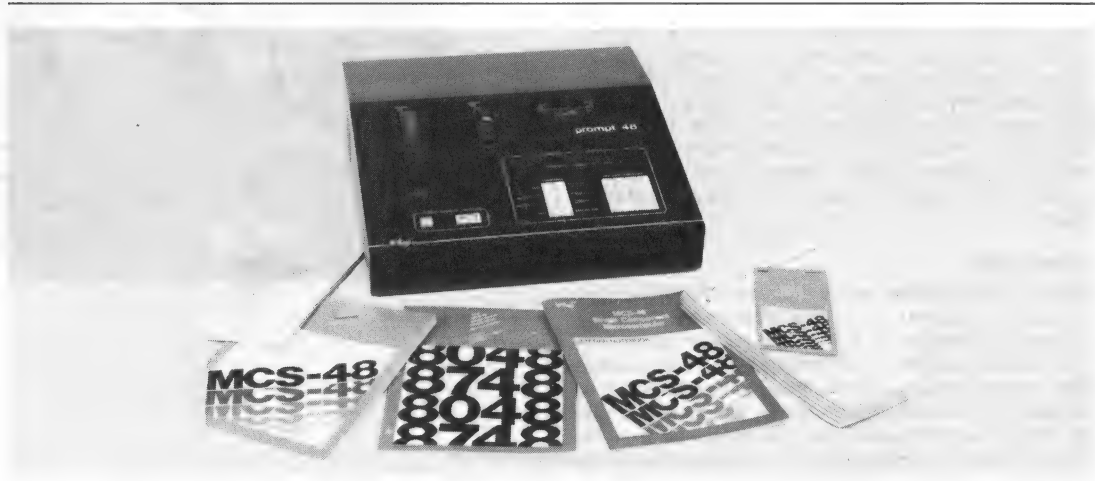
Single +5V DC system power requirement

Integral keyboard and displays (no teletypewriter or CRT terminal required)

Extensive PROMPT 48 monitor, allowing system I/O, bus, and memory expansion

Compatible with Intellec microcomputer development systems

Includes comprehensive design library



DESIGN
AIDS

FEATURES

Single Component Computer

The 8748 is the first microcomputer fully integrated on one component. All elements of a computing system are provided, including CPU, RAM, I/O, timer, interrupts, and erasable, reprogrammable nonvolatile program memory.

Programming Socket

PROMPT's programming socket programs this revolutionary "smart PROM" — the 8748 — in a highly reliable, convenient manner. A fail-safe interlock ensures the device is properly inserted before applying programming pulses. Each location may be individually programmed, one byte at a time. A read-before-write programming algorithm prevents device damage by inadvertently programming unerased memory.

MCS-48 Processors

The execution socket accepts either an 8035 or an 8748 MCS-48 processor. Both are supplied with each PROMPT 48, and either can serve as heart of the PROMPT system. There are no processors within the PROMPT 48 mainframe, which instead contains monitor ROM and RAM, user RAM, peripherals, drivers, and sophisticated control circuitry. Once a processor is seated in the execution socket and power is applied, the PROMPT system comes to life. Various access modes may be selected such as program execution from PROMPT system RAM, or from on-chip PROM. Thus programs may first be executed from PROMPT RAM with the 8035 processor. When debugging is complete, the 8035 (execution socket) processor can program the 8748 (programming socket) processor. Finally, a programmed 8748 processor may be exercised by itself from the execution socket. The execution socket processor runs either monitor or user programs.

System Monitor

The system reset command initializes the PROMPT system and enters the monitor. The monitor interrupt command exits a user program gracefully, preserving system status and entering the monitor. The user interrupt command causes an interrupt only if the PROMPT system is running a user program. A comprehensive system monitor resides in four 1K-byte read only memories. It drives the PROMPT keyboard and displays and responds to commands and functions. The top 16 bytes of on-chip program memory must be used by the PROMPT system to switch between monitor and user programs. It requires one level of the MCS-48 eight-level stack.

Commands

PROMPT 48's commands are grouped and color-coded to simplify access to the 8748's separate program and data memory. Registers, data memory, or program memory, may be examined and modified with the examine and modify commands. Then either the next or previous register and memory locations may be accessed with one keystroke. Programs may be exercised in three modes. The go no break (GO NO BREAK) runs in real time. The go with break (GO WITH BREAK) mode is not

real time — after each instruction the MCS-48 program counter is compared against pending breakpoints. If no break is encountered, execution resumes. The go single step (GO SINGLE STEP) mode exercises one instruction at a time. Commands are like sentences, with parameters separated by ☐ NEXT. Each command ends with ☐ EXECUTE/END. In addition to the PROMPT basic commands, thirteen functions simplify programming. Each is started merely by pressing a hex data/function key and entering parameters as required, as shown in Table 1.



Cable Interface

An optional cable, PROMPT-SER, directly connects the PROMPT system to virtually any terminal via a rear access slot. Another cable, PROMPT-SPP, allows programs and data to be downloaded from the Intellec microcomputer development system to the PROMPT system for debugging.



Key	Function	Operation
[2]	Port 2 map	Allows specification of direction of each pin on port 2. Port 2 is multiplexed to address external program memory and expand I/O. Thus it must be buffered; the P2 map command establishes the direction of buffering.
[3]	Program EPROM	Programs 8748 EPROMs.
[4]	Byte search (with optional mask)	Sweeps through register, data, or program memory searching for byte matches. Starting and ending memory addresses are specified.
[5]	Word search (with optional mask)	Sweeps through register, data, or program memory searching for word matches. Starting and ending memory addresses are specified.
[6]	Hex calculator	Computes hexadecimal sums and differences.
[7]	8748 program for debug	Similar to program EPROM, but ensures that the top of program memory contains monitor re-entry code for debugging.
[8]	Compare	Verifies any portions of EPROM program memory against PROMPT memory.
[9]	Move memory	Allows blocks of register, data, or program memory to be moved.
[A]	Access	Specifies one of six access modes for PROMPT 48. For example EPROM, PROMPT RAM, or external program memory, and a variety of input/output options may be selected.
[B]	Breakpoint	Allows any or all of the eight breakpoints to be set and cleared.
[C]	Clear	Clears portions of register, data, or program memory.
[D]	Dump	Dumps register, data, or program memory to PROMPT's serial channel: for example, a teletypewriter paper tape punch.
[E]	Enter	Enters (reads) register, data, or program memory from PROMPT's serial channel.
[F]	Fetch	Fetches programs from EPROM to PROMPT RAM.

Table 1. PROMPT 48 Commands and Functions

Access

Easy access to the pins of the executing processor is provided via the I/O ports and bus connector. Only the EA external access, SS single step, and X1, X2 clock inputs are reserved for the PROMPT system.

Expansion

Program or data memory may be expanded beyond that provided on-chip or in the PROMPT system. I/O ports may be expanded, as with the 8243, or peripheral controllers may be memory-mapped. The I/O ports and Bus connector allows the execution socket processor to be directly interfaced to prototype systems, yet be controlled from the PROMPT panel.

Control

The command/function group panel keyboard and displays completely control PROMPT 48 — a teletypewriter or CRT terminal is not needed. A hyphen prompting character appears whenever a command or function can be entered. Addresses and data are shown whenever examining registers and memory. Parameters for commands and functions are also shown.

FUNCTIONAL DESCRIPTION

"PROMPT" stands for PROgramMING Tool. It is a programmer for 8748 EPROMs, and a versatile aid for debugging MCS-48 programs. Programs can be entered via its integral panel keyboard, programming socket, or serial channel. Almost any terminal can be interfaced to the serial channel, including a teletypewriter, CRT, or an Inteltec microcomputer development system. Inteltec PROMPT 48 simplifies the programming of MCS-48 systems. Like the 8748 it is radically new, highly integrated, and expandable. Like the MCS-48 family, it is low cost, and ideal for small applications and programs. It is a design aid, not a development system with sophisticated software and peripherals.

MCS-48 Processors

PROMPT 48 comes complete with two of Intel's revolutionary MCS-48 processors: an 8748-4 Single Component 8-Bit Microcomputer and an 8035-4 Single Component 8-Bit Microcomputer. Advances in n-channel MOS technology allow Intel, for the first time to integrate into one 40-pin component all computer functions:

8-bit CPU

1K x 8-bit EPROM/ROM program memory

64 x 8-bit RAM data memory

27 input/output lines

8-bit timer/event counter

Performance — More than 90 instructions — each one or two cycles — make the single chip MCS-48 equal in performance to most multi-chip microprocessors. The MCS-48 is an efficient controller and arithmetic processor, with extensive bit handling, binary, and BCD arithmetic instructions. These are encoded for minimum program length; 70% are single byte operation codes, and none is more than two bytes.

Flexibility — Three interchangeable, pin-compatible devices offer flexibility and low cost in development and production, as follows:

8748 — with user-programmable and erasable EPROM program memory for prototype and pre-productions systems.

8048 — with factory-programmed mask ROM memory for low-cost, high volume production.

8035 — without program memory, for use with external program memories.

Circuitry — Each MCS-48 processor operates on a single +5V supply, with internal oscillator and clock driver, and circuitry for interrupts and resets. Extra circuitry is in the 8048 ROM processor to allow low power standby operation. The 64 x 8 RAM data memory can be independently powered.

Compatibility — For systems requiring additional compatibility, the MCS-48 can be expanded with the new 8243 I/O expander, 8155 I/O and 256-byte RAM, 8755 I/O and 2K-byte EPROM, or 8355 I/O and 2K ROM devices. MCS-48 processors readily interface to MCS-80/85 peripherals and standard memories.

Memory Capacity

PROMPT 48 is a complete, fully assembled and powered microcomputer system including program memory, data

memory, I/O, and system monitor beyond that available on MCS-48 single component computers. 1K bytes of PROMPT system RAM serve as "writable program memory" — a ROM simulator for the program memory on each MCS-48 computer. 256 bytes of PROMPT system RAM serve as "external data memory," beyond the 64 register bytes on each MCS-48 computer. Users may further expand program or data memory via the panel I/O ports and bus connector.

Programming

Programs written first in assembly language, are entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Most MCS-48 operations can be specified with only two keystrokes. Once entered, routines can be exercised one instruction (single step) or many instructions at a time. The principal MCS-48 register — the accumulator — is displayed while single stepping. Programs can be executed in real time (GO NO BREAK) or with as many as eight different breakpoints (GO WITH BREAK).

Control

PROMPT 48 can be fully controlled either by the panel keyboard and displays, or remotely by a serial channel. Thus a teletypewriter or CRT can be used but neither is required. Full remote control by a serial channel means users can download and debug programs using the PROMPT 48 together with an Inteltec microcomputer development system.

Access

The PROMPT panel I/O ports and bus connector allow easy access to all MCS-48 pins except those reserved for control by the PROMPT system, namely EA external access, SS single step, and X1, X2 clock inputs.

Optional Expansion

PROMPT 48 may be expanded beyond the resources on both the MCS-48 single component computer and the PROMPT system. External program and data memory may be interfaced and input/output ports added with the 8243 I/O expander.

Applications

A specialized PROM Programmer Kit, the PROMPT-SPP, allows PROMPT 48 to serve as an economical 8748 Specialized PROM Programmer peripheral in Inteltec microcomputer development systems. The PROMPT-SPP cable plugs directly into the rear panel of the Inteltec microcomputer development system, as shown in Figure 1.

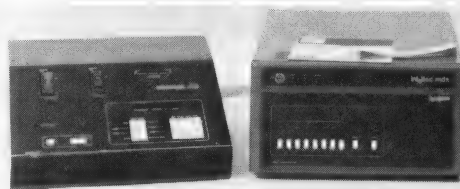


Figure 1. PROMPT 48 used as an Inteltec Microcomputer Development System Peripheral

Documentation

The PROMPT 48 manual includes chapters for the reader with little or no programming experience. Topics treated range from number systems to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPS — simplify microcomputer

concepts. PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and application notes, make the Intellec PROMPT 48 ideal for the newcomer to microcomputing.

SPECIFICATIONS

Timing

Basic Instruction — 2.5 μ s
Cycle Time — $t_{CY} = 2.5 \mu$ s
Clock — 6 MHz \pm 0.1%

Memory Bytes

The 8748 contains 64 bytes of register memory, no external data memory, and 1024 bytes of RAM program memory. The PROMPT system provides 256 bytes of external data memory, and 1024 bytes of RAM program memory. PROMPT RAM program memory can be used in place of the on-chip EPROM program memory; thus programs less than 1024 bytes may be designed. For larger programs additional memory can be directly interfaced to the MCS-48 bus via the PROMPT panel I/O ports and bus connector.

Memory Configuration

Memory	Maximum	On Chip	In PROMPT 48
Register	64	64	0
Data	3328	0	256
Program	4096	1024 EPROM	1024 RAM

I/O Ports

All MCS-48 I/O ports are accessible on the PROMPT panel connector.

Bus — A true bidirectional 8-bit port with associated strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or a non-latching input port. Input and output lines cannot be mixed.

Ports 1 and 2 — Data written to these 8-bit ports is latched and remains unchanged until written. As inputs these lines are not latching. The lines of ports 1 and 2 are called quasibidirectional. A special output structure allows each line of port 1 and half of port 2 to serve as an input, an output, or both. Any mix of input, output, and both lines is allowed.

T0, T1, and INT — Three pins that can serve as inputs. T0 can be designated as a clock output. Input/output can be expanded via the PROMPT panel connector with a special I/O expander (8243) or standard peripherals.

Reset and Interrupts

Reset — Initializes the PROMPT system and enters the monitor.

Monitor Interrupt — exits a user program gracefully, preserving system status and entering the monitor.

User Interrupt — causes an interrupt only if the PROMPT system is running a user program.

The processor traps to location 3₁₆. The MCS-48 timer/event counter is not used by the PROMPT system and is available to the user. Either timer flag or interrupt will signal when overflow has occurred. The timer interrupt can be used only in the go-no-break (real time) mode.

EPROM Programming

PROMPT 48 provides a programming socket to directly program 8748s. Programs are loaded into the PROMPT RAM program memory via keyboard. EPROM, teletype-writer, or other serial interface. A fail-safe interlock ensures programming pulses are applied only if the device is properly inserted. Inadvertent reprogramming is prevented by a read-before-write programming algorithm. Each location may be individually programmed, one byte at a time.

Panel I/O Ports and Bus Connectors

All MCS-48 pins, except five, are accessible on the I/O ports and bus connector. The five reserved for PROMPT system control are EA external access, SS single step, X1, X2 crystal inputs, and 5V. Due to internal buffering of the MCS-48 bus, access times will be negligibly degraded by the PROMPT system. Since MCS-48 processors do not communicate internal address gate status, bus data must be driven out if neither PSEN nor RD is asserted.

System Devices

Both user programs and the PROMPT monitor enjoy access to system devices: serial I/O, panel displays, and keyboard. These are memory-mapped to program memory addresses beyond 2K.

Serial I/O — The serial I/O port (data 820₁₆, control 821₁₆) is defined by software and jumpers for 110 baud, 20 mA current loop, but can easily be jumpered for other baud rates and RS232C levels. Asynchronous or synchronous transmission, data format, control characters, and parity can be programmed.

Panel Displays — Eight display ports (data 810-817₁₆) allow each of the panel displays to be written from user programs. Data written on a display device will time out after a fixed interval. Displays must be refreshed on a polled or interrupt-driven basis. User programs can call software drivers which provide this capability.

Keyboard — Software is used to debounce the panel keyboard (data 810₁₆). The monitor's input routines (see Software Drivers) provide this debouncing and can be called from user programs.

Commands

Single step }
With break } Go
No break }

Examine/modify { Register } Memory
 { Data }
 { Program }

Open previous/clear/entry ☐ Next ☐ Execute/End

Functions

- 2 Port 2 map
- 3 Program EPROM (8748)
- 4 Search (R, D or P)* memory for 1 byte, optional mask
- 5 Search (R, D or P) memory for 2 bytes, optional mask
- 6 Hexadecimal calculator +, -
- 7 8748 program EPROM for debug
- 8 Compare EPROM with memory
- 9 Move memory (R, D or P)
- A Access
- B Breakpoint
- C Clear memory (R, D or P)
- D Dump memory (R, D or P)
- E Enter (read) memory (R, D or P)
- F Fetch EPROM program memory

Note

*R, D, or P is register, data, or program.

Software Drivers

Panel Keyboard In — KBIN, KDBIN

Panel Display Out — DGS6, DGOUT, HXOUT, BLK, REFS, ENREF

Serial Channel — CI, CO, RI, PO, CSTS

Connectors

Serial I/O — 3M 3462-0001 Flat Crimp/AMP 88106-1 Flat Crimp/ TI H312113 Solder/AMP 1-583485-5 Solder.

Panel I/O Ports and Bus Connector — 3M 3425 Flat Crimp. A complete cable set including wirewrap header for prototyping is included with each PROMPT.

Equipment Supplied

PROMPT 48 mainframe with two MCS-48 processors (8748, 8035), display/keyboard, EPROM programmer, power supply, cabinet, and ROM-based monitor.

110 V AC power cable

110 or 220 V AC

Fuse

Panel I/O ports

Bus connector cable set

Physical Characteristics

Height — 5.3 in. (13.5 cm) max

Width — 17 in. (43.2 cm)

Depth — 17 in. (43.2 cm) max

Weight — 21 lb. (9.6 kg)

Electrical Characteristics

Power Requirements — either 115 or 230V AC ($\pm 10\%$) may be switch selected on the mainframe. 1.8 amps max current (at 125 V AC).

Frequency — 47-63 Hz

Environmental Characteristics

Operating Temperature — 0°C to +40°C

Non-Operating Temperature — 20°C to +65°C

Reference Manuals

9800402 — Intellec PROMPT 48 User's Manual (SUPPLIED)

9800270 — MCS-48 User's Manual (SUPPLIED)

9800255 — MCS-48 and UPI-41 Assembly Language Programming Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

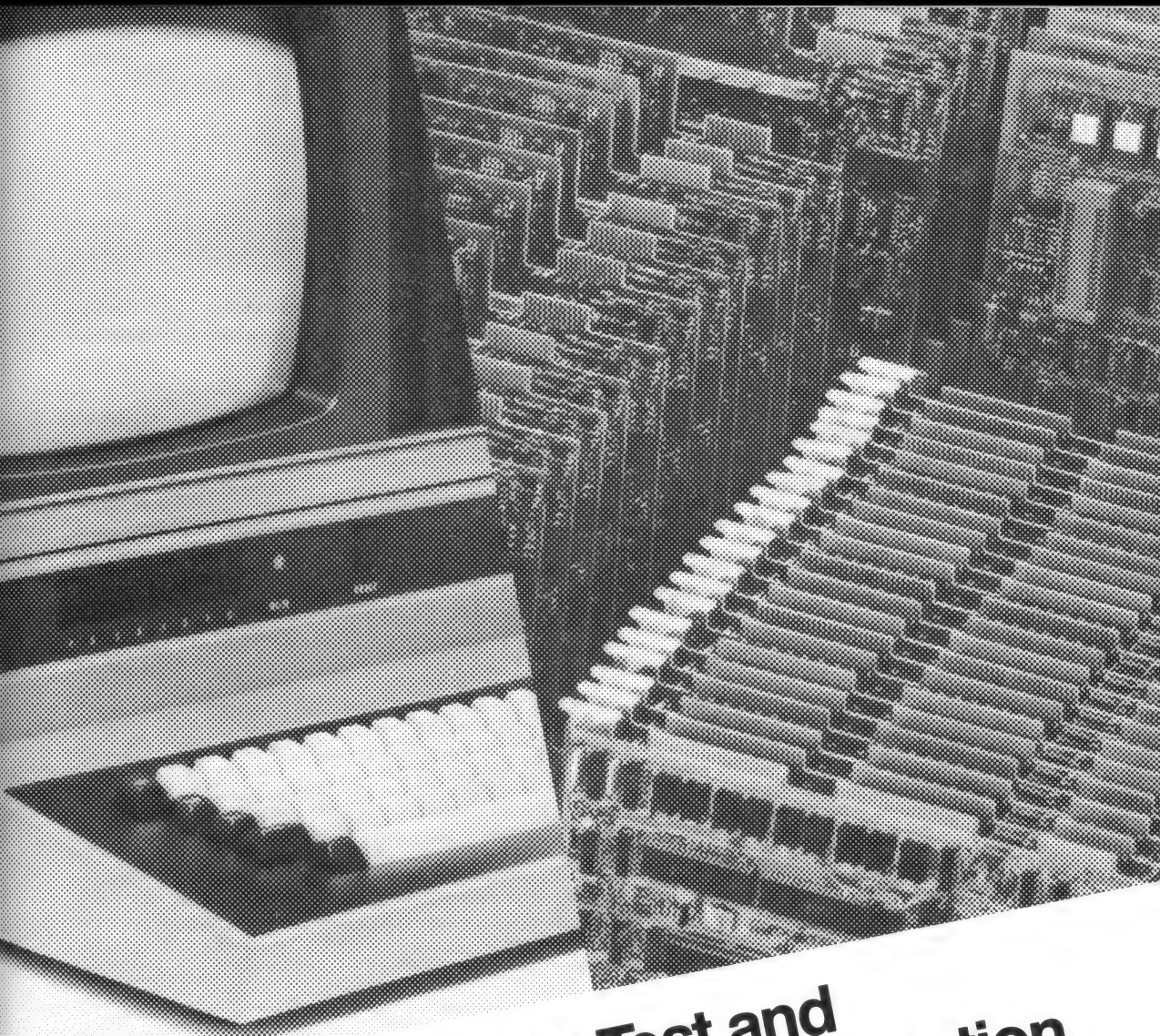
ORDERING INFORMATION

Part Number Description

PROMPT-48 or
PROMPT-48-220V Intellec PROMPT 48 MCS-48 micro-computer design aid. Complete with two MCS-48 processors (8748 and 8305), EPROM programmer, integral keyboard, displays, and system monitor in ROM

PROMPT-SER Serial cable for connecting PROMPT to TTY, CRT

PROMPT-SPP Specialized PROM programmer kit for connecting PROMPT 48 to Intellec microcomputer development systems for EPROM programming



12 Test and Instrumentation Systems

TEST AND INSTRUMENTATION SYSTEMS

INTRODUCTION

This section provides information on Intel's new μ Scope 820 Microprocessor System Control and on the μ Scope Probe 8080A, the associated personality probe for the 8080A microprocessor. These portable test instruments may be used for maintenance and repair of microprocessor systems, and have been specifically designed to ease the task of microcomputer system checkout for the laboratory, production line, and field technician. They also provide the more powerful analytical capabilities necessary to troubleshoot difficult problems for the more experienced, sophisticated user.

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μ Scope 820 Microprocessor System Console	12-3
μ Scope Probe 8080A	12-8



μ SCOPE 820 MICROPROCESSOR SYSTEM CONSOLE

Gives complete control over microprocessor, including single step, run-with-display, or run-real-time capability

Provides a 32-bit hardware breakpoint with bit masking and a 256-word trace memory

Executes diagnostic routines from μ Scope 820 console overlay memory

Provides an interface to microcomputer systems for troubleshooting system problems

Monitors, displays, and alters register, memory, and I/O values for system under test

Executes instrument resident software patch routines even when microcomputer system is ROM-based

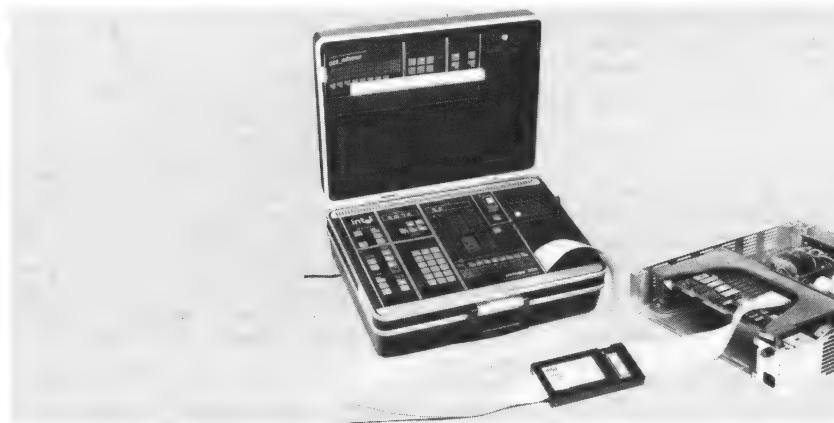
Is a stand-alone, self-contained, rugged portable unit

Human engineered with easy to read 9-segment hexadecimal displays and extensive operator prompting

Designed to support many different microprocessors

Has built-in, self-test operation

Intel's new μ SCOPE 820 Microprocessor System Console provides equipment manufacturers with a portable microcomputer system designed to expedite troubleshooting and maintenance of other microcomputer systems. The unit can control and examine system operations. Diagnostics can be automated by EPROM (erasable, programmable read only memories) or ROMs into the socket at the upper left of the keyboard display panel. The μ Scope 820 is a portable, self-contained instrument designed to provide the control, monitoring, and interaction necessary to effectively and quickly evaluate and debug 8-bit microcomputer-based systems in the lab, on the production line, or in the field. Connection to the user's system is through a personality probe plugged into the microprocessor socket. Each personality probe is unique to each microprocessor type. The instrument features many different operating and control modes, allowing the operator to carry out a number of functional checks on the microcomputer system under test (SUT). Although the unit has been specifically designed to ease the task of microcomputer system checkout for the lab, production line, and field technician, it also provides the more powerful analytical capabilities necessary to troubleshoot difficult problems by the more experienced, sophisticated user. Preprogrammed test routines resident in front panel PROMs, dedicated high level commands keys, visual prompting, and simplified data entry sequences all ease the checkout of microcomputer hardware. For more rigorous diagnostic tasks, the unit provides a 32-bit maskable hardware breakpoint with optional course of action after a breakpoint match, a 256 x 32-bit trace memory, and a 128 x 8 overlay RAM that allows real-time entry of test routines via the μ Scope 820 keyboard.



TEST
SYSTEMS

FEATURES

CPU Control

The instrument provides complete control over the operation of the microprocessor in the system under test (SUT). The user CPU can be forced to halt, single step, reset, run real time, or run with display. All of the above CPU commands may be issued without impacting other operational parameters or diagnostic sequences previously established.

Reset/Self-Test

The reset and self-test features of the unit allow the operator to either initialize the instrument to a known state or quickly verify that the instrument is operating correctly. When the console is reset, the breakpoint and overlay memory are disabled, the display registers are cleared and the specific examine modes are aborted.

When the operator initiates the self-test of the unit, a sequence of operations take place which serve to confirm proper operation of a majority of the instrument.

Breakpoint Control

The hardware breakpoint of the instrument allows the operator to alter the normal program flow of the SUT. Breakpoint logic is implemented in hardware, thereby eliminating any throughput degradation of the SUT. All 32 bits of the breakpoint condition word are maskable in order to allow the breakpoint condition to be as specific or as general as may be desired. The occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or the recording of a single cycle of trace data. All of these options are selectable via the exam action key prior to enabling the breakpoint.

Trace Memory

The console has a full 32-bit word trace memory that records 256 cycles of SUT operation without causing any delays. The trace memory provides information about CPU operation just prior to a CPU halt or just prior to the initiation of a panel freeze via the trace display key. The operator can alternatively elect to have data recorded on all SUT microprocessor cycles or only when program execution of the SUT microprocessor generates a breakpoint match. Once the data is recorded, sequential examination of the data may be accomplished simply by depressing the exam next or exam last keys.

Overlay Memory

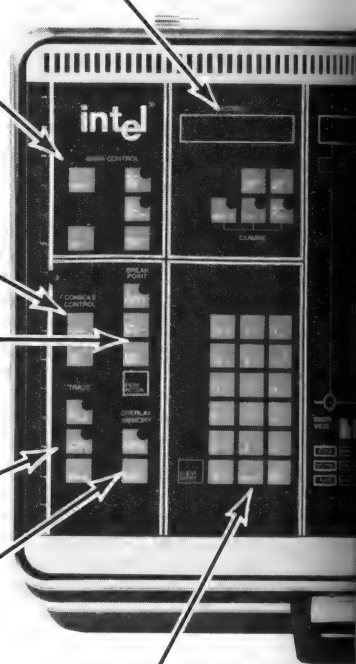
A unique feature of the unit is the ability to map its memory onto the SUT memory space. Using the overlay memory allows the operator to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. The subroutine may either be entered via the front panel hexadecimal keypad or via the front panel's ROM/PROM socket. By using the unit's overlay memory, the operator may quickly set up the SUT to execute special maintenance or troubleshooting programs to permit rapid evaluation of system operation.

Address Display/Select

A dedicated, 4-digit hexadecimal address display allows the following address information to be displayed:

- The address of any memory location.
- The I/O port number of any I/O port.
- The address of any overlay memory location.
- The address of the overlay memory origin assignment.
- The address at which the breakpoint is to occur.
- The address portion of the breakpoint mask.
- The address of the given trace record element.

An additional feature of the address display/select logic is that once the operator has initiated a given memory, trace, or I/O examination, it is possible to continue the examination in a sequential fashion either in an ascending or descending address value.



Address, Data, and Control Entry

The address, data, and control variable entry into the instrument is accomplished via the conveniently located hexadecimal keypad. For selection of the information to be displayed or modified the operator enters the hexadecimal value of the desired address, I/O port number, or label assigned to each of the registers. Once this entry is made, the operator can then elect to either continue data entry if modification is desired or press the end execute key if examination only is desired. For all data entry sequences potentially requiring multiple value entry, the μ Scope 820 Microprocessor System Console provides operator prompting to indicate the specific information expected.

Value Display/Select

The value displays provide clear and easy to use information. Together with the address display, they provide simultaneous readout of trace vectors, breakpoint conditions and breakpoint mask values, memory contents, and I/O port contents. In addition, the display allows readout of all single and double byte register values, the state of CPU pins and flags, and information regarding the course of action following the occurrence of a breakpoint, as well as information regarding the breakpoint pass count. The information displayed by the 4-digit hexadecimal value readouts is selected via the hexadecimal keypad in conjunction with any of the instrument's eleven dedicated examine keys. Further, the information is either displayed statically or is continually updated 10 times/sec if the unit is in the run-with-display mode.

As well as easy to use and understand. A plastic overlay employing membrane switch contacts provides long lasting durability as well as protection from accidental spills. Audio and tactile feedback for the membrane switches is provided for operator convenience. Ease of use of the front panel has been further enhanced by human engineering with functional grouping of switches as well as LEDs that prompt the operator during data entry sequences. Graphics have also been added to reinforce the functional switch groupings as well as data entry procedures.

PROM/ROM Socket

A front panel socket is provided for mounting 2K PROMs or ROMs that serve as storage for preprogrammed test subroutines. The actual useable program space of the PROM/ROM is 1920 bytes. The remaining 128 bytes of storage, shadowed by RAM, are used by the unit to identify up to 16 separate subroutines in the PROM/ROM and to define the specific instrument states and conditions under which the subroutine will be called. Each of the separate subroutines is uniquely enabled by the subroutine select (SUBR SELECT) key and the hex keypad.

Power Supply

The system console is complete with its own fully regulated DC power supply that provides all the DC power required by the unit itself, as well as that which is required by the associated microprocessor probe. The supply is completely self-contained, including its own AC on/off switch, line fuse, line filter, and power cord. An additional feature of the power supply is that it has been designed to permit line voltage selection in the field to facilitate operation with a wide range of AC line voltages and frequencies.

Breakpoint Action

Following the occurrence of a breakpoint match, the operator has the flexibility to execute a number of different diagnostic operations. The selection of these alternate courses of action is accomplished by pushing the exam action key and then entering the assigned value of the specific action desired via the hex keypad. Further keypad entries specify the parametric value of the action selected such as the number of breakpoint pass counts or the start address of a subroutine call following a breakpoint.

Probe Connection

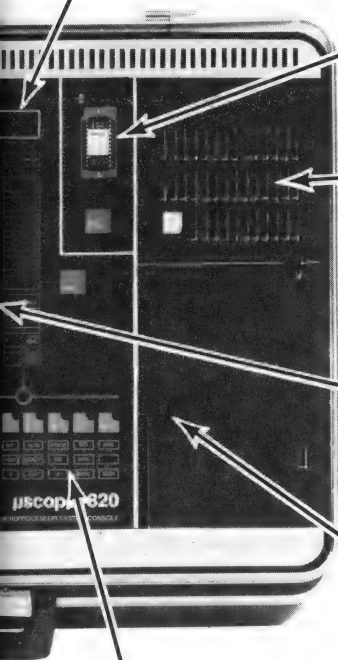
The instrument is intended to work with many of the microprocessors available today. This is accomplished by standardized interface logic which transmits and receives various address, data, and control signals between the system console and the circuitry of the particular probe. The interconnect circuitry between the instrument and probe has been designed to drive a 4-foot cable that permits convenient positioning of the panel and the SUT. In addition, a board edge connector has been provided for a personality ROM that provides front panel definition and interpretation of specific control signals for different types of microprocessors. This personality ROM is supplied with each probe kit.

Binary Data Display/Modification

All 8-bit values can be displayed in binary format on the instrument. The binary display operates in parallel with the hexadecimal display and is provided for those instances where operator recognition is enhanced by binary presentation. The selection procedure for the binary data display is identical to that for the hexadecimal value display. Once the selection has been made, the operator may alter the value by means of further hex keypad entries or by changing the binary state of any of the data bits via the eight binary data switches.

Front Panel

The front panel of the μ Scope 820 Microprocessor System Console has been designed to be rugged and



FUNCTIONAL DESCRIPTION

CPU Control

User selectable commands permit one of four possible CPU operating modes:

Run Real Time — User's CPU runs at full speed set by user clock. No wait states or cycle stealing are required.

Run with Display — User's CPU runs at full speed, except that 10 times/sec the instrument halts user's CPU temporarily to acquire display data. Worst case throughput is 95% of real time operation.

Halt — User CPU halted at next opcode fetch. DMA activity is permitted during halt.

Single Step — User CPU executes one instruction then halts.

Breakpoint Control

The breakpoint condition is set by a 32-bit word (16-bit address, 8-bit data, 8-bit status). The breakpoint mask is also set by a 32-bit word which is bit selectable. There are three courses of action following a breakpoint match:

1. Halt on first opcode fetch following breakpoint match.
2. Halt on first opcode fetch following Nth breakpoint match $1 \leq N \leq 256$.
3. Execute subroutine beginning at first opcode fetch following breakpoint match.

All breakpoint actions following a match are controlled by the breakpoint enable/disable switch except for trace recording and the sync trigger output. The sync output is a negative true TTL output occurring whenever a breakpoint match occurs.

Trace Memory

The trace memory is a 256-word memory with each word consisting of 16 address bits, 8 data bits, and 8 status bits. The memory is a circular buffer which records the last 256 cycles (words) prior to a user CPU halt or display trace command. Trace data can be recorded on all CPU cycles or only when breakpoint matches occur (independent of breakpoint enable/disable status). In addition, the operator may initiate a panel freeze to temporarily stop all trace data recording, and allow display

of previously recorded data without halting the user CPU.

Overlay Memory

The μScope 820 Microprocessor System Console allows memory read/writes of the user CPU in any assigned 1K or 2K block to be made to the instrument's overlay memory. For 1K block assignments, the first 128 bytes reside in the instrument's RAM memory while the remaining 896 bytes reside in the interchangeable front panel ROM/EPROM (either Intel's 2716 EPROM or Intel's 2316E ROM). For 2K block assignments, again the first 128 bytes are from RAM and the remaining 1920 bytes are from the front panel 2716/2316E.

Data Entry

All single and double byte items may be entered via the front panel hexadecimal keypad. In addition, all single byte items may be optionally entered via eight binary input keys.

Data Display

Eight hexadecimal 0.5 in. LEDs are provided for the simultaneous display of 4 bytes of information. The displays are physically separated into two groups. The first group displays 2 bytes of address, while the second group displays CPU data, status, single and double byte register values, or single and double byte breakpoint values. In addition, eight binary displays are used to provide quick recognition of single byte binary data patterns.

Self Test

The necessary hardware and software have been incorporated into the instrument to facilitate the self-checking of the majority of its operations. Included in these self tests are:

- Bit tests of all breakpoint condition and mask latches.
- Bit tests of all RAM.
- Verifies checksum on all operating system ROMs.
- Clears trace memory and performs bit test on trace RAM.
- Checks miscellaneous I/O ports and peripheral components
- Lights all front panel displays for user verification.

SPECIFICATIONS

Commands

Reset
Self test
CPU reset
Run real time
Run with display
Halt
Single step
Enable/disable breakpoint
Enable/disable overlay

Enable trace all cycles
Enable trace at breakpoint
Examine/modify value

- Single registers
- Double registers
- CPU states
- Breakpoint pass count

Examine/modify memory
Examine/modify I/O
Examine/modify overlay memory
Examine/modify next location
Examine/modify last location

Examine/modify breakpoint condition
Examine/modify breakpoint mask
Examine/modify breakpoint action
Examine/modify overlay origin
Display trace data
Clear entry
Continue
End/execute
Subroutine select

Connection

Four external connections to the μScope 820 Microprocessor System Console are provided:

1.2m (4 ft), 50 conductor flat cable — for connection to the microprocessor probe

20-pin board edge connector — for the probe personality PROM

24-pin zero force insertion sockets — for overlay EPROM/ROM

Recessed pin — for breakpoint sync output

Breakpoint

Pulse Width — 180 ns typ

Output High — 2.5V min, — 1.2 mA

Output Low — 0.5V max, 24.0 mA

Physical Characteristics

Width — 18-7/8 in. (479 mm)

Length — 15-1/2 in. (394 mm)

Height (top closed) — 6-5/8 in. (168 mm)
Height (top removed) — 4-5/8 in. (117 mm)
Weight — 20 lb (9.1 kg)

Electrical Characteristics

Voltage — 100, 120, 220, 240 — 10% + 5%, 110V AC max
Frequency — 48-63 Hz

Environmental Characteristics

Operating Temperature — 0°C to 55°C (32°F to 130°F)

Storage Temperature — -40°C to 75°C (-40°F to 167°F)

Humidity — 95% RH, 15°C to 40°C (59°F to 104°F) non-condensing

Accessories Supplied

Two keys

One fuse for 220/240V operation

One 2.3m (7.5 ft) power cord

Reference Manuals

9800526A — μScope 820 Operator's Handbook (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION**Part Number Description**

USC-820 Microprocessor system console



μ SCOPE PROBE 8080A

Provides interconnection for 8080A microprocessor-based systems to μ Scope 820 Microprocessor System Console

Provides complete control over system under test (SUT), yet causes minimal interference with SUT operation

Comes complete with cable, buffer box, personality ROM, and μ Scope 820 system console overlay

Fits securely in console carrying case during transit

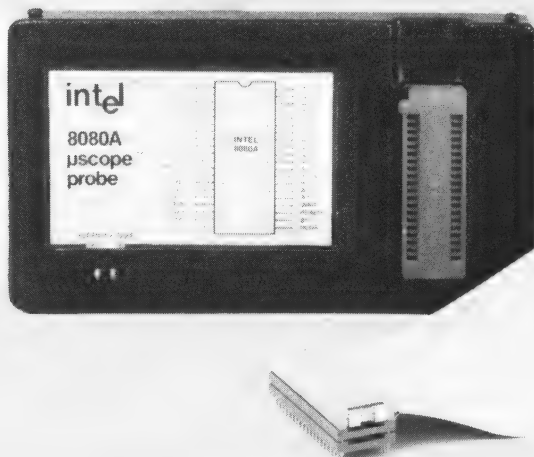
Provides complete protection for plug pins during transit

Connects via 4-foot cable to μ Scope 820 console

Has user system interconnect cable with integral ground plane for low noise operation

Operates over broad range of environmental conditions

The μ Scope Probe 8080A provides the μ Scope Microprocessor System Console with the ability to interact with 8080A microcomputer-based systems. The purpose of the probe is to interface the μ Scope 820 console to the CPU of the system under test (SUT). All of the interface signals and the associated circuitry have been designed to be effectively transparent to the SUT. CPU data, address, and clock lines are sensed by the probe 8080A, with only the CPU ground lines being switched. In addition, all SUT loading and timing degradations have been minimized by specially designed buffer circuitry. The mechanical design of the probe is compact, rugged, and allows proper operation of the probe and the console over the full ambient range specified. The buffer circuitry and the ground plane design of the interconnect cable provide low noise electrical signals while allowing the SUT to be four feet from the system console.



SPECIFICATIONS

μ Scope 820 Console Configuration

Several features of the console are directly determined by the probe being used with it. The instrument features that are determined by the 8080A interface probe are:

Single Registers — A, B, C, D, E, H, L

Double Registers — BC, DE, HL, PC, SP

CPU States — Flags, CPU pins (SYNC, RESET, HLDA, HOLD, READY, INT, INTE)

Trace/Breakpoint Word Size — 32 bits with 16 bits of address, 8 bits of data, and 8 bits of CPU status.

μ Scope 820 Console Interconnect

The probe interconnection to the μ Scope 820 console is accomplished via a 4-foot (1.2m) flat cable. 50-pin mating connectors plug into a board edge connector in the power cord compartment of the instrument and into a flat cable connector on the buffer box.

System Under Test (SUT) Interconnect

Interconnection from the buffer box to the SUT is accomplished with a 16-inch (406 mm) flat cable, complete with an integral ground plane, which is terminated with a low profile 40-pin DIP connector. The DIP connector is inserted into the SUT 8080A socket and the 8080A itself is plugged into the 40-pin socket provided on the probe buffer box.

Connections

Three external connections to the probe are provided:
50-pin flat cable connector on buffer box
40-pin zero insertion socket for the 8080A
40-pin low profile replaceable IC DIP connector for connection to SUT

Accessories Supplied

One μ Scope 820 system console overlay
One personality ROM
One hardware reference manual

Physical Characteristics

Probe Buffer Box

Height: 0.75 in. (19 mm)
Length: 7.25 in. (184 mm)
Width: 3.75 in. (95 mm)

User System Interconnect Cable

Width: 2¼ in. (57 mm)
Length: 16 in. (406 mm) flat cable

μ Scope 820 Console Personality ROM PC Card

Height: ¾ in. (19 mm)
Width: 2¼ in. (57 mm)
Length: 3¼ in. (83 mm)

Electrical Characteristics

All DC specifications are in addition to user system parameters. All capacitance values include cables and connectors.

Non-Intercepted Signals

$\emptyset 1, \emptyset 2$	$\pm 10 \mu\text{A}$ max; 55 pF typ
$A_{15}-A_0, D_7-D_0$	-0.25 mA max @ 0.45V; $30 \mu\text{A}$ max @ 5.25V; 49 pF typ
+ 12V Supply	15 μA max
WAIT	35 pF typ (capacitance loading only)

Intercepted Signals

Outputs to User System	
SYNC	20 mA min @ 0.5V; -1 mA min @ 2.7V; 40 pF typ
HOLDA, INTE, DBIN, and $\overline{\text{WR}}$	4 mA min @ 0.4V; -0.2 mA min @ 2.7V; 40 pF typ
Inputs from User System	
INT, READY, RESET	40 μA max @ 2.7V; -0.72 mA max @ 0.4V; 50 pF typ
HOLD	60 μA max @ 2.7V; -1.08 mA max @ 0.4V; 50 pF typ

Power Requirements — Power supplied by μ Scope 820 Microprocessor System Console.

Environmental Characteristics

Operating Temperature — 0°C to 55°C (32°F to 130°F)

Storage Temperature — -40°C to 75°C (-40°F to 167°F)

Humidity — 95% RH, 15°C to 40°C (59°F to 104°F) non-condensing

Reference Manuals

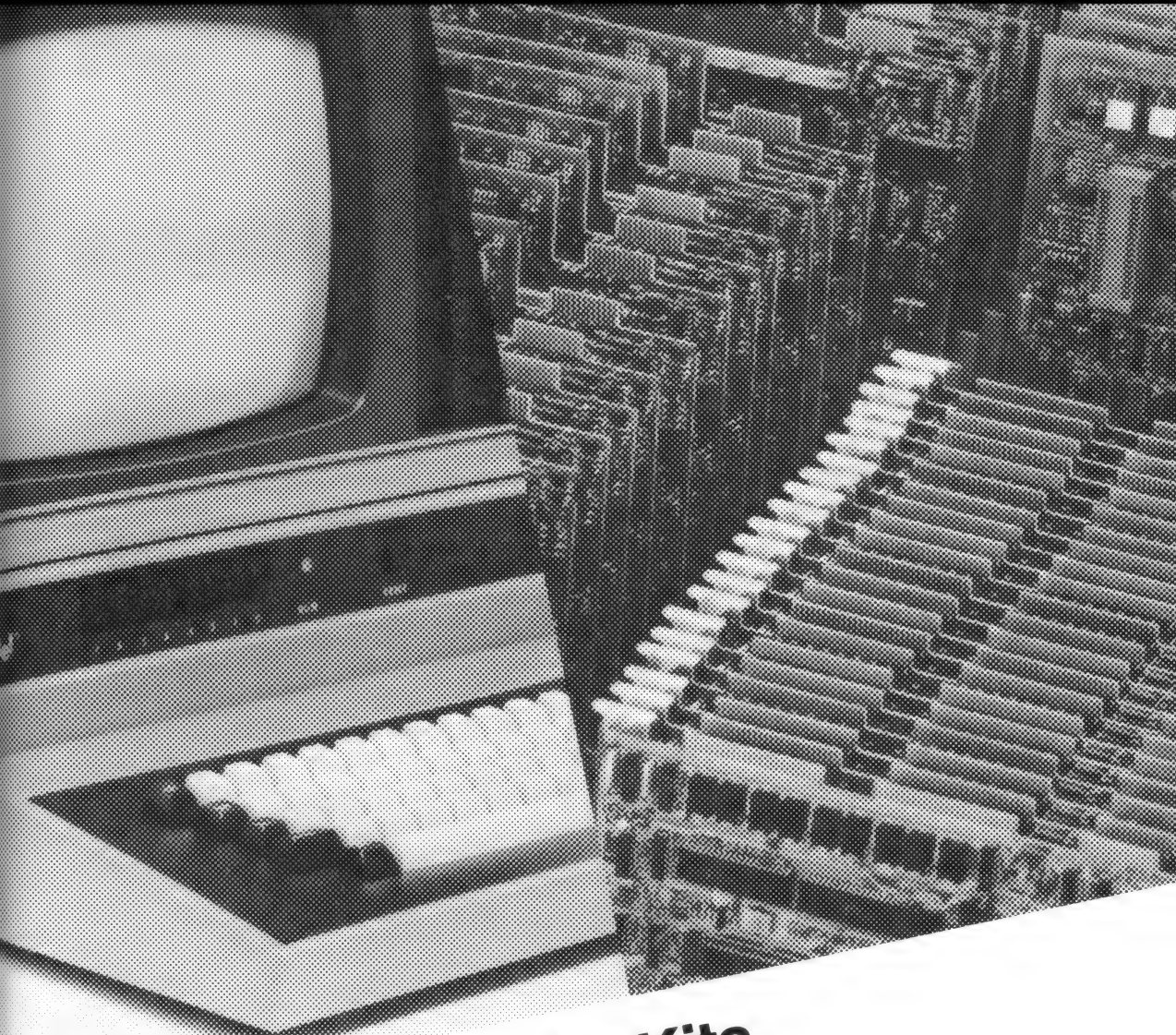
9800526 — μ Scope 820 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

PRB-80 8080A interface probe



13 Kits

KITS

INTRODUCTION

This section provides information on the SDK-85 MCS-85 System Design Kit, Intel's complete single board microcomputer system in kit form. The kit contains all the necessary components to build a useful, functional system in three to five hours. It is designed around the Intel 8085A microprocessor, and included in this section is a complete 8085A instruction set of mnemonics, functions, and instruction codes.

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SDK-85 MCS-85 SYSTEM DESIGN KIT

Complete single board microcomputer system including CPU, memory, and I/O

Easy to assemble, low cost, kit form

Extensive system monitor software in ROM

Interactive LED display and keyboard

Large wire-wrap area for custom interfaces

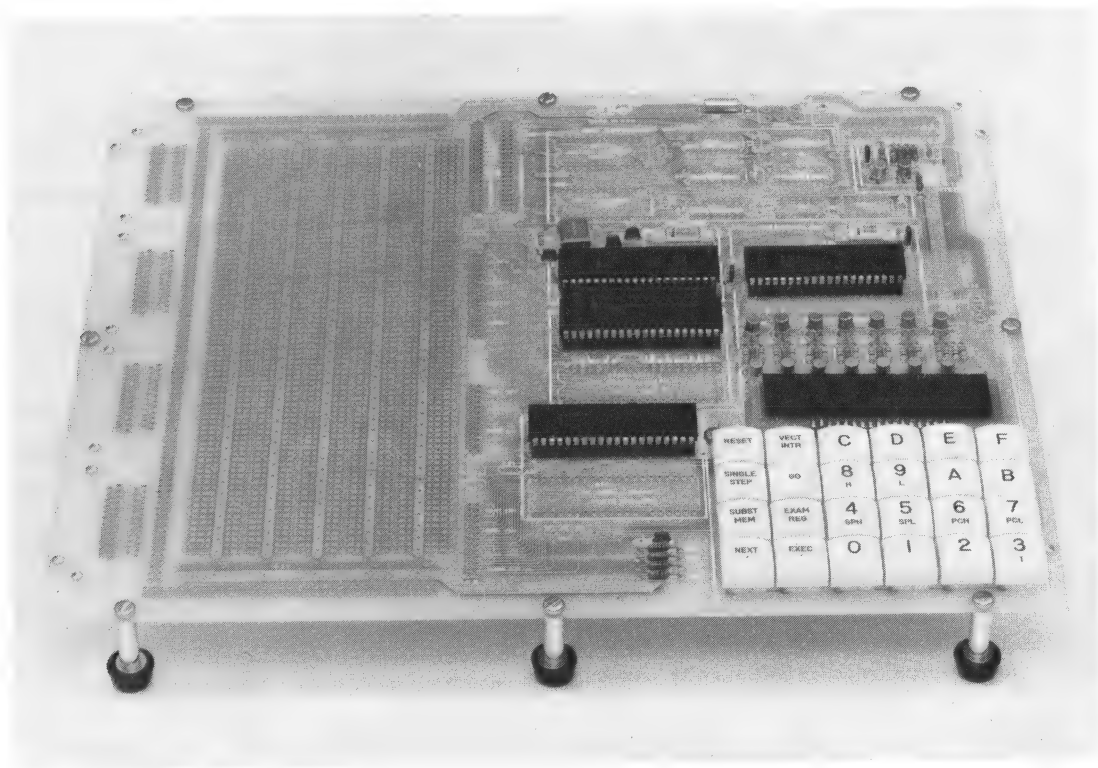
Popular 8080A instruction set

Interfaces directly with TTY

High performance 3 MHz 8085A CPU (1.3 μ s instruction cycle)

Comprehensive design library included

The SDK-85 MCS—85 System Design Kit is a complete single board microcomputer system in kit form. It contains all components required to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included is a preprogrammed ROM containing a system monitor for general software utilities and system diagnostics. The complete kit includes a 6-digit LED display and a 24-key keyboard for a direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal. The SDK-85 is an inexpensive, high performance prototype system that has designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-85 is a complete 8085A microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, capacitors, and sockets are included. Assembly time varies from three to five hours, depending on the skill of the user. The SDK-85 functional block diagram is shown in Figure 1.

8085A Processor

The SDK-85 is designed around Intel's 8085A microprocessor. The Intel 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software upward compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085A (CPU), 8156 (RAM), and 8355/8755 (ROM/PROM). A block diagram of the 8085A microprocessor is shown in Figure 2.

System Integration — The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

Addressing — The 8085A uses a multiplexed data bus. The 16-bit address is split between the 8-bit address bus and the 8-bit address/data bus. The on-chip address latches of 8155/8156/8355/8755 memory products allows a direct interface with the 8085A.

System Monitor

A compact but powerful system monitor is supplied with the SDK-85 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

Communications Interface

The SDK-85 communicates with the outside world through either the on-board LED display/keyboard combination, or the user's TTY terminal (jumper selectable).

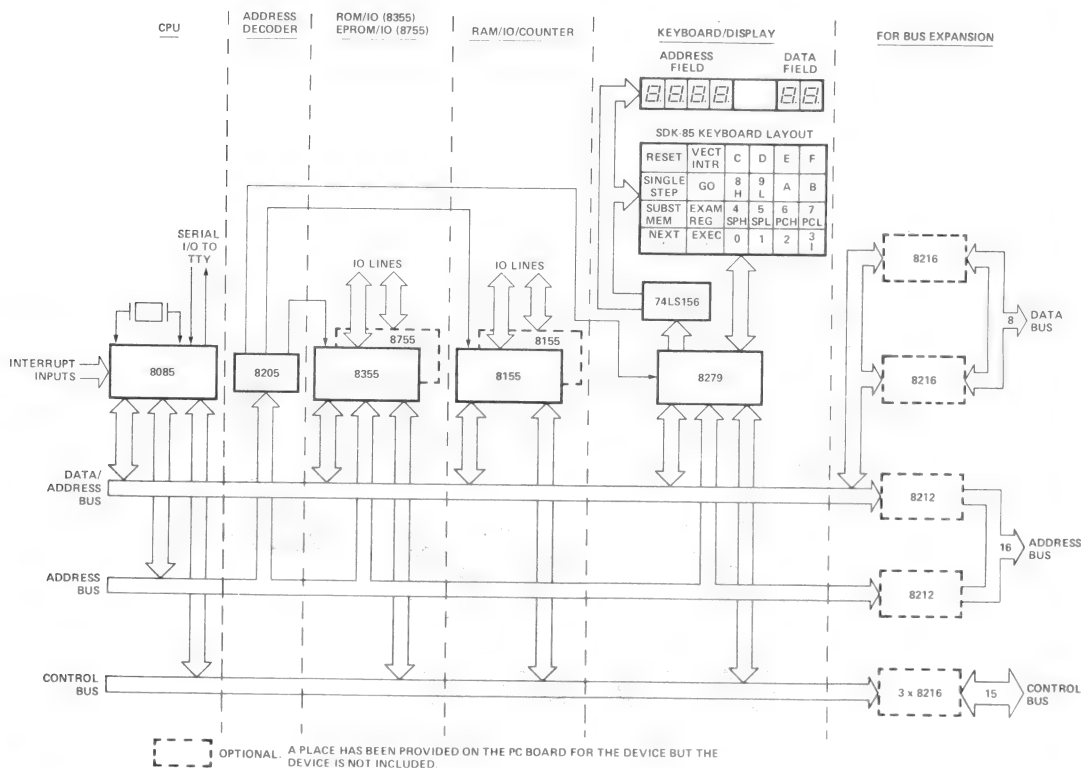
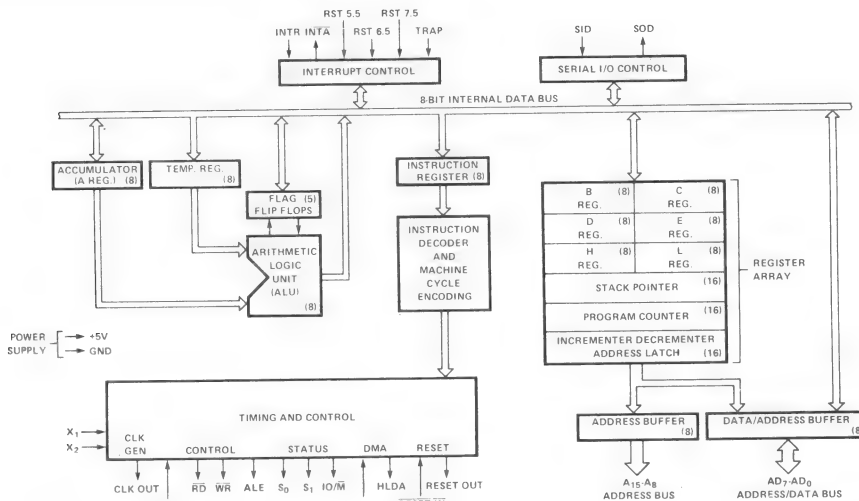


Figure 1. SDK-85 System Design Kit Functional Block Diagram



- SEVEN 8-BIT REGISTERS. SIX OF THEM CAN BE LINKED IN REGISTER PAIRS FOR CERTAIN OPERATIONS.
- 8-BIT ALU.
- 16-BIT STACK POINTER (STACK IS MAINTAINED OFFBOARD IN SYSTEM RAM MEMORY).
- 16-BIT PROGRAM COUNTER.

Figure 2. 8085A Microprocessor Block Diagram

Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (45 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-85 user's manual contains step-by-step instructions for easy assembly without mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-85 is ready to go. The monitor starts immediately upon power-on or reset.

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program.
Single step	Allows user to execute user program one instruction at a time—useful for debugging.
Substitute memory	Allows user to examine and modify memory locations.
Examine register	Allows user to examine and modify 8085A's register contents.
Vector interrupt	Serves as user interrupt button.

Table 1. Keyboard Monitor Commands

Commands — Keyboard monitor commands and teletype monitor commands are provided in Table 1 and Table 2, respectively.

Command	Operation
Display memory	Displays multiple memory locations.
Substitute memory	Allows user to examine and modify memory locations one at a time.
Insert instructions	Allows user to store multiple bytes in memory.
Move memory	Allows user to move blocks of data in memory.
Examine register	Allows user to examine and modify the 8085A's register contents.
Go	Allows user to execute user programs.

Table 2. Teletype Monitor Commands

Documentation

In addition to detailed information on using the monitors, the SDK-85 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-85 is shown in Figure 3 and listed in the Specifications section under Reference Manuals.



Figure 3. SDK-85 Design Library

8085A INSTRUCTION SET

Table 3 contains a summary of processor instructions used for the 8085A microprocessor.

Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
MOVE, LOAD, AND STORE										
MOV r1r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M.r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r.M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
OTHER INSTRUCTIONS										
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12

continued

Mnemonic ¹	Description	Instruction Code ²								Clock ³ Cycles
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
DCX B	Decrement B & C registers	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E registers	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L registers	0	0	1	0	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupts	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085 INSTRUCTIONS										
RIM	Read interrupt mask	0	0	1	0	0	0	0	0	4
SIM	Set interrupt mask	0	0	1	1	0	0	0	0	4

Notes

1. All mnemonics copyright © Intel Corporation 1977.
2. DDD or SSS: B=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
3. Two possible cycle times. (6/12) indicates instruction cycles dependent on condition flags.

Table 3. Summary of 8085A Processor Instructions

SPECIFICATIONS

Central Processor

CPU — 8085A

Instruction Cycle — 1.3 µs

T_{cy} — 330 ns

Memory

ROM — 2K bytes (expandable to 4K bytes) 8355/8755A

RAM — 256 bytes (expandable to 512 bytes) 8155

Addressing

ROM — 0000-07FF (expandable to 0FFF with an additional 8355/8755A)

RAM — 2000-20FF (2800-28FF available with an additional 8155)

Note

The wire-wrap area of the SDK-85 PC board may be used for additional custom memory expansion up to the 64K-byte addressing limit of the 8085A.

Input/Output

Parallel — 38 lines (expandable to 76 lines)

Serial — Through SID/SOD ports of 8085A. Software generated baud rate.

Baud Rate — 110

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — 20 mA current loop TTY

Note

By populating the buffer area of the board, the user has access to all bus signals that enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts

Three Levels

(RST 7.5) — Keyboard interrupt

(RST 6.5) — TTL input

(INTR) — TTL input

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Pre-programmed 8755A or 8355 ROM

Addresses — 0000-07FF

Monitor I/O — Keyboard/display or TTY (serial I/O)

Physical Characteristics

Width — 12.0 in. (30.5 cm)

Height — 10 in. (25.4 cm)

Depth — 0.50 in. (1.27 cm)

Weight — approx. 12 oz

Electrical Characteristics

DC Power Requirement (power supply not included in kit)

Voltage	Current
$V_{CC} 5V \pm 5\%$	1.3A
$V_{TTY} - 10V \pm 10\%$	0.3A (V_{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0-55°C

Reference Manuals

9800451 — SDK-85 User's Manual (SUPPLIED)

9800366 — MCS-85 User's Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

8085/8080 Assembly Language Reference Card (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number Description

SDK-85 MCS-85 system design kit

SDK-86 MCS-86 SYSTEM DESIGN KIT

PRELIMINARY

Complete single board microcomputer system including CPU, memory, and I/O

Interactive LED display and keyboard

Easy to assemble kit form

Wire wrap area for custom interfaces

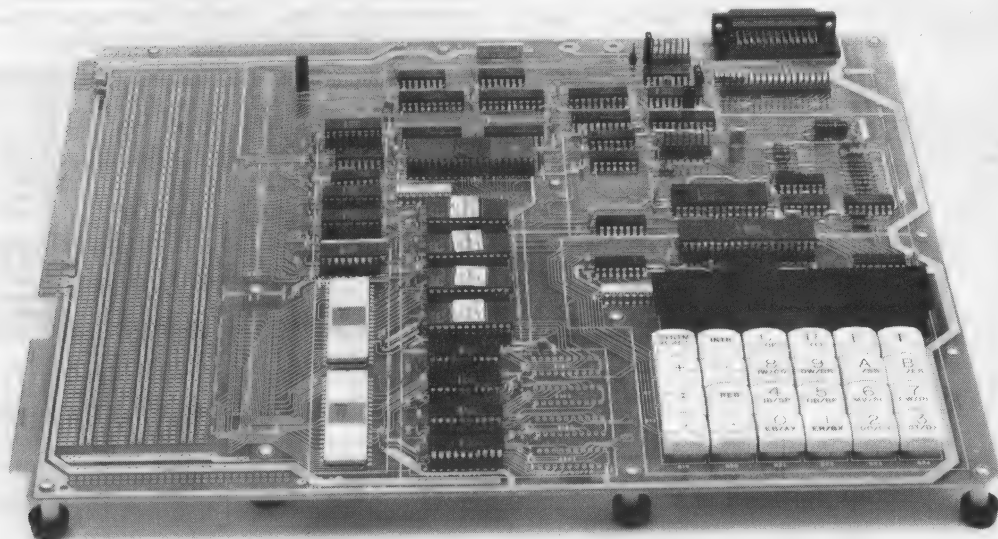
High performance 8086 16-bit CPU

Extensive system monitor software in ROM

Interfaces directly with TTY or CRT

Comprehensive design library included

The SDK-86 MCS-86 System Design Kit is a complete single board 8086 microcomputer system in kit form. It contains all necessary components to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included are preprogrammed ROMs containing a system monitor for general software utilities and system diagnostics. The complete kit includes an 8-digit LED display and a mnemonic 24-key keyboard for direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal, CRT terminal, or the serial port of an Intellec system. The SDK-86 is a high performance prototype system with designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-86 is a complete MCS-86 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, and sockets are included. Assembly time varies from 4 to 10 hours, depending on the skill of the user. The SDK-86 functional block diagram is shown in Figure 1.

8086 Processor

The SDK-86 is designed around Intel's 8086 microprocessor. The Intel 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor features attributes of both 8-bit and 16-bit microprocessors in that it address memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. Additional features of the 8086 include the following:

- Direct addressing capability to one megabyte of memory
- Assembly language compatible with 8080/8085
- 14 word x 16-bit register set with symmetrical operations
- 24 operand addressing modes
- Bit, byte, word, and block operations
- 8 and 16-byte signed and unsigned arithmetic in binary or decimal mode, including multiply and divide
- 5 MHz clock rate
- MULTIBUS compatible system interface

A block diagram of the 8086 microprocessor is shown in Figure 2.

System Monitor

A compact but powerful system monitor is supplied with the SDK-86 to provide general software utilities and system diagnostics. It comes in preprogrammed ROMs.

Communications Interface

The SDK-86 communicates with the outside world through either the on-board LED display/keyboard combination or the user's TTY or CRT terminal (jumper selectable), or by means of a special mode in which an Intellec development system transports finished programs to and from the SDK-86. Memory may be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (22 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-86 assembly manual contains step-by-step instructions for easy assembly with a minimum of mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-86 is ready to go. The monitor starts immediately upon power-on or reset.

Commands — Keyboard mode commands, serial port commands, and Intellec slave mode commands are summarized in Table 1, Table 2, and Table 3, respectively. The SDK-86 keyboard is shown in Figure 3.

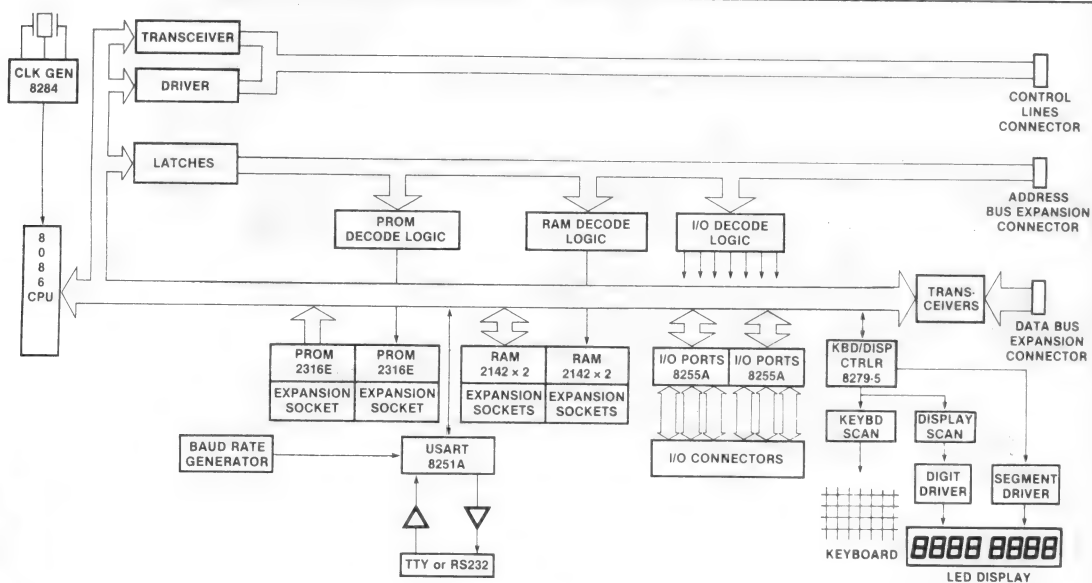


Figure 1. SDK-86 System Design Kit Functional Block Diagram

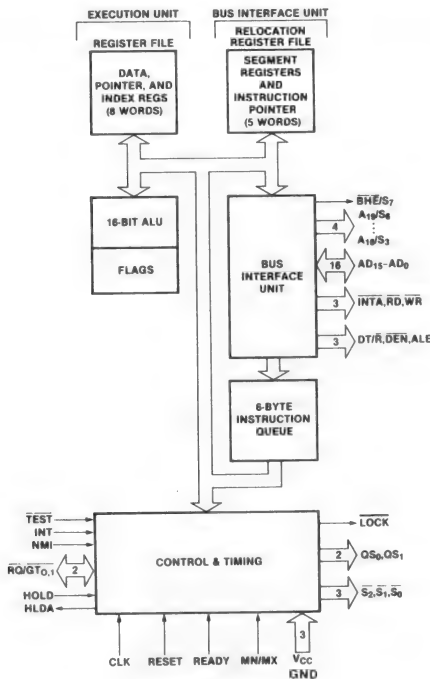


Figure 2. 8086 Microprocessor Block Diagram

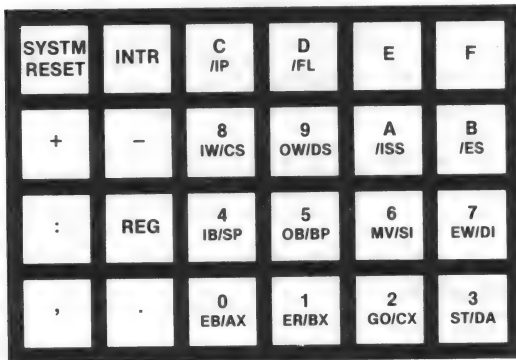


Figure 3. SDK-86 Keyboard

Documentation

In addition to detailed information on using the monitors, the SDK-86 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-86 is shown in Figure 4 and listed in the Specifications section under Reference Manuals.



Figure 4. SDK-86 Design Library

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program, and causes it to halt at predetermined program stop. Useful for debugging.
Single step	Allows user to execute user program one instruction at a time. Useful for debugging.
Substitute memory	Allows user to examine and modify memory locations in byte or word mode.
Examine register	Allows user to examine and modify 8086 register contents.
Block move	Allows user to relocate program and data portions in memory.
Input or output	Allows direct control of SDK-86 I/O facilities in byte or mode.

Table 1. Keyboard Mode Commands

Command	Operation
Dump memory	Allows user to print or display blocks of memory information larger than amount visible on terminal's CRT display.
Start/continue display	Allows user to display blocks of memory information larger than amount visible on terminal's CRT display.
Punch/read paper tape	Allows user to transmit finished programs into and out of SDK-86 via TTY paper tape punch.

Table 2. Serial Mode Commands

Command	Operation
Up/download	Allows user to transport finished programs between Intellec and SDK-86, using special Intellec utility program.
Note The Intellec slave mode utilizes all the keyboard mode commands and serial mode commands (listed in Tables 1 and 2, respectively), as well as the up/download slave mode command, via the console of the Intellec development system.	

Table 3. Intellec Slave Mode Commands

8086 INSTRUCTION SET

Table 4 contains a summary of processor instructions used for the 8086 microprocessor.

Mnemonic and Description	Instruction Code	Mnemonic and Description	Instruction Code
DATA TRANSFER		CMP - Compare:	
MOV - Move:	7 8 5 4 3 2 1 0 7 8 5 4 3 2 1 0 7 8 5 4 3 2 1 0 7 8 5 4 3 2 1 0	Register/memory and register	0 0 1 1 1 0 d w mod reg r/m
Register/memory to/from register	1 0 0 0 1 0 d w mod reg r/m	Immediate with register/memory	1 0 0 0 0 s w mod 1 1 1 r/m data data if s=w-01
Immediate to register/memory	1 1 0 0 0 1 1 w mod 0 0 0 r/m data data if w=1	Immediate with accumulator	0 0 1 1 1 0 w data data if w=1
Immediate to register	1 0 1 1 w reg data data if w=1	AAS -ASCII adjust for subtract	0 0 1 1 1 1 1
Memory to accumulator	1 0 1 0 0 0 w addr-low addr-high	DAS -Decimal adjust for subtract	0 0 1 0 1 1 1
Accumulator to memory	1 0 1 0 0 0 1 w addr-low addr-high	MUL -Multiply (unsigned)	1 1 1 1 0 1 1 w mod 1 0 0 r/m
Register/memory to segment register	1 0 0 0 1 1 1 0 mod 0 reg r/m	IMUL -Integer multiply (signed)	1 1 1 1 0 1 1 w mod 1 0 1 r/m
Segment register to register/memory	1 0 0 0 1 1 0 0 mod 0 reg r/m	AAM -ASCII adjust for multiply	1 1 0 1 0 1 0 0 0 0 0 1 0 1 0
PUSH - Push:		DIV -Divide (unsigned)	1 1 1 1 0 1 1 w mod 1 1 0 r/m
Register/memory	1 1 1 1 1 1 1 1 mod 1 1 0 r/m	IDIV -Integer divide (signed)	1 1 1 1 0 1 1 w mod 1 1 1 r/m
Register	0 1 0 1 0 reg	AAD -ASCII adjust for divide	1 1 0 1 0 1 0 1 0 0 0 0 1 0 1 0
Segment register	0 0 0 reg 1 1 0	CBW -Convert byte to word	1 0 0 1 1 0 0 0
POP - Pop:		CWD -Convert word to double word	1 0 0 1 1 0 0 1
Register/memory	1 0 0 0 1 1 1 1 mod 0 0 0 r/m	LOGIC	
Register	0 1 0 1 1 reg	NOT -Invert	1 1 1 1 0 1 1 w mod 0 1 0 r/m
Segment register	0 0 0 reg 1 1 1	SHL/SAL -Shift logical/arithmetic left	1 1 0 1 0 0 v w mod 1 0 0 r/m
XCHG - Exchange:		SHR -Shift logical right	1 1 0 1 0 0 v w mod 1 0 1 r/m
Register/memory with register	1 0 0 0 0 1 1 w mod reg r/m	SAR -Shift arithmetic right	1 1 0 1 0 0 v w mod 1 1 1 r/m
Register with accumulator	1 0 0 1 0 reg	ROL -Rotate left	1 1 0 1 0 0 v w mod 0 0 0 r/m
IN/INW - Input to AL/AX from:		ROR -Rotate right	1 1 0 1 0 0 v w mod 0 0 1 r/m
Fixed port	1 1 1 0 0 1 0 w port	RCL -Rotate through carry flag left	1 1 0 1 0 0 v w mod 0 1 0 r/m
Variable port	1 1 1 0 1 1 0 w	RCR -Rotate through carry right	1 1 0 1 0 0 v w mod 0 1 1 r/m
OUT/OUTW - Output from AL/AX to:		AND - And:	
Fixed port	1 1 1 0 0 1 1 w port	Reg./memory and register to either	0 0 1 0 0 0 d w mod reg r/m
Variable port	1 1 1 0 1 1 1 w	Immediate to register/memory	1 0 0 0 0 0 w mod 1 0 0 r/m data data if w=1
XLAT -Translate byte to AL	1 1 0 1 0 1 1 1	Immediate to accumulator	0 0 1 0 0 1 0 w data data if w=1
LEA -Load EA to register	1 0 0 0 1 1 0 1 mod reg r/m	TEST - And function to flags, no result:	
LDS -Load pointer to DS	1 1 0 0 0 1 0 1 mod reg r/m	Register/memory and register	1 0 0 0 0 1 0 w mod reg r/m
LES -Load pointer to ES	1 1 0 0 0 1 0 0 mod reg r/m	Immediate data and register/memory	1 1 1 1 0 1 1 w mod 0 0 0 r/m data data if w=1
LANP -Load AH with flags	1 0 0 1 1 1 1 1	Immediate data and accumulator	1 0 1 0 1 0 0 w data data if w=1
SANP -Store AH into flags	1 0 0 1 1 1 1 0	OR - Or:	
PUSHF -Push flags	1 0 0 1 1 1 0 0	Reg./memory and register to either	0 0 0 0 1 0 d w mod reg r/m
POPF -Pop flags	1 0 0 1 1 1 0 1	Immediate to register/memory	1 0 0 0 0 0 w mod 0 0 1 r/m data data if w=1
ARITHMETIC		Immediate to accumulator	0 0 0 0 1 1 0 w data data if w=1
ADD - Add:		XOR - Exclusive or:	
Reg./memory with register to either	0 0 0 0 0 d w mod reg r/m	Reg./memory and register to either	0 0 1 1 0 d w mod reg r/m
Immediate to register/memory	1 0 0 0 0 s w mod 0 0 0 r/m data data if s=w-01	Immediate to register/memory	1 0 0 0 0 0 w mod 1 1 0 r/m data data if w=1
Immediate to accumulator	0 0 0 0 0 1 0 w data data if w=1	Immediate to accumulator	0 0 1 1 0 1 0 w data data if w=1
ADC -Add with carry:		STRING MANIPULATION	
Reg./memory with register to either	0 0 0 1 0 d w mod reg r/m	REP -Repeat	1 1 1 1 0 0 1 z
Immediate to register/memory	1 0 0 0 0 s w mod 0 1 0 r/m data data if s=w-01	MOV/MOVW -Move byte/word	1 0 1 0 0 1 0 w
Immediate to accumulator	0 0 0 1 0 1 0 w data data if w=1	CMPS/CMPSW -Compare byte/word	1 0 1 0 0 1 1 w
INC - Increment:		SCAS/SCASW -Scan byte/word	1 0 1 0 1 1 1 w
Register/memory	1 1 1 1 1 1 1 w mod 0 0 0 r/m	LODS/LODSW -Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
Register	0 1 0 0 0 reg	STOS/STOSW -Store byte/wd from AL/AX	1 0 1 0 1 0 1 w
AAA -ASCII adjust for add	0 0 1 1 0 1 1 1	CONTROL TRANSFER	
DAA -Decimal adjust for add	0 0 1 0 0 1 1 1	CALL - Call:	
DEC - Subtract:		Direct within segment	1 1 1 1 0 0 0 0 disp-low disp-high
Reg./memory and register to either	0 0 1 0 1 0 d w mod reg r/m	Indirect within segment	1 1 1 1 1 1 1 1 mod 0 1 0 r/m
Immediate from register/memory	1 0 0 0 0 s w mod 1 0 1 r/m data data if s=w-01	Direct intersegment	1 0 0 1 1 0 1 0 offset-low offset-high
Immediate from accumulator	0 0 1 0 1 1 0 w data data if w=1	Indirect intersegment	1 1 1 1 1 1 1 1 mod 0 1 1 r/m
SSB - Subtract with borrow			
Reg./memory and register to either	0 0 0 1 1 0 d w mod reg r/m		
Immediate from register/memory	1 0 0 0 0 s w mod 0 1 1 r/m data data if s=w-01		
Immediate from accumulator	0 0 0 1 1 1 0 w data data if w=1		
DEC - Decrement:			
Register/memory	1 1 1 1 1 1 1 w mod 0 0 1 r/m		
Register	0 1 0 0 1 reg		
NEG -Change sign	1 1 1 1 0 1 1 w mod 0 1 1 r/m		

continued

Mnemonic and Description	Instruction Code			Mnemonic and Description	Instruction Code		
JMP - Unconditional Jump:	7 8 5 4 3 2 1 0	7 8 5 4 3 2 1 0	7 8 5 4 3 2 1 0		7 8 5 4 3 2 1 0	7 8 5 4 3 2 1 0	
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high	JNB-Jump on not sign	0 1 1 1 0 0 1	disp	
Direct within segment-short	1 1 1 0 1 0 1 1	disp		LOOP-Loop CX times	1 1 1 0 0 0 1 0	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		LOOPZ/LOOPPE-Loop while zero/equal	1 1 1 0 0 0 0 1	disp	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	LOOPNZ/LOOPNE-Loop while not zero/equal	1 1 1 0 0 0 0 0	disp	
		seg-low	seg-high	JCXZ-Jump on CX zero	1 1 1 0 0 0 1 1	disp	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m					
RET - Return from CALL:				INT Interrupt			
Within segment	1 1 0 0 0 0 1 1			Type specified	1 1 0 0 1 1 0 1	type	
Within seg. adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high	Type 3	1 1 0 0 1 1 0 0		
Intersegment	1 1 0 0 1 0 1 1			INTO-Interrupt on overflow	1 1 0 0 1 1 1 0		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	IRET-Interrupt return	1 1 0 0 1 1 1 1		
JE/JZ-Jump on equal/zero	0 1 1 1 0 1 0 0	disp					
JL/JNBE-Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp		PROCESSOR CONTROL			
JLE/JNB-Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp		CLC-Clear carry	1 1 1 1 1 0 0 0		
JJB/JNAE-Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp		CMC-Complement carry	1 1 1 1 1 0 1 0		
JBE/JNA-Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp		STC-Set carry	1 1 1 1 1 0 0 1		
JP/JPE-Jump on parity/parity even	0 1 1 1 1 0 1 0	disp		CLD-Clear direction	1 1 1 1 1 1 0 0		
JOB-Jump on overflow	0 1 1 1 0 0 0 0	disp		STD-Set direction	1 1 1 1 1 1 0 1		
JB-Jump on sign	0 1 1 1 1 0 0 0	disp		CLI-Clear interrupt	1 1 1 1 1 1 0 1 0		
JNB/JNZ-Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp		STI-Set interrupt	1 1 1 1 1 0 1 1		
JNL/JBE-Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp		NLT-Halt	1 1 1 1 0 1 0 0		
JNLE/JB-Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp		WAIT-Wait	1 0 0 1 1 0 1 1		
JNB/JAE-Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp		ESC-Escape (to external device)	1 1 0 1 1 x	mod x r/m	
JNBE/JA-Jump on not below or equal/above	0 1 1 1 1 0 1 1	disp		LOCK-Bus lock prefix	1 1 1 1 0 0 0 0		
JNP/JNB-Jump on not par/par odd	0 1 1 1 1 0 1 1	disp					
JNO-Jump on not overflow	0 1 1 1 0 0 0 1	disp					

Notes

AL - 8-bit accumulator
 AX - 16-bit accumulator
 CX - Count register
 DS - Data segment
 ES - Extra segment
 Above/below refers to unsigned value.
 Greater = more positive;
 Less = less positive (more negative) signed values
 if d = 1 then "to"; if d = 0 then "from"
 if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
 if mod = 00 then DISP = 0*, disp-low and disp-high are absent
 if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
 if mod = 10 then DISP = disp-high; disp-low
 if r/m = 000 then EA = (BX) + (SI) + DISP
 if r/m = 001 then EA = (BX) + (DI) + DISP
 if r/m = 010 then EA = (BP) + (SI) + DISP
 if r/m = 011 then EA = (BP) + (DI) + DISP
 if r/m = 100 then EA = (SI) + DISP
 if r/m = 101 then EA = (DI) + DISP
 if r/m = 110 then EA = (BP) + DISP*
 if r/m = 111 then EA = (BX) + DISP
 DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high; disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
 if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
 if v = 0 then "count" = 1; if v = 0 then "count" in (CL)
 x = don't care.
 if v = 0 then "count" = 1; if v = 1 then "count" in (CL) register.
 z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics © Intel, 1978

Table 4. 8086 Instruction Set Summary

SPECIFICATIONS

Central Processor

CPU — 8086-4

Note

May be operated at 2.5 MHz or 5 MHz, jumper selectable, for use with 8086.

Memory

ROM — 8K bytes 2316/2716

RAM — 2K bytes (expandable to 4K bytes) 2142

Addressing

ROM — FE000-FFFFF

RAM — 0-7FF (800-FFF available with additional 2142's)

Note

The wire-wrap area of the SDK-86 PC board may be used for additional custom memory expansion.

Input/Output

Parallel — 48 lines (two 8255A's)

Serial — RS232 or current loop (8251A)

Baud Rate — selectable from 110 to 4800 baud

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — 20 mA current loop TTY or RS232

Note

The user has access to all bus signals which enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts (256 vectored)

Maskable

Non-maskable

TRAP

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Preprogrammed 2716 or 2316 ROMs

Addresses — FE000-FFFF

Monitor I/O — Keyboard/display or TTY or CRT (serial I/O)

Physical Characteristics

Width — 13.5 in. (34.3 cm)

Height — 12 in. (30.5 cm)

Depth — 1.75 in. (4.45 cm)

Weight — approx. 24 oz. (3.3 kg)

Electrical Characteristics

DC Power Requirement

(Power supply not included in kit)

Voltage	Current
$V_{CC} 5V \pm 5\%$	3.5A
$V_{TTY} - 12V \pm 10\%$	0.3A
(V _{TTY} required only if teletype is connected)	

Environmental Characteristics

Operating Temperature — 0-50°C

Reference Manuals

9800697A — SDK-86 MCS-86 System Design Kit Assembly Manual

9800722 — MCS-86 User's Manual

9800640A — 8086 Assembly Language Programming Manual

8086 Assembly Language Reference Card

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SDK-86	MCS-86 system design kit



14 Microcomputer Training

MICROCOMPUTER TRAINING PROGRAMS

INTRODUCTION

Intel provides complete training for all its system related products. Courses are given regularly at Intel's training centers located in Santa Clara, California; Boston, Massachusetts; and Chicago, Illinois. These training centers are staffed by highly trained and experienced instructors. This section describes the overall program for microcomputer training and provides outlines for the following courses offered by Intel: the MCS-80/85 system workshop, the PL/M-80 language/software design workshop, the RMX/80 real-time multi-tasking executive system workshop, the MCS-48 system workshop, the MCS-86 system workshop, and the PL/M-86 language/software design workshop.

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Microcomputer Training Programs	14-3
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MICROCOMPUTER TRAINING PROGRAMS

**Courses presented at training centers
and customer facilities**

Training center locations

- Boston
- Chicago
- Santa Clara

**Scheduled on a continuing basis
throughout the year**

**On-site courses tuned to customer
requirements**

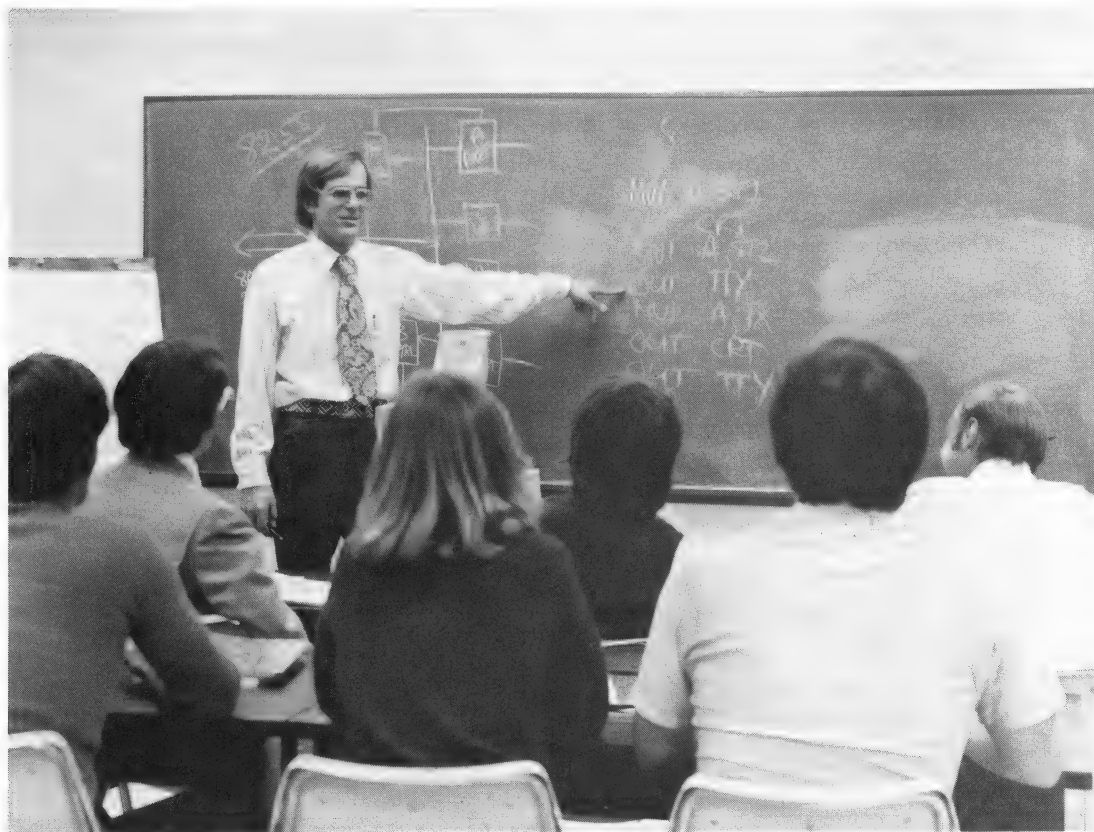
System demonstration

**Hands-on laboratory sessions reinforce
lecture**

**Training center classes limited to 14
attendees**

**Intellec microcomputer development
systems with in-circuit emulators used
in laboratory**

Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel offers a selection of workshops designed to provide users with the tools for making optimum use of Intel microcomputers in system development.



COURSE DESCRIPTIONS

MCS-80/85 System Workshop

This workshop will prepare the student to design and develop a system using Intel 8080/8085 microprocessors by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcom-

puter Development System and an in-circuit emulator. The course outline for this workshop is presented in Table 1.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is recommended.

<p>Day 1</p> <p>Introduction</p> <ol style="list-style-type: none"> Microprocessor system <ol style="list-style-type: none"> Function Organization Programming Central processor overview <ol style="list-style-type: none"> Functional sections Programming model Execution sequence <p>Assembly Language Instructions</p> <ol style="list-style-type: none"> Input/output Register/memory reference Arithmetic, logical, rotates <p>Programmed Input/Output</p> <ol style="list-style-type: none"> Status request Command Data transfer <p>Development System</p> <ol style="list-style-type: none"> Function System monitor Disk operating system <p>Debugging With the System Monitor</p> <ol style="list-style-type: none"> Breakpoints Examine registers <p>Laboratory</p> <ol style="list-style-type: none"> Using the system monitor Program instruction sequences Debugging and breakpoints <p>Day 2</p> <p>Disk Operating System Modules</p> <ol style="list-style-type: none"> Macroassembler Text editor File utility commands <p>System Timing</p> <ol style="list-style-type: none"> Instructions State transition Signal relationships Specifications <p>Subroutines</p> <ol style="list-style-type: none"> Invocation Stack memory Parameters <p>Interrupt System</p> <ol style="list-style-type: none"> Description RST instruction Service subroutines <p>Laboratory</p> <ol style="list-style-type: none"> Using the disk operating system Program assembly and execution 	<p>Day 3</p> <p>Branch Tables</p> <ol style="list-style-type: none"> Application Construction <p>Direct load/store instructions</p> <p>Special purpose instruction Macros</p> <ol style="list-style-type: none"> Definition Reference Expansion <p>8080A CPU Set</p> <ol style="list-style-type: none"> 8228/8238 System Controller 8224 Clock Generator RAM/ROM/PROM address decoding Memory mapped I/O <p>8085 CPU Set</p> <ol style="list-style-type: none"> 8085 bus structure 8355/8755 ROM/EPROM and I/O 8155 RAM/Timer and I/O <p>Laboratory</p> <ol style="list-style-type: none"> Monitor subroutines Program debug under disk operating system <p>Day 4</p> <p>Family Peripherals</p> <ol style="list-style-type: none"> Memory design <ol style="list-style-type: none"> 8708 PROM 2114 RAM I/O design <ol style="list-style-type: none"> 8255 parallel interface 8251 serial interface <p>In-Circuit Emulator</p> <ol style="list-style-type: none"> Prototype development Resource sharing Mapping commands Utility commands Debug commands Emulation syntax <p>Laboratory</p> <ol style="list-style-type: none"> Use of the in-circuit emulator for system debugging <p>Day 5</p> <p>Single Board Computers</p> <ol style="list-style-type: none"> Use as a system component Parallel I/O options Serial I/O options Interrupt system Family boards <p>Relocation and Linkage</p> <ol style="list-style-type: none"> iSIS-II link and locate commands Relocatable libraries Parameter passing System design
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Table 1. MCS-80/85 System Workshop Course Outline

PL/M-80 Language/Software Design Workshop

This workshop will prepare the student for designing, developing, and debugging modular PL/M-80 programs, by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcomputer

Development System and an in-circuit emulator. The course outline for this workshop is presented in Table 2.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design and computer programming is recommended.

Day 1

Introduction

- a. Preview of course
- b. Overview of PL/M, linking, and relocation
- c. Why use a high level language

Definitions

Symbols, identifiers, reserved words, comments, data elements, expressions, statements, declarations

Data Elements

Variables, subscripted variables, data type, constants

Operators, Operations and Priorities

Arithmetic and Boolean

Evaluating Expressions

Statements

Redefine, basic, conditional

Assignment

- a. Implement a given algorithm in PL/M

Day 2

ISIS-II Disc Operating System

- a. Components of system

ISIS-II File Structure

- a. System files
- b. User files
- c. Device files
- d. Directory and file attributes

ISIS-II Commands

- a. CUSPS — Commonly used system programs
- b. Directory and attribute commands
- c. Rename and delete commands
- d. Creating system and user discs

ISIS-II Editor

- a. Definition of terminology
- b. Invoking the editor
- c. Editor commands
- d. Editing existing files

ISIS-II PL/M 80 Compiler

- a. Invoking PL/M
- b. Compiler options

ISIS-II Locate

- a. Invoking locate

Laboratory

- a. Introduction to ISIS-II disc operating system
- b. Creating a PL/M source file
- c. Compiling a PL/M program
- d. Locating and executing a PL/M program

Day 3

Review

Procedures

- a. Declaration
- b. Invocation
- c. Program construction

Data References

- a. Based variables
- b. Variable equivalencing

Statement Labels

Unconditional Transfers

Blocks

- a. Concept and use
- b. Scope of declarations
- c. Modular compilation
- d. Modular program

ISIS-II Link

- a. Invoking link
- b. Link options
- c. Assembly object modules

Laboratory

- a. Compile program modules
- b. Link and locate modules
- c. Execute program

Day 4

Review

ISIS-II Librarian

- a. Creating a library
- b. Managing a library
 1. Adding modules
 2. Deleting modules

ISIS-II System Interfaces

- a. System library

In-Circuit Emulator

- a. Definition
- b. System overview
 1. Memory and I/O mapping
 2. Breakpoint capability
 3. Dynamic tracing
 4. Control block

In-Circuit Emulator Software Driver

- a. Modes
- b. Commands

System Debugging Examples

System Demonstration

continued

Laboratory a. Create a library b. Link object to a library c. Locate d. Load and emulate using in-circuit emulator Day 5 Review Interrupt Procedures Reentrant Procedures	Predeclared Procedures a. Time, move, length, last, and size procedures b. Type transfers c. Shifts and rotates The Memory Array and STACKPTR Variables Discussion of Selected Programs Laboratory a. Execution and debugging of selected programs
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Table 2. PL/M-80 Language/Software Design Workshop Course Outline

RMX/80 Real-Time Multi-Tasking Executive System Workshop

This workshop will cover the concepts of multi-tasking, i.e., what a task is, concurrency of tasks, asynchronous events, priorities and scheduling, resource sharing, interrupts, and inter-task communication. Also included will be discussions on system design, writing tasks,

system generation, and debugging. The course outline for this workshop is presented in Table 3.

Prerequisites: Prior attendance at the PL/M-80 language/software design workshop. This may be satisfied with an equivalent knowledge of PL/M-80 language and compiler, ISIS-II utility facilities, ISIS-II relocation facilities, and modular systems programming.

Day 1 Introduction a. Preview of workshop What is RMX/80 a. Constituent parts of the RMX/80 product b. Overview of the RMX/80 development process Review of the Development Process a. Intel 8080/8085 translators 1. Assembler 2. PL/M-80 compiler 3. Translator debug option (in-circuit emulator) b. ISIS-II Commands c. Linking task modules with the RMX/80 nucleus and Intel provided tasks d. Locating the final module in an end product environment (single board computer modules) e. Debugging the task environment Real Time Asynchronous Event Processing a. Definition of terminology b. Recognition of asynchronous events 1. Polling (status loop) 2. Preemption (interrupt) c. The single unit program 1. Status environment 2. Interrupt environment d. Program execution 1. Sequential processing 2. Concurrent processing Day 2 RMX/80 Model a. Task 1. Single unit program b. Exchanges and messages 1. SEND function 2. WAIT function	c. Context switching and dispatching of tasks 1. Task states d. A sequential model e. A concurrent model f. The interrupt exchange/message 1. Interrupt levels RMX/80 Terminal Handler a. Message formats b. Service request exchanges 1. Terminal input (line edited) 2. Terminal output c. Service response exchanges Implementing an RMX Task(s) Module a. Translator include option b. Creating a task(s) module c. RMX/80 system creation d. Configuration module e. System generation Laboratory a. Implementation of two modules Day 3 Laboratory a. Implement configuration module and system generation Use of In-Circuit Emulator to Emulate Task System a. Hardware considerations Terminal Handler a. Line edit input b. Control character table c. Alarm exchange — alarm message type d. Debugger and wakeup exchange Debugger Task a. Configuration b. Invoking the debugger c. Debugger commands
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continued

MICROCOMPUTER TRAINING PROGRAMS

<p>Day 4</p> <p>RMX/80 Interrupt Processing</p> <ol style="list-style-type: none"> Interrupt exchanges Enabling and disabling interrupt levels Software priorities and interrupt masking iSBC 80/10 user required interrupt services <ol style="list-style-type: none"> Interrupt poll routines Clock control routines User defined interrupt handling <p>Line Printer Driver Task Example</p> <ol style="list-style-type: none"> Interrupt handling <ol style="list-style-type: none"> Using RMX/80 model User defined handler <p>Analog I/O Tasks</p> <p>High Speed Math Unit Tasks</p> <p>Laboratory</p> <ol style="list-style-type: none"> Interrupt handling 	<p>Day 5</p> <p>Disk File System</p> <ol style="list-style-type: none"> Disk file system services <ol style="list-style-type: none"> File access File read/write File seek Disk I/O Add-on ISIS-II Services <ol style="list-style-type: none"> File attributes File rename File delete Configuration <ol style="list-style-type: none"> Free space manager Concurrent operation File System Structure <ol style="list-style-type: none"> Directory format File data format <p>Laboratory</p> <ol style="list-style-type: none"> Disk file system
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Table 3. RMX/80 Real-Time Multi-Tasking Executive System Workshop Course Outline

MCS-48 System Workshop

This workshop will prepare the student to design and develop a system using the Intel 8049 microprocessor, by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcomputer Development System, the PROMPT-48, and an in-circuit

emulator. The course outline for this workshop is presented in Table 4.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design or computer programming is recommended.

<p>Day 1</p> <p>Orientation</p> <p>Introduction</p> <ol style="list-style-type: none"> Microprocessor system <ol style="list-style-type: none"> Function Organization Programming 8048 overview <ol style="list-style-type: none"> Functional sections Programming model Execution sequence <p>Assembly Language Instructions</p> <ol style="list-style-type: none"> I/O instructions Data move instructions Increment/decrement instructions Branch instructions Work session No. 1 Accumulator group instructions <ol style="list-style-type: none"> ADD/ADDC Logicals <p>PROMPT-48</p> <ol style="list-style-type: none"> Function Operation <p>Laboratory Exercise</p> <ol style="list-style-type: none"> Program entry and execution using PROMPT-48 	<p>Day 2</p> <p>Assembly Language Instructions</p> <ol style="list-style-type: none"> Accumulator group instructions <ol style="list-style-type: none"> Flags Rotates Specials (XCH, DA, SWAP) Worksession No. 2 Subroutines <ol style="list-style-type: none"> Invocation Stack operation Interrupt system <ol style="list-style-type: none"> Description Service subroutines Multiple source systems <p>Development System</p> <ol style="list-style-type: none"> Function Disk operating system <p>Text Editor and Macroassembler</p> <ol style="list-style-type: none"> Function Operation <p>Laboratory Exercise</p> <ol style="list-style-type: none"> Bootstrap procedures Create, edit, and assemble source program Execute program
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continued

MICROCOMPUTER TRAINING PROGRAMS

Day 3

System Timing

- a. Basic timing and timer
- b. Bus timing for peripheral devices

Peripherals and Design

- a. Expanding memory*
 1. Program memory (1, 2K ROMs)
 2. Data memory (RAMs)
- b. Expanding ports (8243)*
 1. Device characteristics
 2. Software control of ports
- c. Combination chips*
 1. 8155 RAM and I/O chip
 2. 8355, 8755 ROM and I/O chip
- d. Peripheral interfacing (parallel)*
 1. 8255 parallel I/O
 2. 8279 keyboard and display interface
 - Keyboard scanning techniques
 - Display refresh

Laboratory Exercise

- a. Edit and assemble using DOS
- b. Execute using PROMPT-48

Day 4

Peripherals and Design

- a. Peripheral interfacing (serial)*
 1. Transmission formats

2. Asynchronous operation
3. RS232C interface

- b. A/D and D/A interfacing*

1. Successive approximation A/D
2. A/D, D/A chips
3. A/D design

Laboratory Exercise

- a. Edit and assemble programs
- b. Execute programs

Day 5

8048 Family

- a. 8041 overview
 1. 8041/8048 difference
 2. 8041 slave/master protocol
- b. 8021 overview
- c. 8049 overview

In-Circuit Emulator

- a. Prototype development
- b. Resource sharing
- c. Commands
 1. Mapping
 2. Utility
 3. Interrogation
 4. Emulation

Laboratory

- a. Use of the in-circuit emulator for system debugging

Note

* Each section will consist of a design example including schematic, bus loading calculations, software, and timing.

Table 4. MCS-48 System Workshop Course Outline

MCS-86 System Workshop

This workshop will prepare the student to develop assembly language programs and design systems based on the Intel 8086 microprocessor through the use of lecture, demonstration, and laboratory "hands-on" experi-

ence with the SDK-86 and the Intel Microcomputer Development System. The course outline for this workshop is presented in Table 5.

Prerequisites: The student has programmed a computer in assembly language and, preferably, is familiar with the 8080/8085 microprocessor.

Day 1

Introduction

- a. Microcomputer system
 1. Function
 2. Memory organization
 3. Interfacing
- b. Central processor overview
 1. Programming
 2. Instruction format

Assembly Language Instruction

- a. Register and data operations
 1. 8-bit
 2. 16-bit
- b. I/O operations

System Design Kit (SDK-86)

- a. Demonstration
- b. Debugging

Laboratory

- a. Using the SDK-86

Day 2

Review

CPU Architecture

- a. Addressing modes

Procedures

- a. Invocation
- b. Stack management
- c. Parameters

Day 3

Review

8086 CPU

- a. Block diagram
- b. Signal description

Interrupt System

- a. Description
- b. Signal pins

8259A — Priority Interrupt Control Unit

continued

MICROCOMPUTER TRAINING PROGRAMS

<p>Development System</p> <ul style="list-style-type: none"> a. ISIS b. Editor c. Demonstration <p>Laboratory</p> <ul style="list-style-type: none"> a. Using the development system <p>Day 4</p> <p>Review</p> <p>Programming for Large Systems</p> <ul style="list-style-type: none"> a. Segmentation registers b. Assembler c. Linkage d. Locate <p>Laboratory</p> <ul style="list-style-type: none"> a. Assembler programming techniques <p>Programming</p> <ul style="list-style-type: none"> a. Arithmetic 	<ul style="list-style-type: none"> b. String operators <p>Day 5</p> <p>CPU Timing</p> <ul style="list-style-type: none"> a. Read cycle b. Memory access time c. Write cycle <p>8284 — Clock Generator</p> <p>8288 — Bus Controller</p> <p>8282/3 — Octal Latch</p> <p>8286/7 — Octal Transceiver</p> <p>Single Board Computer</p> <ul style="list-style-type: none"> a. Design example b. Demonstration <p>Other 8086 Configurations</p> <p>Introduction to PL/M-86</p> <p>Application Techniques</p>
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Table 5. MCS-86 System Workshop Course Outline

PL/M-86 Language/Software Design

Workshop

This workshop will prepare the student for designing, developing, and debugging modular PL/M-86 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec Microcomputer Development System. The course outline for this workshop is presented in Table 6.

ment System. The course outline for this workshop is presented in Table 6.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design and computer programming is recommended.

<p>Day 1</p> <p>Introduction</p> <ul style="list-style-type: none"> a. Preview of course b. Overview of PL/M, linking and relocation c. Why use a high level language <p>Definitions</p> <ul style="list-style-type: none"> a. Symbols, identifiers, reserved words, comments, data elements, expressions, statements, declarations <p>Data Elements</p> <ul style="list-style-type: none"> a. Variables, subscripted variables, constants <p>Data Types</p> <ul style="list-style-type: none"> a. Logical, integer, real <p>Operators, Operations and Priorities</p> <ul style="list-style-type: none"> a. Arithmetic and boolean <p>Evaluating Expressions</p> <p>Statements</p> <ul style="list-style-type: none"> a. Redefine, basic, conditional <p>Assignment</p> <ul style="list-style-type: none"> a. Implement a given algorithm in PL/M 	<p>Day 2</p> <p>ISIS-II Disk Operating System</p> <ul style="list-style-type: none"> a. Components of system <p>ISIS-II File Structure</p> <ul style="list-style-type: none"> a. System files b. User files c. Device files d. Directory and file attributes <p>ISIS-II Commands</p> <ul style="list-style-type: none"> a. CUSPS — Commonly Used System Programs b. Directory and attribute commands c. Rename and delete commands d. Creating system and user disks <p>ISIS-II Editor</p> <ul style="list-style-type: none"> a. Definition of terminology b. Invoking the editor c. Editor commands d. Editing existing files <p>ISIS-II PL/M-86 Compiler</p> <ul style="list-style-type: none"> a. Invoking PL/M b. Compiler options <p>ISIS-II LOC-86</p> <ul style="list-style-type: none"> a. Invoking LOC-86
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continued

<p>Laboratory</p> <ol style="list-style-type: none"> Introduction to ISIS-II disk operating system Creating a PL/M source file Compiling a PL/M program Locating and executing a PL/M program <p>Day 3</p> <p>Review</p> <p>Procedures</p> <ol style="list-style-type: none"> Declaration Invocation Program construction <p>Data References</p> <ol style="list-style-type: none"> Based variables Variable equivalencing Pointer type <p>Statement Labels</p> <p>Unconditional Transfers</p> <p>Blocks</p> <ol style="list-style-type: none"> Concept and use Scope of declarations Modular compilation Modular program <p>ISIS-II LINK-86</p> <ol style="list-style-type: none"> Invoking LINK-86 Link options Assembly object modules <p>Laboratory</p> <ol style="list-style-type: none"> Compile program modules Link and locate modules Execute program 	<p>Day 4</p> <p>Review</p> <p>ISIS-II LIB-86</p> <ol style="list-style-type: none"> Creating a library Managing a library <ol style="list-style-type: none"> Adding modules Deleting modules <p>String Operations</p> <ol style="list-style-type: none"> Move bytes or words Compare bytes or words Find bytes or words Skip bytes or words <p>The LOCKSET Procedure</p> <ol style="list-style-type: none"> Excluding mutual access <p>Laboratory</p> <ol style="list-style-type: none"> Create a library Link object to a library Locate <p>Day 5</p> <p>Review</p> <p>Interrupt Procedures</p> <p>Reentrant Procedures</p> <p>Predeclared Procedures</p> <ol style="list-style-type: none"> TIME, MOVE, LENGTH, LAST and SIZE procedures Type transfers Shifts and rotates <p>The Memory Array and STACKPTR Variables</p> <p>Discussion of Selected Programs</p> <p>Laboratory</p> <ol style="list-style-type: none"> Execution and debugging of selected programs
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Table 6. PL/M-86 Language/Software Design Workshop Course Outline

REGISTRATION AND ADDITIONAL INFORMATION

Contact MCSD Training at Intel Corporation, Santa Clara, California 95051, (408) 987-8003 or 987-8004 or your local Intel sales office.

NOTES

NOTES



NOTES



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